Digital Circuits

- Transfer Characteristics of the Inverter Pair
- One device sizing strategy
- Multiple-input gates
The basic logic gates

It suffices to characterize the inverter of a logic family and then express the performance of other gates in that family in terms of the performance of the inverter.

What characteristics are required and desirable for an inverter to form the basis for a useful logic family?
What are the logic levels for a given inverter of for a given logic family?

$V_H = ?$  $V_L = ?$

Ask the inverter how it will interpret logic levels

- The circuit will interpret them the way they are defined!!
- Analytical expressions may be complicated
- How is this determination made?
Review from Last Time

Ask the inverter how it will interpret logic levels

\[ V_{IN} \rightarrow \text{inverter} \rightarrow V_{OUT} \]

\[ V_H=? \]
\[ V_L=? \]
Ask the inverter how it will interpret logic levels

Inverter pair

When \( V'_{\text{OUT}} = V_{\text{IN}} \), \( V_H \) and \( V_L \) are stable operating points, \( V_{\text{TRIP}} \) is a quasi-stable operating point

Observe: slope of IPTC is greater than 1 at \( V_{\text{TRIP}} \) and less than 1 at \( V_H \) and \( V_L \)
Review from Last Time

Observation

When $V_{OUT} = V_{IN}$ for the inverter, $V'_{OUT}$ is also equal to $V_{IN}$. Thus the intersection point for $V_{OUT} = V_{IN}$ in the inverter transfer characteristics (ITC) is also an intersection point for $V'_{OUT} = V_{IN}$ in the inverter-pair transfer characteristics (IPTC).

Implication: Inverter characteristics can be used directly to obtain $V_{TRIP}$
What properties of an inverter are necessary for it to be useful for building a two-level logic family?

The inverter-pair transfer characteristics must have three unique intersection points with the $V'_{\text{OUT}} = V_{\text{IN}}$ line.

What are the logic levels for a given inverter of for a given logic family?

The two extreme intersection points of the inverter-pair transfer characteristics with the $V'_{\text{OUT}} = V_{\text{IN}}$ line.

Can we legislate $V_H$ and $V_L$ for a logic family? No!

What other properties of the inverter are desirable?

Reasonable separation between $V_H$ and $V_L$ (enough separation so that noise does not cause circuit to interpret level incorrectly).

$$V_{\text{TRIP}} \approx \frac{V_H + V_L}{2}$$

(to provide adequate noise immunity and process insensitivity)
What are the transfer characteristics of the static CMOS inverter pair?

Consider first the inverter.
Transfer characteristics of the static CMOS inverter
Transfer characteristics of the static CMOS inverter
(Neglect λ effects)

**Case 1**  $M_1$ triode, $M_2$ cutoff

$$I_{D1} = \mu_n C_{oxn} \frac{W_1}{L_1} \left( V_{IN} - V_{Tn} - \frac{V_{OUT}}{2} \right) V_{OUT}$$

$$I_{D2} = 0$$

Equating $I_{D1}$ and $-I_{D2}$ we obtain:

$$0 = \mu_n C_{oxn} \frac{W_1}{L_1} \left( V_{IN} - V_{Tn} - \frac{V_{OUT}}{2} \right) V_{OUT}$$

It can be shown that setting the first product term to 0 will not verify, thus

$$V_{OUT} = 0$$

valid for:

$$V_{GS1} \geq V_{Tn} \quad V_{DS1} < V_{GS1} - V_{Tn} \quad V_{GS2} \geq V_{Tp}$$

thus, valid for:

$$V_{IN} \geq V_{Tn} \quad V_{OUT} < V_{IN} - V_{Tn} \quad V_{IN} - V_{DD} \geq V_{Tp}$$
Graphical Interpretation of these conditions:

\[ V_{IN} \geq V_{Tn} \qquad V_{OUT} < V_{IN} - V_{Tn} \qquad V_{IN} - V_{DD} \geq V_{Tp} \]
Transfer characteristics of the static CMOS inverter
(Neglect λ effects)

Case 1  $M_1$ triode, $M_2$ cutoff

$V_{out} = 0$
Transfer characteristics of the static CMOS inverter (Neglect \( \lambda \) effects)

Case 1 \( M_1 \) triode, \( M_2 \) cutoff

\( V_{out} = 0 \)
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

Partial solution:
Transfer characteristics of the static CMOS inverter
(Neglect \( \lambda \) effects)

Case 2  \( M_1 \) triode, \( M_2 \) sat
Transfer characteristics of the static CMOS inverter
(Neglect λ effects)

Case 1  \( M_1 \) triode, \( M_2 \) cutoff

\[ V_{\text{OUT}} = 0 \]
Transfer characteristics of the static CMOS inverter
(Neglect λ effects)
Partial solution:
Regions of Operation for Devices in CMOS inverter
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

Case 2  $M_1$ triode, $M_2$ sat
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

Case 2  $M_1$ triode, $M_2$ sat

$$I_{D1} = \mu_n C_{Ox} \frac{W}{L} \left( V_{IN} - V_{Tn} - \frac{V_{OUT}}{2} \right) V_{OUT}$$

$$I_{D2} = -\frac{\mu_p C_{Ox}}{2} \frac{W}{L} \left( V_{IN} - V_{DD} - V_{Tp} \right)^2$$

Equating $I_{D1}$ and $-I_{D2}$ we obtain:

$$\frac{\mu_p C_{Ox}}{2} \frac{W}{L} \left( V_{IN} - V_{DD} - V_{Tp} \right)^2 = \mu_n C_{Ox} \frac{W}{L} \left( V_{IN} - V_{Tn} - \frac{V_{OUT}}{2} \right) V_{OUT}$$

valid for:

$$V_{GS1} \geq V_{Tn} \quad V_{DS1} < V_{GS1} - V_{Tn} \quad V_{GS2} \leq V_{Tp} \quad V_{DS2} \leq V_{GS2} - V_{T2}$$

thus, valid for:

$$V_{IN} \geq V_{Tn} \quad V_{OUT} < V_{IN} - V_{Tn} \quad V_{IN} - V_{DD} \leq V_{Tp} \quad V_{OUT} - V_{DD} \leq V_{IN} - V_{DD} - V_{Tp}$$
Transfer characteristics of the static CMOS inverter (Neglect $\lambda$ effects)

Case 2 $M_1$ triode, $M_2$ sat

\[ \begin{align*}
V_{\text{OUT}} - V_{\text{DD}} & \leq V_{\text{IN}} - V_{\text{DD}} - V_{\text{Tp}} \\
V_{\text{IN}} & \geq V_{\text{Tn}} \\
V_{\text{OUT}} & < V_{\text{IN}} - V_{\text{Tn}} \\
V_{\text{IN}} - V_{\text{DD}} & \leq V_{\text{Tp}}
\end{align*} \]
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

Case 2  $M_1$ triode, $M_2$ sat

\[ V_{\text{OUT}} - V_{DD} \leq V_{IN} - V_{DD} - V_{Tp} \]

\[ V_{IN} \geq V_{Tn} \]

\[ V_{OUT} < V_{IN} - V_{Tn} \]

\[ V_{IN} - V_{DD} \leq V_{Tp} \]
Transfer characteristics of the static CMOS inverter

Partial solution:
Transfer characteristics of the static CMOS inverter
(Neglect \(\lambda\) effects)

Case 3  \(M_1\) sat, \(M_2\) sat
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

Case 3 $M_1$ sat, $M_2$ sat

\[ I_{d1} = \frac{\mu_n C_{OXn}}{2} \frac{W_1}{L_1} (V_{IN} - V_{Tn})^2 \]

\[ I_{d2} = \frac{\mu_p C_{OXp}}{2} \frac{W_2}{L_2} (V_{IN} - V_{DD} - V_{Tp})^2 \]

Equating $I_{d1}$ and $-I_{d2}$ we obtain:

\[ \frac{\mu_p C_{OXp}}{2} \frac{W_2}{L_2} (V_{IN} - V_{DD} - V_{Tp})^2 = \frac{\mu_n C_{OXn}}{2} \frac{W_1}{L_1} (V_{IN} - V_{Tn})^2 \]

Which can be rewritten as:

\[ \sqrt{\frac{\mu_p C_{OXp}}{2} \frac{W_2}{L_2} (V_{DD} + V_{Tp} - V_{IN})} = \sqrt{\frac{\mu_n C_{OXn}}{2} \frac{W_1}{L_1} (V_{IN} - V_{Tn})} \]

Which can be simplified to:

\[ V_{IN} = \frac{(V_{Tn}) \sqrt{\frac{\mu_n C_{OXn}}{2} \frac{W_1}{L_1}} + (V_{DD} + V_{Tp}) \sqrt{\frac{\mu_p C_{OXp}}{2} \frac{W_2}{L_2}}}{\sqrt{\frac{\mu_n C_{OXn}}{2} \frac{W_1}{L_1}} + \sqrt{\frac{\mu_p C_{OXp}}{2} \frac{W_2}{L_2}}} \]

This is a vertical line
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

Case 3   $M_1$ sat, $M_2$ sat

$$V_{IN} = \frac{\left( V_{TN} \right) \left[ \frac{\mu n C_{Ox_n} W_1}{2 L_1} + \left( V_{DD} + V_{TP} \right) \frac{\mu p C_{Ox_p} W_2}{2 L_2} \right]}{\sqrt{\left[ \frac{\mu n C_{Ox_n} W_1}{2 L_1} + \frac{\mu p C_{Ox_p} W_2}{2 L_2} \right]}}$$

Since $C_{Ox_n} \approx C_{Ox_p} = C_{Ox}$ this can be simplified to:

$$V_{IN} = \frac{\left( V_{TN} \right) \left[ \frac{W_1}{L_1} + \left( V_{DD} + V_{TP} \right) \frac{W_2}{L_2} \right]}{\sqrt{\left[ \frac{W_1}{L_1} + \frac{W_2}{L_2} \right]}}$$

valid for:

$$V_{GS1} \geq V_{TN}$$
$$V_{DS1} \geq V_{GS1} - V_{TN}$$
$$V_{GS2} \leq V_{TP}$$
$$V_{DS2} \leq V_{GS2} - V_{T2}$$

thus, valid for:

$$V_{IN} \geq V_{TN}$$
$$V_{OUT} \geq V_{IN} - V_{TN}$$
$$V_{IN} - V_{DD} \leq V_{TP}$$
$$V_{OUT} - V_{DD} \leq V_{IN} - V_{DD} - V_{TP}$$
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

Case 3  $M_1$ sat, $M_2$ sat

\[
\begin{align*}
V_{\text{OUT}} & \leq V_{\text{IN}} - V_{\text{DD}} - V_{T_p} \\
V_{\text{IN}} & \geq V_{T_n} \\
V_{\text{OUT}} & \geq V_{\text{IN}} - V_{T_n} \\
V_{\text{IN}} - V_{\text{DD}} & \leq V_{T_p}
\end{align*}
\]
Transfer characteristics of the static CMOS inverter
(Neglect \lambda effects)

Case 3 \quad M_1 \text{ sat, } M_2 \text{ sat}

\begin{align*}
V_{\text{OUT}} - V_{\text{DD}} &\leq V_{\text{IN}} - V_{\text{DD}} - V_{\text{Tp}} \\
V_{\text{IN}} &\geq V_{\text{Tn}} \\
V_{\text{OUT}} &\geq V_{\text{IN}} - V_{\text{Tn}} \\
V_{\text{IN}} - V_{\text{DD}} &\leq V_{\text{Tp}}
\end{align*}
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

Partial solution:
Transfer characteristics of the static CMOS inverter
(Neglect \( \lambda \) effects)

Case 4 \( M_1 \) sat, \( M_2 \) triode
Transfer characteristics of the static CMOS inverter
(Neglect \( \lambda \) effects)

Case 4 \( M_1 \) sat, \( M_2 \) triode

\[
I_{D1} = \frac{\mu_n C_{Ox}}{2} \frac{W_1}{L_1} (V_{IN} - V_{Tn})^2
\]

\[
I_{D2} = -\mu_p C_{Oxp} \frac{W_2}{L_2} \left( V_{IN} - V_{DD} - V_{Tp} - \frac{V_{OUT} - V_{DD}}{2} \right) \cdot (V_{OUT} - V_{DD})
\]

Equating \( I_{D1} \) and \(-I_{D2}\) we obtain:

\[
\frac{\mu_n C_{Ox}}{2} \frac{W_1}{L_1} (V_{IN} - V_{Tn})^2 = \mu_p C_{Oxp} \frac{W_2}{L_2} \left( V_{IN} - V_{DD} - V_{Tp} - \frac{V_{OUT} - V_{DD}}{2} \right) \cdot (V_{OUT} - V_{DD})
\]

valid for:

\[
V_{GS1} \geq V_{Tn} \quad V_{DS1} \geq V_{GS1} - V_{Tn} \quad V_{GS2} \leq V_{Tp} \quad V_{DS2} > V_{GS2} - V_{T2}
\]

thus, valid for:

\[
V_{IN} \geq V_{Tn} \quad V_{OUT} \geq V_{IN} - V_{Tn} \quad V_{IN} - V_{DD} \leq V_{Tp} \quad V_{OUT} - V_{DD} > V_{IN} - V_{DD} - V_{Tp}
\]
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

Case 4 $M_1$ sat, $M_2$ triode

\[
V_{OUT} = \begin{cases} 
V_{DD} & V_{IN} \geq V_{Tn} \\
M_1 CO & V_{IN} - V_{DD} \leq V_Tp \\
M_2 CO & V_{OUT} - V_{DD} > V_{IN} - V_{DD} - V_Tp \\
M_2 TR & V_{OUT} \geq V_{IN} - V_{Tn} \\
M_2 SAT & V_{IN} - V_{DD} \leq V_Tp \\
M_1 TR & \end{cases}
\]
Transfer characteristics of the static CMOS inverter
(Neglect \( \lambda \) effects)

Case 4 \( M_1 \) sat, \( M_2 \) triode

\[
\begin{align*}
V_{OUT} & > V_{IN} - V_{DD} - V_{Tp} \\
V_{IN} & \geq V_{Tn} \\
V_{OUT} & \geq V_{IN} - V_{Tn} \\
V_{IN} - V_{DD} & \leq V_{Tp}
\end{align*}
\]
Transfer characteristics of the static CMOS inverter
(Neglect λ effects)

Partial solution:

\[
\begin{align*}
V_{DD} & \quad V_{DD} \\
VIN & \quad VOUT \\
-V_{Tp} & \quad VTn \\
V_{DD}+V_{Tp} & \quad V_{DD}
\end{align*}
\]
Transfer characteristics of the static CMOS inverter
(Neglect \( \lambda \) effects)

Case 4  \( M_1 \) cutoff, \( M_2 \) triode
Transfer characteristics of the static CMOS inverter  
(Neglect $\lambda$ effects)

**Case 5**  $M_1$ cutoff, $M_2$ triode

$I_{d1} = 0$

$I_{d2} = -\mu_p C_{oxp} \frac{W_2}{L_2} \left(V_{IN} - V_{DD} - V_{TP} - \frac{V_{OUT} - V_{DD}}{2}\right) \bullet (V_{OUT} - V_{DD})$

Equating $I_{d1}$ and $-I_{d2}$ we obtain:

$$\mu_p C_{oxp} \frac{W_2}{L_2} \left(V_{IN} - V_{DD} - V_{TP} - \frac{V_{OUT} - V_{DD}}{2}\right) \bullet (V_{OUT} - V_{DD}) = 0$$

valid for:

$$V_{GS1} < V_{TN} \quad V_{GS2} \leq V_{TP} \quad V_{DS2} > V_{GS2} - V_{T2}$$

thus, valid for:

$$V_{IN} < V_{TN} \quad V_{IN} - V_{DD} \leq V_{TP} \quad V_{OUT} - V_{DD} > V_{IN} - V_{DD} - V_{TP}$$
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

Case 5  $M_1$ cutoff, $M_2$ triode

\[ V_{OUT} \]

\[ V_{DD} \]

\[ V_{Tn} \]

\[ V_{IN} \]

\[ V_{TP} \]

\[ V_{OUT} - V_{DD} > V_{IN} - V_{DD} - V_{TP} \]

\[ V_{IN} < V_{Tn} \]

\[ V_{IN} - V_{DD} \leq V_{TP} \]
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

Case 5 $M_1$ cutoff, $M_2$ triode

$V_{OUT}$

$V_{DD}$

$-V_{Tp}$

$V_{IN}$

$V_{Tn}$

$V_{IN} - V_{DD} \leq V_{Tp}$

$V_{OUT} - V_{DD} > V_{IN} - V_{DD} - V_{Tp}$

$V_{IN} < V_{Tn}$

$V_{DD}$

$V_{DD} + V_{Tp}$

(Neglect $\lambda$ effects)
Transfer characteristics of the static CMOS inverter (Neglect λ effects)
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)
Transfer characteristics of the static CMOS inverter
(Neglect \( \lambda \) effects)

From Case 3 analysis:

\[
V_{IN} = \frac{(V_{Tn}) + (V_{DD} + V_{Tp})}{\sqrt{\frac{\mu_p}{\mu_n} \frac{W_2}{W_1} \frac{L_1}{L_2}}} \left(1 + \sqrt{\frac{\mu_p}{\mu_n} \frac{W_2}{W_1} \frac{L_1}{L_2}}\right)
\]
Inverter Transfer Characteristics of Inverter Pair

What are $V_H$ and $V_L$?

Find the points on the inverter pair transfer characteristics where $V_{OUT}'=V_{IN}$ and the slope is less than 1.
Inverter Transfer Characteristics of Inverter Pair for **THIS** Logic Family

\[ V_{IN} \xrightarrow{\text{M}1} V'_{OUT} \xrightarrow{\text{M}2} V_{OUT} \]

\[ V_H = V_{DD} \quad \text{and} \quad V_L = 0 \]

Note this is independent of device sizing for THIS logic family!!
Sizing of the Basic CMOS Inverter

The characteristic that device sizes do not need to be used to establish $V_H$ and $V_L$ logic levels is a major advantage of this type of logic.

How should $M_1$ and $M_2$ be sized?

How many degrees of freedom are there in the design of the inverter?
How should $M_1$ and $M_2$ be sized?

How many degrees of freedom are there in the design of the inverter?

$$\{ W_1, W_2, L_1, L_2 \}$$

4 degrees of freedom

But in basic device model and in most performance metrics, $W_1/L_1$ and $W_2/L_2$ appear as ratios

$$\{ \frac{W_1}{L_1}, \frac{W_2}{L_2} \}$$

effectively 2 degrees of freedom
How should $M_1$ and $M_2$ be sized?

\[ \{ W_1, W_2, L_1, L_2 \} \] 4 degrees of freedom

Usually pick $L_1 = L_2 = L_{\text{min}}$

\[ \{ W_1/L_1, W_2/L_2 \} \] effectively 2 degrees of freedom

How are $W_1$ and $W_2$ chosen?

Depends upon what performance parameters are most important for a given application!
How should $M_1$ and $M_2$ be sized?

![Circuit Diagram]

One popular sizing strategy:
1. Pick $W_1 = W_{\text{MIN}}$ to minimize area of $M_1$
2. Pick $W_2$ to set trip-point at $V_{\text{DD}}/2$

Usually pick $L_1 = L_2 = L_{\text{min}}$

$\{ \frac{W_1}{L_1}, \frac{W_2}{L_2} \}$ 2 remaining degrees of freedom
How should $M_1$ and $M_2$ be sized?

pick $L_1=L_2=L_{\text{min}}$

One popular sizing strategy:
1. Pick $W_1=W_{\text{MIN}}$ to minimize area of $M_1$
2. Pick $W_2$ to set trip-point at $V_{DD}/2$

Observe Case 3 provides expression for $V_{\text{TRIP}}$

Thus, at the trip point,

$$V_{\text{OUT}} = V_{\text{IN}} = V_{\text{TRIP}} = \left( V_{Tn} \right) + \left( V_{DD} + V_{Tp} \right) \frac{\sqrt{\mu_p W_2 L_1}}{\sqrt{\mu_n W_1 L_2}} \times \frac{1}{1 + \sqrt{\frac{\mu_p W_2 L_1}{\mu_n W_1 L_2}}}$$
How should $M_1$ and $M_2$ be sized?

pick $L_1=L_2=L_{\text{min}}$

One popular sizing strategy:
1. Pick $W_1=W_{\text{MIN}}$ to minimize area of $M_1$
2. Pick $W_2$ to set trip-point at $V_{\text{DD}}/2$

Typically $V_{Tn}=0.2V_{\text{DD}}$, $|V_{Tp}|=0.2V_{\text{DD}}$

$$V_{\text{TRIP}} = \frac{(V_{Tn}) + (V_{DD} + V_{Tp}) \sqrt{\frac{\mu_p}{\mu_n}} \frac{W_2}{L_1}}{1 + \sqrt{\frac{\mu_p}{\mu_n}} \frac{W_2}{L_1}}$$

$$\therefore \quad \frac{V_{DD}}{2} = \frac{(0.2V_{DD}) + (V_{DD} - 0.2V_{DD}) \sqrt{\frac{\mu_p}{\mu_n}} \frac{W_2}{L_1}}{1 + \sqrt{\frac{\mu_p}{\mu_n}} \frac{W_2}{L_1}}$$

Solving this equation for $W_2$, obtain

$$W_2 = W_1 \left( \frac{\mu_n}{\mu_p} \right)$$

Other sizing strategies are used as well and will be discussed later!
Extension of Basic CMOS Inverter to Multiple-Input Gates

Performs as a 2-input NOR Gate

Can be easily extended to an n-input NOR Gate
Extension of Basic CMOS Inverter to Multiple-Input Gates

Performs as a 2-input NAND Gate

Can be easily extended to an n-input NAND Gate
Static CMOS Logic Family

Observe PUN is p-channel, PDN is n-channel
Static CMOS Logic Family

n-channel PDN and p-channel PUN
$V_H = V_{DD}$, $V_L = 0V$ (same as for inverter!)
General Logic Family

Compound Gate in CMOS Process

- p-channel PUN
- n-channel PDN

\[ V_H = V_{DD}, \quad V_L = 0V \] (same as for inverter!)

Arbitrary PUN and PDN
Other CMOS Logic Families

Enhancement Load NMOS

Enhancement Load Pseudo-NMOS

Depletion Load NMOS
End of Lecture 36