Digital Circuits

- Transfer Characteristics of the Inverter Pair
- One device sizing strategy
- Multiple-input gates
The basic logic gates

It suffices to characterize the inverter of a logic family and then express the performance of other gates in that family in terms of the performance of the inverter.

What characteristics are required and desirable for an inverter to form the basis for a useful logic family?
What are the logic levels for a given inverter of for a given logic family?

\[ V_H = ? \quad V_L = ? \]

Can we legislate them?

- Some authors choose to define them based upon specific features of inverter
- Analytical expressions may be complicated
- But what if the circuit does not interpret them the same way they are defined!!
What are the logic levels for a given inverter of for a given logic family?

Ask the inverter how it will interpret logic levels
• The inverter will interpret them the way the circuit really operate as a Boolean system !!
• Analytical expressions may be complicated
• How is this determination made?
Ask the inverter how it will interpret logic levels

Consider a very long cascade of inverters
Apply a large voltage at the input (alternatively a small input could be used)
w.l.o.g. assume an even number of inverters in chain indicated
Ask the inverter how it will interpret logic levels

\[ V_{\text{H}}=? \]
\[ V_{\text{L}}=? \]

Consider a very long cascade of inverters

Apply a large voltage at the input (alternatively a small input could be used)

w.l.o.g. assume an even number of inverters in chain indicated

If logic levels are to be maintained, the voltage at the end of this even number of stages must be \( V_{\text{H}} \), that of the next must be \( V_{\text{L}} \), the next \( V_{\text{H}} \), etc. until the start of the cascade is approached
Ask the inverter how it will interpret logic levels

V_IN → V_OUT

V_H = ?

V_L = ?

V_IN → Voffee

V_LARGE

V_H

V_L

V_H
Ask the inverter how it will interpret logic levels

VH=?
VL=?
Ask the inverter how it will interpret logic levels

\[ V_H = \] ?
\[ V_L = \] ?

- Two inverter loop
- Very useful circuit!
The two-inverter loop

SRAM Cell

S₂ often eliminated (shorted)
The two-inverter loop

S\_2 \text{ often eliminated} \ (\text{shorted})

Standard 6-transistor SRAM Cell
Ask the inverter how it will interpret logic levels

Thus, consider the inverter pair
Ask the inverter how it will interpret logic levels

Inverter pair

$V_H$ and $V_L$ will be on the intersection of the transfer characteristics of the inverter pair (IPTC) and the $V'_{OUT}=V_{IN}$ line

$V_H$ and $V_L$ often termed the “1” and “0” states
Ask the inverter how it will interpret logic levels

Inverter pair

When $V_{OUT} = V_{IN}$, $V_H$ and $V_L$ are stable operating points, $V_{TRIP}$ is a quasi-stable operating point

Observe: slope of IPTC is greater than 1 at $V_{TRIP}$ and less than 1 at $V_H$ and $V_L$
When $V_{\text{OUT}} = V_{\text{IN}}$ for the inverter, $V'_{\text{OUT}}$ is also equal to $V_{\text{IN}}$. Thus the intersection point for $V_{\text{OUT}} = V_{\text{IN}}$ in the inverter transfer characteristics (ITC) is also an intersection point for $V'_{\text{OUT}} = V_{\text{IN}}$ in the inverter-pair transfer characteristics (IPTC).

Implication: Inverter characteristics can be used directly to obtain $V_{\text{TRIP}}$. 
Logic Family Characteristics

What properties of an inverter are necessary for it to be useful for building a two-level logic family?

The inverter-pair transfer characteristics must have three unique intersection points with the $V'_{\text{OUT}} = V_{\text{IN}}$ line.

What are the logic levels for a given inverter of for a given logic family?

The two extreme intersection points of the inverter-pair transfer characteristics with the $V'_{\text{OUT}} = V_{\text{IN}}$ line.

Can we legislate $V_H$ and $V_L$ for a logic family? No!

What other properties of the inverter are desirable?

Reasonable separation between $V_H$ and $V_L$ (enough separation so that noise does not cause circuit to interpret level incorrectly)

$$V_{\text{TRIP}} \approx \frac{V_H + V_L}{2}$$

(to provide adequate noise immunity and process insensitivity)
What happens near the quasi-stable operating point?

$S_2$ closed and $X = Y = V_{TRIP}$
What happens near the quasi-stable operating point?

S₂ closed and X=Y=V_{TRIP}

If X decreases even very slightly, will move to the X=0, Y=1 state (very fast)

If X increases even very slightly, will move to the X=1, Y=0 state (very fast)
What if the inverter pair had the following transfer characteristics?
What if the inverter pair had the following transfer characteristics?

Multiple levels of logic
Every intersection point with slope <1 is a stable point
Every intersection point with slope >1 is a quasi-stable point
What are the transfer characteristics of the static CMOS inverter pair?

Consider first the inverter

\[ V_{\text{IN}} \rightarrow \text{Inverter} \rightarrow V'_{\text{OUT}} \]

\[ V_{\text{IN}} \rightarrow \text{Inverter} \rightarrow V_{\text{OUT}} \]
Transfer characteristics of the static CMOS inverter
Transfer characteristics of the static CMOS inverter
(Neglect λ effects)

Case 1  $M_1$ triode, $M_2$ cutoff

$$I_{D1} = \mu_n C_{oxn} \frac{W_1}{L_1} \left( V_{IN} - V_{Tn} - \frac{V_{OUT}}{2} \right) V_{OUT}$$

$$I_{D2} = 0$$

Equating $I_{D1}$ and $-I_{D2}$ we obtain:

$$0 = \mu_n C_{oxn} \frac{W_1}{L_1} \left( V_{IN} - V_{Tn} - \frac{V_{OUT}}{2} \right) V_{OUT}$$

It can be shown that setting the first product term to 0 will not verify, thus

$$V_{OUT} = 0$$

valid for:

$$V_{GS1} \geq V_{Tn} \quad V_{DS1} < V_{GS1} - V_{Tn} \quad V_{GS2} \geq V_{Tp}$$

thus, valid for:

$$V_{IN} \geq V_{Tn} \quad V_{OUT} < V_{IN} - V_{Tn} \quad V_{IN} - V_{DD} \geq V_{Tp}$$
Graphical Interpretation of these conditions:

\[ V_{IN} \geq V_{Tn} \quad V_{OUT} < V_{IN} - V_{Tn} \quad V_{IN} - V_{DD} \geq V_{Tp} \]
Transfer characteristics of the static CMOS inverter
(Neglect \( \lambda \) effects)

Case 1 \( M_1 \) triode, \( M_2 \) cutoff

\[ V_{\text{OUT}} = 0 \]
Transfer characteristics of the static CMOS inverter
(Neglect λ effects)

Case 1 \( M_1 \) triode, \( M_2 \) cutoff

\( V_{\text{OUT}} = 0 \)
Transfer characteristics of the static CMOS inverter
(Neglect λ effects)
Partial solution:
Transfer characteristics of the static CMOS inverter (Neglect $\lambda$ effects)

Case 2 $M_1$ triode, $M_2$ sat
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

Case 1  $M_1$ triode, $M_2$ cutoff

$V_{\text{OUT}} = 0$
Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

Partial solution:
Regions of Operation for Devices in CMOS inverter

- $V_{DD}$
- $V_{IN}$
- $V_{OUT}$
- $M_1$
- $M_2$
- $V_{DD}$
- $V_{DD} + V_{Tp}$
- $-V_{Tp}$
- $-V_{Tn}$
- $M_1\text{CO}$
- $M_2\text{CO}$
- $M_2\text{TR}$
- $M_1\text{TR}$
- $M_2\text{SAT}$
- $M_1\text{SAT}$
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

Case 2 $M_1$ triode, $M_2$ sat

![Diagram of transfer characteristics of a static CMOS inverter showing $V_{OUT}$ vs $V_{IN}$ with $V_{DD}$ and $-V_{Tp}$ axes, and labels for $M_1CO$, $M_2TR$, $M_2CO$, $M_1SAT$, $M_2SAT$, $V_{DD}$, $V_{DD} + V_{Tp}$, $V_{TN}$, and $V_{TP}$.]
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

**Case 2**  $M_1$ triode, $M_2$ sat

$$I_{D1} = \mu_n C_{Ox_n} \frac{W_1}{L_1} \left( V_{IN} - V_{Tn} - \frac{V_{OUT}}{2} \right) V_{OUT}$$

$$I_{D2} = -\frac{\mu_p C_{Ox_p}}{2} \frac{W_2}{L_2} \left( V_{IN} - V_{DD} - V_{Tp} \right)^2$$

Equating $I_{D1}$ and $-I_{D2}$ we obtain:

$$\frac{\mu_p C_{Ox_p}}{2} \frac{W_2}{L_2} \left( V_{IN} - V_{DD} - V_{Tp} \right)^2 = \mu_n C_{Ox_n} \frac{W_1}{L_1} \left( V_{IN} - V_{Tn} - \frac{V_{OUT}}{2} \right) V_{OUT}$$

valid for:

$$V_{GS1} \geq V_{Tn} \quad V_{DS1} < V_{GS1} - V_{Tn} \quad V_{GS2} \leq V_{Tp} \quad V_{DS2} \leq V_{GS2} - V_{T2}$$

thus, valid for:

$$V_{IN} \geq V_{Tn} \quad V_{OUT} < V_{IN} - V_{Tn} \quad V_{IN} - V_{DD} \leq V_{Tp} \quad V_{OUT} - V_{DD} \leq V_{IN} - V_{DD} - V_{Tp}$$
Transfer characteristics of the static CMOS inverter
(Neglect λ effects)

Case 2  \( M_1 \) triode, \( M_2 \) sat

\[
\begin{align*}
V_{OUT} - V_{DD} & \leq V_{IN} - V_{DD} - V_{Tp} \\
V_{IN} & \geq V_{Tn} \\
V_{OUT} & < V_{IN} - V_{Tn} \\
V_{IN} - V_{DD} & \leq V_{Tp}
\end{align*}
\]
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

Case 2  $M_1$ triode, $M_2$ sat

\[
\begin{align*}
V_{\text{OUT}} - V_{\text{DD}} & \leq V_{\text{IN}} - V_{\text{DD}} - V_{T_p} \\
V_{\text{IN}} & \geq V_{T_n} \\
V_{\text{OUT}} & < V_{\text{IN}} - V_{T_n} \\
V_{\text{IN}} - V_{\text{DD}} & \leq V_{T_p}
\end{align*}
\]
Transfer characteristics of the static CMOS inverter

Partial solution:
Transfer characteristics of the static CMOS inverter (Neglect $\lambda$ effects)

Case 3 \( M_1 \) sat, \( M_2 \) sat
Transfer characteristics of the static CMOS inverter
(Neglect \( \lambda \) effects)

Case 3 \( M_1 \) sat, \( M_2 \) sat

\[
I_{d1} = \frac{\mu_n C_{Ox}}{2} \frac{W_1}{L} (V_{IN} - V_{Tn})^2
\]
\[
I_{d2} = \frac{\mu_p C_{Ox}}{2} \frac{W_2}{L} (V_{IN} - V_{DD} - V_{Tp})^2
\]

Equating \( I_{d1} \) and \(-I_{d2}\) we obtain:

\[
\frac{\mu_p C_{Ox}}{2} \frac{W_2}{L} (V_{IN} - V_{DD} - V_{Tp})^2 = \frac{\mu_n C_{Ox}}{2} \frac{W_1}{L} (V_{IN} - V_{Tn})^2
\]

Which can be rewritten as:

\[
\sqrt{\frac{\mu_p C_{Ox}}{2} \frac{W_2}{L} (V_{DD} + V_{Tp} - V_{IN})} = \sqrt{\frac{\mu_n C_{Ox}}{2} \frac{W_1}{L} (V_{IN} - V_{Tn})}
\]

Which can be simplified to:

\[
V_{IN} = \frac{(V_{Tn}) \sqrt{\frac{\mu_n C_{Ox}}{2} \frac{W_1}{L} + (V_{DD} + V_{Tp}) \sqrt{\frac{\mu_p C_{Ox}}{2} \frac{W_2}{L}}}}{\sqrt{\frac{\mu_n C_{Ox}}{2} \frac{W_1}{L} + \sqrt{\frac{\mu_p C_{Ox}}{2} \frac{W_2}{L}}}}
\]
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

Case 3  $M_1$ sat, $M_2$ sat

$$V_{IN} = \frac{(V_{Tn}) \sqrt{\frac{\mu n C_{Ox} W_1}{2 L_1}} + (V_{DD} + V_{Tp}) \sqrt{\frac{\mu p C_{Ox} W_2}{2 L_2}}}{\sqrt{\frac{\mu n C_{Ox} W_1}{2 L_1}} + \sqrt{\frac{\mu p C_{Ox} W_2}{2 L_2}}}$$

Since $C_{Ox} = C_{Ox} = C_{Ox}$ this can be simplified to:

$$V_{IN} = \frac{(V_{Tn}) \sqrt{\frac{W_1}{L_1}} + (V_{DD} + V_{Tp}) \sqrt{\frac{\mu p W_2}{\mu n L_2}}}{\sqrt{\frac{W_1}{L_1}} + \sqrt{\frac{\mu p W_2}{\mu n L_2}}}$$

valid for:

$$V_{GS1} \geq V_{Tn} \quad V_{DS1} \geq V_{GS1} - V_{Tn} \quad V_{GS2} \leq V_{Tp} \quad V_{DS2} \leq V_{GS2} - V_{T2}$$

thus, valid for:

$$V_{IN} \geq V_{Tn} \quad V_{OUT} \geq V_{IN} - V_{Tn} \quad V_{IN} - V_{DD} \leq V_{Tp} \quad V_{OUT} - V_{DD} \leq V_{IN} - V_{DD} - V_{Tp}$$
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

Case 3  $M_1$ sat, $M_2$ sat

$$V_{OUT} - V_{DD} \leq V_{IN} - V_{DD} - V_{Tp}$$

$$V_{IN} \geq V_{Tn}$$

$$V_{OUT} \geq V_{IN} - V_{Tn}$$

$$V_{IN} - V_{DD} \leq V_{Tp}$$
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

Case 3  $M_1$ sat, $M_2$ sat

\[
V_{OUT} - V_{DD} \leq V_{IN} - V_{DD} - V_{Tp}
\]
\[
V_{IN} \geq V_{Tn}
\]
\[
V_{OUT} \geq V_{IN} - V_{Tn}
\]
\[
V_{IN} - V_{DD} \leq V_{Tp}
\]
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

Partial solution:
Transfer characteristics of the static CMOS inverter
(Neglect \( \lambda \) effects)

Case 4 \( M_1 \) sat, \( M_2 \) triode
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

**Case 4** $M_1$ sat, $M_2$ triode

$$I_{D1} = \frac{\mu_n C_{oXn}}{2} \frac{W_1}{L} (V_{in} - V_{Tn})^2$$

$$I_{D2} = -\mu_p C_{oXp} \frac{W_2}{L_2} \left( V_{in} - V_{DD} - V_{Tp} - \frac{V_{OUT} - V_{DD}}{2} \right) \cdot (V_{OUT} - V_{DD})$$

Equating $I_{D1}$ and $-I_{D2}$ we obtain:

$$\frac{\mu_n C_{oXn}}{2} \frac{W_1}{L_1} (V_{in} - V_{Tn})^2 = \mu_p C_{oXp} \frac{W_2}{L_2} \left( V_{in} - V_{DD} - V_{Tp} - \frac{V_{OUT} - V_{DD}}{2} \right) \cdot (V_{OUT} - V_{DD})$$

valid for:

$$V_{GS1} \geq V_{Tn} \quad V_{DS1} \geq V_{GS1} - V_{Tn} \quad V_{GS2} \leq V_{Tp} \quad V_{DS2} > V_{GS2} - V_{T2}$$

thus, valid for:

$$V_{in} \geq V_{Tn} \quad V_{OUT} \geq V_{IN} - V_{Tn} \quad V_{IN} - V_{DD} \leq V_{Tp} \quad V_{OUT} - V_{DD} > V_{IN} - V_{DD} - V_{Tp}$$
Transfer characteristics of the static CMOS inverter
(Neglect \( \lambda \) effects)

Case 4 \( M_1 \) sat, \( M_2 \) triode

\[
\begin{align*}
V_{\text{OUT}} &> V_{\text{IN}} - V_{\text{DD}} - V_{T_p} \\
V_{\text{IN}} &\geq V_{T_n} \\
V_{\text{OUT}} &\geq V_{\text{IN}} - V_{T_n} \\
V_{\text{IN}} - V_{\text{DD}} &\leq V_{T_p}
\end{align*}
\]
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

Case 4  $M_1$ sat, $M_2$ triode

\[ V_{OUT} - V_{DD} > V_{IN} - V_{DD} - V_{Tp} \]

\[ V_{IN} \geq V_{Tn} \]

\[ V_{OUT} \geq V_{IN} - V_{Tn} \]

\[ V_{IN} - V_{DD} \leq V_{Tp} \]
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

Partial solution:
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

Case 4  $M_1$ cutoff, $M_2$ triode
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

Case 5  $M_1$ cutoff, $M_2$ triode

$I_{d1} = 0$

$I_{d2} = -\mu_p C_{OXP} \frac{W}{L_2} \left( V_{IN} - V_{DD} - V_{TP} - \frac{V_{OUT} - V_{DD}}{2} \right) \cdot (V_{OUT} - V_{DD})$

Equating $I_{d1}$ and $-I_{d2}$ we obtain:

$\mu_p C_{OXP} \frac{W}{L_2} \left( V_{IN} - V_{DD} - V_{TP} - \frac{V_{OUT} - V_{DD}}{2} \right) \cdot (V_{OUT} - V_{DD}) = 0$

valid for:

$V_{GS1} < V_{Tn}$  $V_{GS2} \leq V_{TP}$  $V_{DS2} > V_{GS2} - V_{T2}$

thus, valid for:

$V_{IN} < V_{Tn}$  $V_{IN} - V_{DD} \leq V_{TP}$  $V_{OUT} - V_{DD} > V_{IN} - V_{DDL} - V_{TP}$
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

Case 5  $M_1$ cutoff, $M_2$ triode
Transfer characteristics of the static CMOS inverter
(Neglect \( \lambda \) effects)

Case 5 \( M_1 \) cutoff, \( M_2 \) triode
Transfer characteristics of the static CMOS inverter
(Neglect λ effects)
Transfer characteristics of the static CMOS inverter

(Neglect $\lambda$ effects)
Transfer characteristics of the static CMOS inverter

(Neglect \( \lambda \) effects)

From Case 3 analysis:

\[
V_{IN} = \frac{(V_{Tn}) + (V_{DD} + V_{Tp}) \sqrt{\frac{\mu_p}{\mu_n} \frac{W_2}{W_1} \frac{L_1}{L_2}}}{1 + \sqrt{\frac{\mu_p}{\mu_n} \frac{W_2}{W_1} \frac{L_1}{L_2}}}
\]
Inverter Transfer Characteristics of Inverter Pair

What are $V_H$ and $V_L$?

Find the points on the inverter pair transfer characteristics where $V_{OUT}'=V_{IN}$ and the slope is less than 1
Inverter Transfer Characteristics of Inverter Pair for THIS Logic Family

\[ V_{IN} \rightarrow V'_{OUT} \]

\[ V'_{OUT} \]

\[ V_H = V_{DD} \text{ and } V_L = 0 \]

Note this is independent of device sizing for THIS logic family!!
Sizing of the Basic CMOS Inverter

The characteristic that device sizes do not need to be used to establish $V_H$ and $V_L$ logic levels is a major advantage of this type of logic.

How should $M_1$ and $M_2$ be sized?

How many degrees of freedom are there in the design of the inverter?
How should \( M_1 \) and \( M_2 \) be sized?

How many degrees of freedom are there in the design of the inverter?

\[
\{ W_1, W_2, L_1, L_2 \} \quad \text{4 degrees of freedom}
\]

But in basic device model and in most performance metrics, \( W_1/L_1 \) and \( W_2/L_2 \) appear as ratios

\[
\{ W_1/L_1, W_2/L_2 \} \quad \text{effectively 2 degrees of freedom}
\]
How should $M_1$ and $M_2$ be sized?

$\{ W_1, W_2, L_1, L_2 \}$  \hspace{1cm} 4 degrees of freedom \hspace{1cm} Usually pick $L_1 = L_2 = L_{\text{min}}$

$\{ W_1/L_1, W_2/L_2 \}$ \hspace{1cm} effectively 2 degrees of freedom

How are $W_1$ and $W_2$ chosen?

Depends upon what performance parameters are most important for a given application!
How should $M_1$ and $M_2$ be sized?

Usually pick $L_1= L_2= L_{\text{min}}$

\{ $W_1/L_1, W_2/L_2$ \} 2 remaining degrees of freedom

One popular sizing strategy:
1. Pick $W_1= W_{\text{MIN}}$ to minimize area of $M_1$
2. Pick $W_2$ to set trip-point at $V_{DD}/2$
How should $M_1$ and $M_2$ be sized?

pick $L_1=L_2=L_{\text{min}}$

One popular sizing strategy:

1. Pick $W_1=W_{\text{MIN}}$ to minimize area of $M_1$
2. Pick $W_2$ to set trip-point at $V_{DD}/2$

Observe Case 3 provides expression for $V_{\text{TRIP}}$

Thus, at the trip point,

$$V_{\text{OUT}} = V_{\text{IN}} = V_{\text{TRIP}} = \frac{(V_{Tn}) + (V_{DD} + V_{Tp}) \sqrt{\mu_p W_2 L_1}}{1 + \sqrt{\mu_n W_1 L_2}}$$
How should $M_1$ and $M_2$ be sized?

pick $L_1=L_2=L_{\text{min}}$

One popular sizing strategy:
1. Pick $W_1=W_{\text{MIN}}$ to minimize area of $M_1$
2. Pick $W_2$ to set trip-point at $V_{DD}/2$

Typically $V_{Tn}=0.2V_{DD}$, $|V_{Tp}|=0.2V_{DD}$

$$V_{\text{TRIP}} = \frac{(V_{Tn}) + (V_{DD} + V_{Tp})}{1 + 1 + \sqrt{\frac{\mu_p}{\mu_n}} \frac{W_2}{L_1} \frac{1}{W_1 L_2}}$$

$\therefore$ $V_{DD} = \frac{0.2V_{DD} + (V_{DD} - 0.2V_{DD})}{1 + \frac{\mu_p}{\mu_n} \frac{W_2}{W_1}}$

Solving this equation for $W_2$, obtain

$$W_2 = W_1 \left( \frac{\mu_n}{\mu_p} \right)$$

Other sizing strategies are used as well and will be discussed later!
End of Lecture 36