EE 330
Lecture 36

Digital Circuit Design

• Basic Logic Gates
• Properties of Logic Families
• Characterization of CMOS Inverter
• One device sizing strategy
• Multiple-input gates
Exam 3  Friday April  13

Review session: Thursday 6pm
Review from Last Lecture

Formalization of cascade circuit analysis working from load to input:

\[
\frac{V_{OUT}}{V_{IN}} = \frac{V_1}{V_{IN}} \cdot \frac{V_2}{V_1} \cdot \frac{V_3}{V_2} \cdot \frac{V_{OUT}}{V_3}
\]

\(R_{in}\) includes effects of all loading
Must recalculate if any change in loading
Analysis systematic and rather simple
This gain is very large!
And no design parameters affect the gain
Current Sources/Mirrors

Review from Last Lecture

Biasing Circuit

Key Block

Current Sink
Current Sources/Mirrors Summary

Review from Last Lecture

npn Current Mirror

$$I_{out} = \left[ \frac{A_{E1}}{A_{E0}} \right] I_{in}$$

n-channel Current Mirror

$$I_{out} = \left[ \frac{W_1}{W_0 \frac{L_0}{L_1}} \right] I_{in}$$
Layout of Current Mirrors

Example with $M = 2$

Standard layout

Better layout

Even better layout

This is termed a common-centroid layout
High-gain amplifier

\[ A_V = \frac{-g_m}{g_0} \]

\[ A_V = \frac{-g_{m1}}{g_{01} + g_{02}} \approx \frac{-g_{m1}}{2g_{01}} \]
End of basic analog

Start of basic digital
Hierarchical Design
Basic Logic Gates
Properties of Logic Families
Characterization of CMOS Inverter
Static CMOS Logic Gates
  – Ratio Logic
Propagation Delay
  – Simple analytical models
  – Elmore Delay
Sizing of Gates

Propagation Delay with Multiple Levels of Logic
Optimal driving of Large Capacitive Loads
Power Dissipation in Logic Circuits
Other Logic Styles
Array Logic
Ring Oscillators
Hierarchical Digital Design Domains:

- Behavioral:
- Structural:
- Physical

Multiple Levels of Abstraction
Hierarchical Digital Design Domains:

Multiple Sublevels in Each Major Level
All Design Steps may not Fit Naturally in this Description
Hierarchical Digital Design Domains:

**Behavioral**: Describes what a system does or what it should do

**Structural**: Identifies constituent blocks and describes how these blocks are interconnected and how they interact

**Physical**: Describes the constituent blocks to both the transistor and polygon level and their physical placement and interconnection

Multiple representations often exist at any level or sublevel
Example: Two distinct representations at the physical level (polygon sublevel)
Example: Two distinct representations at physical level (schematic sublevel)

\[ \frac{W}{L} = 4 \]

- \[ W = 4 \mu \]
  - \[ L = 1 \mu \]
- \[ W = 8 \mu \]
  - \[ L = 2 \mu \]

\[ W_1, L \]
\[ W_2, L \]
\[ W_1 + W_2, L \]
Example: Two distinct representations at the structural/behavioral level (gate sublevel)

\[ C = A \oplus B \]
In each domain, multiple levels of abstraction are generally used.

Consider Physical Domain

– Consider lowest level to highest

0 - placement of diffusions, thin oxide regions, field oxide, etc. on a substrate.
1 - polygons identify all mask information (not unique)
2 - transistors (not unique)
3 - gate level (not unique)
4 - cell level
   Adders, Flip Flop, MUTs,…
Structural Level:

- DSP
- Blocks (Adders, Memory, Registers, etc.)
- Gates
- Transistor

Information Type

HDL
Netlists
Behavior Level (top down):

- Application
- Programs
- Subroutines
- Boolean Expressions

Information Type
High-Level Language
HDL
Representation of Digital Systems

Standard Approach to Digital Circuit Design

8 – level representation

1. Behavioral Description
   – Technology independent

2. RTL Description (Register Transfer Level)
   (must verify (1) ⇔ (2))

3. RTL Compiler
   Registers and Combinational Logic Functions

4. Logic Optimizer

5. Logic Synthesis
   Generally use a standard call library for synthesis

(sublevels 6-8 not shown on this slide)
1. Behavioral Description
   - Technology independent
2. RTL Description
   (must verify (1) \iff (2))
3. RTL Compiler
   Registers and Combinational Logic Functions
4. Logic Optimizer
5. Logic Synthesis
   Generally use a standard call library for synthesis
6. Place and Route

(physically locates all gates and registers and interconnects them)

7. Layout Extraction
   • DRC
   • Back Annotation

8. Post Layout simulation

May necessitate a return to a higher level in the design flow

Logic synthesis, though extensively used, often is not as efficient nor as optimal for implementing some important blocks or some important functions

These applications generally involve transistor level logic circuit design that may combine one or more different logic design styles
Logic Optimization

What is optimized (or minimized)?

- Number of Gates
- Number or Levels of Logic
- Speed
- Delay
- Power Dissipation
- Area
- Cost
- Peak Current
  
Depends Upon What User Is Interested In
Digital Circuit Design

- Hierarchical Design
- Basic Logic Gates
- Properties of Logic Families
- Characterization of CMOS Inverter
- Static CMOS Logic Gates
  - Ratio Logic
- Propagation Delay
  - Simple analytical models
  - Elmore Delay
- Sizing of Gates

- Propagation Delay with Multiple Levels of Logic
- Optimal driving of Large Capacitive Loads
- Power Dissipation in Logic Circuits
- Other Logic Styles
- Array Logic
- Ring Oscillators
Logic Circuit Block Design

Many different logic design styles

• Static Logic Gates
• Complex Logic Gates
• Pseudo NMOS
• Pass Transistor Logic
• Dynamic Logic Gates
  • Domino Logic
  • Zipper Logic
  • Output Prediction Logic

Various logic design styles often combined in the implementation of one logic block
The basic logic gates

X  Y  Y = \overline{X}
X  Y  Y = X
A  B  Y = A + B
A  B  Y = A \cdot B
A  B  Y = \overline{A + B}
A  B  Y = \overline{A \cdot B}
A  B  Y = A \oplus B
A  B  Y = \overline{A \oplus B}

A  B  AOI  Y = A \cdot B + C \cdot D
A  B  OAI  Y = (A + B) \cdot (C + D)
A  B  Y = A_1 + A_2 + \ldots A_n
A  B  Y = A_1 \cdot A_2 \cdot \ldots A_n

Question: How many basic gates exist and how many of these are useful?
The set of NOR gates is complete
Any combinational logic function can be realized with only multiple-input NOR gates

The set of NAND gates is complete
Any combinational logic function can be realized with only multiple-input NOR gates

Performance of the BASIC gates is critical!
The basic logic gates

It suffices to characterize the inverter of a logic family and then express the performance of other gates in that family in terms of the performance of the inverter.

What characteristics are required and desirable for an inverter to form the basis for a useful logic family?
Desirable and/or Required Logic Family Characteristics

1. High and low logic levels must be uniquely distinguishable (even in a long cascade)
2. Capable of driving many loads (good fanout)
3. Fast transition times (but in some cases, not too fast)
4. Good noise margins (low error probabilities)
5. Small die area
6. Low power consumption
7. Economical process requirements
Desirable and/or Required Logic Family Characteristics

8. Minimal noise injection to substrate
9. Low leakage currents
10. No oscillations during transitions
11. Compatible with synthesis tools
12. Characteristics do not degrade too much with temperature
13. Characteristics do not vary too much with process variations

Are some of these more important than others?

Yes! – must have well-defined logic levels for circuits to even function as logic
What are the logic levels for a given inverter of a given logic family?

\[ V_H = ? \quad \text{and} \quad V_L = ? \]

Can we legislate them?

- Some authors choose to simply define a value for them
- Simple and straightforward approach
- But what if the circuit does not interpret them the same way they are defined!!
What are the logic levels for a given inverter of for a given logic family?

\[ V_H = ? \]

\[ V_L = ? \]

Can we legislate them?

World’s most widely used electronics text
What are the logic levels for a given inverter of for a given logic family?

$V_H = ?$

$V_L = ?$

Can we legislate them?

![CMOS VLSI Design](image)
What are the logic levels for a given inverter of for a given logic family?

\[ V_H = ? \quad V_L = ? \]

Can we legislate them?

- Some authors choose to define them based upon specific features of inverter
- Analytical expressions may be complicated
- But what if the circuit does not interpret them the same way they are defined!!
What are the logic levels for a given inverter of for a given logic family?

\[ V_H = ? \quad V_L = ? \]

Ask the inverter how it will interpret logic levels

- The inverter will interpret them the way the circuit really operate as a Boolean system!!
- Analytical expressions may be complicated
- How is this determination made?
Ask the inverter how it will interpret logic levels

\[ V_{\text{IN}} \rightarrow V_{\text{OUT}} \]

\[ V_H = ? \]

\[ V_L = ? \]

Consider a very long cascade of inverters

Apply a large voltage at the input (alternatively a small input could be used)

w.l.o.g. assume an even number of inverters in chain indicated

\[ V_{\text{LARGE}} \rightarrow \cdots \rightarrow \cdots \rightarrow \cdots \rightarrow \text{even number of stages} \]
Ask the inverter how it will interpret logic levels

\[ V_H = ? \]
\[ V_L = ? \]

Consider a very long cascade of inverters

Apply a large voltage at the input (alternatively a small input could be used)

w.l.o.g. assume an even number of inverters in chain indicated

If logic levels are to be maintained, the voltage at the end of this even number of stages must be \( V_H \), that of the next must be \( V_L \), the next \( V_H \), etc. until the start of the cascade is approached
Ask the inverter how it will interpret logic levels

$V_{IN} \rightarrow V_{OUT}$

$V_H = ?$

$V_L = ?$

$V_{OUT}$

$V_{IN}$

$V_{LARGE}$

$V_H \rightarrow V_H \rightarrow V_H \rightarrow \cdots$

$V_{IN}$

$S_1$

$S_2$

$S_3$

$V_H \rightarrow V_L \rightarrow V_H \rightarrow \cdots$

$V_{LARGE}$

$V_{H}\rightarrow V_{H}\rightarrow V_{H}$
Ask the inverter how it will interpret logic levels

V_H = ?
V_L = ?
Ask the inverter how it will interpret logic levels

\[ V_H = ? \]
\[ V_L = ? \]

- Two inverter loop
- Very useful circuit!
Ask the inverter how it will interpret logic levels

Thus, consider the inverter pair
Ask the inverter how it will interpret logic levels

V\(_H\) and V\(_L\) will be on the intersection of the transfer characteristics of the inverter pair (IPTC) and the V\(_{\text{OUT}}\) = V\(_{\text{IN}}\) line.

V\(_H\) and V\(_L\) are often termed the “1” and “0” states.
Ask the inverter how it will interpret logic levels

V_{IN} \quad V_{OUT} \quad V'_{OUT}

Inverter pair

When V'_{OUT}=V_{IN}, V_H and V_L are stable operating points, V_{TRIP} is a quasi-stable operating point.

Observe: slope of IPTC is greater than 1 at V_{TRIP} and less than 1 at V_H and V_L.
When $V_{\text{OUT}} = V_{\text{IN}}$ for the inverter, $V'_{\text{OUT}}$ is also equal to $V_{\text{IN}}$. Thus the intersection point for $V_{\text{OUT}} = V_{\text{IN}}$ in the inverter transfer characteristics (ITC) is also an intersection point for $V'_{\text{OUT}} = V_{\text{IN}}$ in the inverter-pair transfer characteristics (IPTC).

Implication: Inverter characteristics can be used directly to obtain $V_{\text{TRIP}}$. 
Logic Family Characteristics

What properties of an inverter are necessary for it to be useful for building a two-level logic family?

The inverter-pair transfer characteristics must have three unique intersection points with the $V'_{OUT} = V_{IN}$ line.

What are the logic levels for a given inverter or for a given logic family?

The two extreme intersection points of the inverter-pair transfer characteristics with the $V'_{OUT} = V_{IN}$ line.

Can we legislate $V_H$ and $V_L$ for a logic family? No!

What other properties of the inverter are desirable?

Reasonable separation between $V_H$ and $V_L$ (enough separation so that noise does not cause circuit to interpret level incorrectly)

$$V_{TRIP} \approx \frac{V_H + V_L}{2}$$ (to provide adequate noise immunity and process insensitivity)
What happens near the quasi-stable operating point?

$S_2$ closed and $X=Y=V_{TRIP}$
What happens near the quasi-stable operating point?

$S_2$ closed and $X=Y=V_{\text{TRIP}}$

If $X$ decreases even very slightly, will move to the $X=0$, $Y=1$ state (very fast)

If $X$ increases even very slightly, will move to the $X=1$, $Y=0$ state (very fast)
What are the transfer characteristics of the static CMOS inverter pair?

Consider first the inverter
Transfer characteristics of the static CMOS inverter
Transfer characteristics of the static CMOS inverter
(Neglect λ effects)

Case 1  
Vin is so high that $M_1$ triode, $M_2$ cutoff

\[ I_{D1} = \mu_n C_{oxn} \frac{W_1}{L_1} \left( V_{IN} - V_{Tn} - \frac{V_{OUT}}{2} \right) V_{OUT} \]

\[ I_{D2} = 0 \]

Equating $I_{D1}$ and $-I_{D2}$ we obtain:

\[ 0 = \mu_n C_{oxn} \frac{W_1}{L_1} \left( V_{IN} - V_{Tn} - \frac{V_{OUT}}{2} \right) V_{OUT} \]

It can be shown that setting the first product term to 0 will not verify, thus

\[ V_{OUT} = 0 \]

valid for:

\[ V_{GS1} \geq V_{Tn} \quad V_{DS1} < V_{GS1} - V_{Tn} \quad V_{GS2} \geq V_{Tp} \]

thus, valid for:

\[ V_{IN} \geq V_{Tn} \quad V_{OUT} < V_{IN} - V_{Tn} \quad V_{IN} - V_{DD} \geq V_{Tp} \]
Graphical Interpretation of these conditions:

\[ V_{IN} \geq V_{Tn} \quad V_{OUT} < V_{IN} - V_{Tn} \quad V_{IN} - V_{DD} \geq V_{Tp} \]
Transfer characteristics of the static CMOS inverter  
(Neglect $\lambda$ effects)

Case 1  $M_1$ triode, $M_2$ cutoff

$V_{\text{out}} = 0$
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

Case 1  $M_1$ triode, $M_2$ cutoff

$V_{\text{out}} = 0$
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

Partial solution:
Regions of Operation for Devices in CMOS inverter
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

Case 2 $M_1$ triode, $M_2$ sat

$M_2$: Square law ID
$M_1$: like a resistor

$\Rightarrow$: square law $V_{out}$
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

Case 2 $M_1$ triode, $M_2$ sat

\[ I_{D1} = \mu_n C_{Ox} \frac{W_1}{L_1} \left( V_{IN} - V_{Tn} - \frac{V_{OUT}}{2} \right) V_{OUT} \]

\[ I_{D2} = -\frac{\mu_p C_{Ox}}{2} \frac{W_2}{L_2} \left( V_{IN} - V_{DD} - V_{Tp} \right)^2 \]

Equating $I_{D1}$ and $-I_{D2}$ we obtain:

\[ \frac{\mu_p C_{Ox}}{2} \frac{W_2}{L_2} \left( V_{IN} - V_{DD} - V_{Tp} \right)^2 = \mu_n C_{Ox} \frac{W_1}{L_1} \left( V_{IN} - V_{Tn} - \frac{V_{OUT}}{2} \right) V_{OUT} \]

valid for:

\[ V_{GS1} \geq V_{Tn} \quad V_{DS1} < V_{GS1} - V_{Tn} \quad V_{GS2} \leq V_{Tp} \quad V_{DS2} \leq V_{GS2} - V_{T2} \]

thus, valid for:

\[ V_{IN} \geq V_{Tn} \quad V_{OUT} < V_{IN} - V_{Tn} \quad V_{IN} - V_{DD} \leq V_{Tp} \quad V_{OUT} - V_{DD} \leq V_{IN} - V_{DD} - V_{Tp} \]
Transfer characteristics of the static CMOS inverter
(Neglect \( \lambda \) effects)

**Case 2**  \( M_1 \) triode, \( M_2 \) sat

\[
\begin{align*}
V_{\text{OUT}} - V_{\text{DD}} & \leq V_{\text{IN}} - V_{\text{DD}} - V_{Tp} \\
V_{\text{IN}} & \geq V_{Tn} \\
V_{\text{OUT}} & < V_{\text{IN}} - V_{Tn} \\
V_{\text{IN}} - V_{\text{DD}} & \leq V_{Tp}
\end{align*}
\]
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

Case 2 $M_1$ triode, $M_2$ sat

$$V_{OUT} \quad V_{DD}$$

$$V_{DD} \quad V_{IN} \quad V_{OUT} \quad -V_{Tp} \quad VTn \quad V_{DD}+V_{Tp}$$

$$V_{OUT} - V_{DD} \leq V_{IN} - V_{DD} - V_{Tp}$$

$$V_{IN} \geq V_{Tn}$$

$$V_{OUT} < V_{IN} - V_{Tn}$$

$$V_{IN} - V_{DD} \leq V_{Tp}$$
Transfer characteristics of the static CMOS inverter

Partial solution:
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

Case 3 $M_1$ sat, $M_2$ sat
Transfer characteristics of the static CMOS inverter
(Neglect λ effects)

Case 3  \( M_1 \) sat, \( M_2 \) sat

\|
\|_b1 = \frac{\mu_n C_{Ox_n}}{2} \frac{W_1}{L_1} \left( V_{IN} - V_{Tn} \right)^2
\|
\|_b2 = \frac{\mu_p C_{Ox_p}}{2} \frac{W_2}{L_2} \left( V_{IN} - V_{DD} - V_{Tp} \right)^2

Equating \( I_{b1} \) and \(-I_{b2}\) we obtain:

\frac{\mu_p C_{Ox_p}}{2} \frac{W_2}{L_2} \left( V_{IN} - V_{DD} - V_{Tp} \right)^2 = \frac{\mu_n C_{Ox_n}}{2} \frac{W_1}{L_1} \left( V_{IN} - V_{Tn} \right)^2

Which can be rewritten as:

\sqrt{\frac{\mu_p C_{Ox_p}}{2} \frac{W_2}{L_2} \left( V_{DD} + V_{Tp} - V_{IN} \right)} = \sqrt{\frac{\mu_n C_{Ox_n}}{2} \frac{W_1}{L_1} \left( V_{IN} - V_{Tn} \right)}

Which can be simplified to:

\|
V_{IN} = \left( V_{Tn} \right) \sqrt{\frac{\mu_n C_{Ox_n}}{2} \frac{W_1}{L_1}} + \left( V_{DD} + V_{Tp} \right) \sqrt{\frac{\mu_p C_{Ox_p}}{2} \frac{W_2}{L_2}}
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

Case 3  $M_1$ sat, $M_2$ sat

\[
V_{\text{IN}} = \frac{(V_{\text{Tn}}) \sqrt{\frac{\mu_n C_{Ox_n} W_1}{2 L_1}} + (V_{\text{DD}} + V_{Tp}) \sqrt{\frac{\mu_p C_{Ox_p} W_2}{2 L_2}}}{\sqrt{\frac{\mu_n C_{Ox_n} W_1}{2 L_1}} + \sqrt{\frac{\mu_p C_{Ox_p} W_2}{2 L_2}}}
\]

Since $C_{Ox_n} \approx C_{Ox_p} = C_{ox}$ this can be simplified to:

\[
V_{\text{IN}} = \frac{(V_{\text{Tn}}) \sqrt{\frac{W_1}{L_1}} + (V_{\text{DD}} + V_{Tp}) \sqrt{\frac{\mu_p W_2}{\mu_n L_2}}}{\sqrt{\frac{W_1}{L_1}} + \sqrt{\frac{\mu_p W_2}{\mu_n L_2}}}
\]

valid for:

\[
V_{GS1} \geq V_{Tn} \quad V_{DS1} \geq V_{GS1} - V_{Tn} \quad V_{GS2} \leq V_{Tp} \quad V_{DS2} \leq V_{GS2} - V_{T2}
\]

thus, valid for:

\[
V_{\text{IN}} \geq V_{Tn} \quad V_{\text{OUT}} \geq V_{\text{IN}} - V_{Tn} \quad V_{\text{IN}} - V_{\text{DD}} \leq V_{Tp} \quad V_{\text{OUT}} - V_{\text{DD}} \leq V_{\text{IN}} - V_{\text{DD}} - V_{Tp}
\]
Transfer characteristics of the static CMOS inverter

(Neglect $\lambda$ effects)

Case 3  $M_1$ sat, $M_2$ sat

\[ V_{\text{OUT}} - V_{\text{DD}} \leq V_{\text{IN}} - V_{\text{DD}} - V_{Tp} \]

\[ V_{\text{IN}} \geq V_{Tn} \]

\[ V_{\text{OUT}} \geq V_{\text{IN}} - V_{Tn} \]

\[ V_{\text{IN}} - V_{\text{DD}} \leq V_{Tp} \]
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

Case 3  $M_1$ sat, $M_2$ sat

\[ V_{\text{OUT}} - V_{\text{DD}} \leq V_{\text{IN}} - V_{\text{DD}} - V_{\text{Tp}} \]

\[ V_{\text{IN}} \geq V_{Tn} \]

\[ V_{\text{OUT}} \geq V_{\text{IN}} - V_{Tn} \]

\[ V_{\text{IN}} - V_{\text{DD}} \leq V_{\text{Tp}} \]
Transfer characteristics of the static CMOS inverter
(Neglect \( \lambda \) effects)

Partial solution:

Diagram showing the transfer characteristics with labeled points for cases 1, 2, and 3.

- Case 1
  - Point at \( V_{DD} \)
  - Point at \( V_{DD} + V_{Tp} \)

- Case 2
  - Point at \( V_{Tn} \)
  - Point at \( -V_{Tp} \)

- Case 3
  - Point at an intermediate position between Case 1 and Case 2
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

Case 4 $M_1$ sat, $M_2$ triode

\[ \text{Transfer characteristics of the static CMOS inverter} \]

\[ \text{(Neglect $\lambda$ effects)} \]

\[ \text{Case 4} \quad M_1 \text{ sat, } M_2 \text{ triode} \]
Transfer characteristics of the static CMOS inverter
(Neglect \( \lambda \) effects)

Case 4 \( M_1 \) sat, \( M_2 \) triode

\[
I_{D1} = \mu_n C_{Oxn} \frac{W_1}{L} (V_{IN} - V_{Tn})^2
\]

\[
I_{D2} = -\mu_p C_{Oxp} \frac{W_2}{L_2} \left( V_{IN} - V_{DD} - V_{Tp} - \frac{V_{OUT} - V_{DD}}{2} \right) \cdot (V_{OUT} - V_{DD})
\]

Equating \( I_{D1} \) and \( -I_{D2} \) we obtain:

\[
\frac{\mu_n C_{Oxn}}{2} \frac{W_1}{L_1} (V_{IN} - V_{Tn})^2 = -\mu_p C_{Oxp} \frac{W_2}{L_2} \left( V_{IN} - V_{DD} - V_{Tp} - \frac{V_{OUT} - V_{DD}}{2} \right) \cdot (V_{OUT} - V_{DD})
\]

valid for:

\[
V_{GS1} \geq V_{Tn} \quad V_{DS1} \geq V_{GS1} - V_{Tn} \quad V_{GS2} \leq V_{Tp} \quad V_{DS2} > V_{GS2} - V_{T2}
\]

thus, valid for:

\[
V_{IN} \geq V_{Tn} \quad V_{OUT} \geq V_{IN} - V_{Tn} \quad V_{IN} - V_{DD} \leq V_{Tp} \quad V_{OUT} - V_{DD} > V_{IN} - V_{DD} - V_{Tp}
\]
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

Case 4  $M_1$ sat, $M_2$ triode

\[
\begin{align*}
V_{\text{OUT}} & = -V_{\text{DD}} > V_{\text{IN}} - V_{\text{DD}} - V_{\text{Tp}} \\
V_{\text{IN}} & \geq V_{Tn} \\
V_{\text{OUT}} & \geq V_{\text{IN}} - V_{Tn} \\
V_{\text{IN}} - V_{\text{DD}} & \leq V_{\text{Tp}}
\end{align*}
\]
Transfer characteristics of the static CMOS inverter  
(Neglect \( \lambda \) effects)

Case 4 \( M_1 \) sat, \( M_2 \) triode

\[ V_{OUT} - V_{DD} > V_{IN} - V_{DD} - V_{Tp} \]
\[ V_{IN} \geq V_{Tn} \]
\[ V_{OUT} \geq V_{IN} - V_{Tn} \]
\[ V_{IN} - V_{DD} \leq V_{Tp} \]
Transfer characteristics of the static CMOS inverter

(Neglect $\lambda$ effects)

Partial solution:
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

Case 4 $M_1$ cutoff, $M_2$ triode
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

Case 5  $M_1$ cutoff, $M_2$ triode

$I_{d1} = 0$

$I_{d2} = -\mu_p C_{Ox p} \frac{W^2}{L^2} \left( V_{IN} - V_{DD} - V_{Tp} - \frac{V_{OUT} - V_{DD}}{2} \right) \cdot (V_{OUT} - V_{DD})$

Equating $I_{d1}$ and $-I_{d2}$ we obtain:

$\mu_p C_{Ox p} \frac{W^2}{L^2} \left( V_{IN} - V_{DD} - V_{Tp} - \frac{V_{OUT} - V_{DD}}{2} \right) \cdot (V_{OUT} - V_{DD}) = 0$

valid for:

$V_{GS1} < V_{Tn}$

$V_{GS2} \leq V_{Tp}$

$V_{DS2} > V_{GS2} - V_{T2}$

thus, valid for:

$V_{IN} < V_{Tn}$

$V_{IN} - V_{DD} \leq V_{Tp}$

$V_{OUT} - V_{DD} > V_{IN} - V_{DD} - V_{Tp}$
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

Case 5  $M_1$ cutoff, $M_2$ triode
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

Case 5  $M_1$ cutoff, $M_2$ triode
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)
Transfer characteristics of the static CMOS inverter
(Neglect \( \lambda \) effects)
Transfer characteristics of the static CMOS inverter

(Neglect $\lambda$ effects)

From Case 3 analysis:

$$V_{IN} = \frac{(V_{Tn}) + (V_{DD} + V_{Tp})}{1 + \sqrt{\frac{\mu_p}{\mu_n} \frac{W_2}{W_1} \frac{L_1}{L_2}}}$$
Inverter Transfer Characteristics of Inverter Pair

\[ V_{\text{IN}} \rightarrow \rightarrow \rightarrow V'O_{\text{OUT}} \]

What are \( V_H \) and \( V_L \)?

Find the points on the inverter pair transfer characteristics where \( V'_{\text{OUT}} = V_{\text{IN}} \) and the slope is less than 1.
Inverter Transfer Characteristics of Inverter Pair for **THIS** Logic Family

\[
\begin{align*}
V_{\text{IN}} & \quad \Downarrow \quad \text{V' OUT} \\
V'_{\text{OUT}} & \quad \Downarrow \quad V_{\text{H}} \quad V_{\text{L}} \quad V_{\text{TRIP}} \quad V_{\text{DD}} + V_{\text{Tp}} \quad V_{\text{DD}} \\
V_{\text{H}} &= V_{\text{DD}} \quad \text{and} \quad V_{\text{L}} = 0
\end{align*}
\]

Note this is independent of device sizing for **THIS** logic family !!
Sizing of the Basic CMOS Inverter

The characteristic that device sizes do not need to be used to establish $V_H$ and $V_L$ logic levels is a major advantage of this type of logic.

How should $M_1$ and $M_2$ be sized?

How many degrees of freedom are there in the design of the inverter?
How should $M_1$ and $M_2$ be sized?

How many degrees of freedom are there in the design of the inverter?

$$\{ W_1, W_2, L_1, L_2 \}$$

4 degrees of freedom

But in basic device model and in most performance metrics, $W_1/L_1$ and $W_2/L_2$ appear as ratios

$$\{ W_1/L_1, W_2/L_2 \}$$

effectively 2 degrees of freedom
How should $M_1$ and $M_2$ be sized?

$\{ W_1, W_2, L_1, L_2 \}$ 4 degrees of freedom  Usually pick $L_1 = L_2 = L_{\text{min}}$

$\{ W_1, W_2 \}$ effectively 2 degrees of freedom

How are $W_1$ and $W_2$ chosen?

Depends upon what performance parameters are most important for a given application!
How should $M_1$ and $M_2$ be sized?

Pick $L_1=L_2=L_{\text{min}}$

One popular sizing strategy:
1. Pick $W_1=W_{\text{MIN}}$ to minimize area of $M_1$
2. Pick $W_2$ to set trip-point at $V_{\text{DD}}/2$

Observe Case 3 provides expression for $V_{\text{TRIP}}$

Thus, at the trip point,

$$V_{\text{OUT}} = V_{\text{IN}} = V_{\text{TRIP}} = \frac{V_{\text{DD}}}{2}, \quad \text{if} \quad \frac{W_2}{W_1} = \frac{\mu_n}{\mu_p}$$
End of Lecture 36