Static CMOS Logic Gates
  - Ratio Logic
Propagation Delay
  - Simple analytical models
  - Elmore Delay
Sizing of Gates
Digital Circuit Design

- Hierarchical Design
- Basic Logic Gates
- Properties of Logic Families
- Characterization of CMOS Inverter

Static CMOS Logic Gates
  - Ratio Logic

Propagation Delay
  - Simple analytical models
  - Elmore Delay

Sizing of Gates

- Propagation Delay with Multiple Levels of Logic
- Optimal driving of Large Capacitive Loads
- Power Dissipation in Logic Circuits
- Other Logic Styles
- Array Logic
- Ring Oscillators
Review from last time

Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

$$V_{OUT} - V_{DD} \leq V_{IN} - V_{DD} - V_T$$

$$V_{IN} \geq V_{Tn}$$

$$V_{OUT} \geq V_{IN} - V_{Tn}$$

$$V_{IN} - V_{DD} \leq V_T$$

Review from last time
Transfer characteristics of the static CMOS inverter

(Neglect $\lambda$ effects)

\[ V_{\text{TRIP}} = \frac{\left( V_{\text{Tn}} \right) + \left( V_{\text{DD}} + V_{\text{Tp}} \right) \sqrt{\frac{\mu_p}{\mu_n} \frac{W_2}{W_1} \frac{L_1}{L_2}}}{1 + \sqrt{\frac{\mu_p}{\mu_n} \frac{W_2}{W_1} \frac{L_1}{L_2}}} \]
How should $M_1$ and $M_2$ be sized?

pick $L_1=L_2=L_{\text{min}}$

One popular sizing strategy:
1. Pick $W_1=W_{\text{MIN}}$ to minimize area of $M_1$
2. Pick $W_2$ to set trip-point at $V_{\text{DD}}/2$

Typically $V_{Tn}=0.2V_{\text{DD}}$, $|V_{Tp}|=0.2V_{\text{DD}}$

$V_{\text{TRIP}} = \frac{(V_{Tn}) + (V_{DD} + V_{Tn}) \sqrt{\frac{\mu_p}{\mu_n}} \frac{W_2}{W_1} \frac{L_1}{L_2}}{1 + \sqrt{\frac{\mu_p}{\mu_n}} \frac{W_2}{W_1} \frac{L_1}{L_2}}$

$\therefore \frac{V_{DD}}{2} = \frac{(0.2V_{DD}) + (V_{DD} - 0.2V_{DD}) \sqrt{\frac{\mu_p}{\mu_n}} \frac{W_2}{W_1}}{1 + \sqrt{\frac{\mu_p}{\mu_n}} \frac{W_2}{W_1}}$

Solving this equation for $W_2$, obtain

$W_2 = W_1 \left( \frac{\mu_n}{\mu_p} \right)$

Other sizing strategies are used as well and will be discussed later!
Extension of Basic CMOS Inverter to Multiple-Input Gates

Review from last time

Performs as a 2-input NOR Gate

Can be easily extended to an n-input NOR Gate
Review from last time

Extension of Basic CMOS Inverter to Multiple-Input Gates

Performs as a 2-input NAND Gate

Can be easily extended to an n-input NAND Gate

Truth Table

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General Logic Family

Review from last time

p-channel PUN
n-channel PDN

Arbitrary PUN and PDN
Other CMOS Logic Families

Enhancement Load NMOS

Enhancement Load Pseudo-NMOS

Depletion Load NMOS
Other CMOS Logic Families

- High and low swings are reduced
- Response time is slow on LH output transitions
- Static Power Dissipation Large when $V_{OUT}$ is low
- Very economical process
- Termed “ratio logic” ($V_H$ or $V_L$ dependent upon device sizes)
- Compact layout (no wells !)
- Degree of freedom in sizing required to establish $V_L$
Other CMOS Logic Families

Enhancement Load NMOS

- Multiple-input gates require single transistor for each additional input
- Still useful if many inputs are required (static power does not increase with $k$)
Other CMOS Logic Families

- High and low swings are reduced
- Response time is slow on LH output transitions
- Static Power Dissipation Large when $V_{OUT}$ is low
- Termed “ratio” logic
Other CMOS Logic Families

- $V_{IN}$
- $V_{OUT}$
- $V_{DD}$
- $V_{TD}<0$

- Low swing is reduced
- Static Power Dissipation Large when $V_{OUT}$ is low
- Very economical process
- Termed “ratio” logic
- Compact layout (no wells !)
- Dominant MOS logic until about 1985
- Depletion device not available in most processes today
Other CMOS Logic Families

- Reduced $V_{H}-V_{L}$
- Device sizing critical for even basic operation
- Shallow slope at $V_{TRIP}$
Other CMOS Logic Families

- Reduced $V_{H} - V_{L}$
- Device sizing critical for even basic operation
- Shallow slope at $V_{\text{TRIP}}$
Other CMOS Logic Families

- Reduced $V_H - V_L$
- Device sizing critical for even basic operation
- Shallow slope at $V_{TRIP}$
Static Power Dissipation in Static CMOS Family

When $V_{\text{OUT}}$ is Low, $I_{D1}=0$

When $V_{\text{OUT}}$ is High, $I_{D2}=0$

Thus, $P_{\text{STATIC}}=0$

This is a key property of the static CMOS Logic Family and is the major reason Static CMOS Logic is so dominant

It can be shown that this zero static power dissipation property can be preserved if the PUN is comprised of n-channel devices, the PDN is comprised of n-channel devices and they are never both driven into the conducting states at the same time
Static Power Dissipation in Ratio Logic Families

Example: Assume $V_{DD}=5V$
$V_T=1V$, $\mu C_{OX}=10^{-4}A/V^2$, $W_1/L_1=1$ and $M_2$ sized so that $V_L=V_Tn$

Observe:

$V_H=V_{DD}-V_{Tn}$

If $V_{IN}=V_H$, $V_{OUT}=V_L$ so

$$I_{D1} = \frac{\mu C_{OX} W_1}{L_1} \left( V_{GS1} - V_T - \frac{V_{DS1}}{2} \right) V_{DS1}$$

$$I_{D1} = 10^{-4} \left( 5 - 1 - 1 - \frac{1}{2} \right) \cdot 1 = 0.25mA$$

$$P_L=(5V)(0.25mA)=1.25mW$$

Enhancement Load NMOS
Static Power Dissipation in Ratio Logic Families

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Assume $V_{DD}=5V$
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If a circuit has 100,000 gates and half of them are in the $V_{OUT}=V_L$ state, the static power dissipation will be
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$$P_{STATIC} = \frac{1}{2}10^5 \bullet 1.25mW = 62.5W$$

This power dissipation is way too high and would be even larger in circuits with 100 million or more gates – the level of integration common in SoC circuits today
Propagation Delay in Static CMOS Family

Switch-level model of Static CMOS inverter (neglecting diffusion parasitics)
Propagation Delay in Static CMOS Family

Switch-level model of Static CMOS inverter (neglecting diffusion parasitics)
Propagation Delay in Static CMOS Family

Since operating in triode through most of transition:

\[ I_D = \frac{\mu C_{OX} W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} = \frac{\mu C_{OX} W}{L} (V_{GS} - V_T) V_{DS} \]

\[ R_{PD} = \frac{L_1}{\mu_n C_{OX} W_1 (V_{DD} - V_{Tn})} \]

\[ I_D = \frac{\mu C_{OX} W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} = \frac{\mu C_{OX} W}{L} (V_{GS} - V_T) V_{DS} \]

\[ R_{PU} = \frac{L_2}{\mu_p C_{OX} W_2 (V_{DD} + V_{Tp})} \]

\[ C_{IN} = C_{OX} \left( W_1 L_1 + W_2 L_2 \right) \]
Propagation Delay in Static CMOS Family

Example: Minimum-sized $M_1$ and $M_2$

If $u_n C_{OX} = 100 \mu A V^{-2}$, $C_{OX} = 4 \text{fF} \mu^{-2}$, $V_{TN} = V_{DD}/5$, $V_{TP} = -V_{DD}/5$, $\mu_n/\mu_p = 3$, $L_1 = W_1 = L_{MIN}$, $L_2 = W_2 = L_{MIN}$, $L_{MIN} = 0.5 \mu$ and $V_{DD} = 5V$

$$R_{PD} = \frac{1}{10^{-4} \cdot 0.8 V_{DD}} = 2.5K\Omega$$

$$C_{IN} = 4 \cdot 10^{-15} \cdot 2L_{MIN}^2 = 2fF$$

$$R_{PU} = \frac{1}{10^{-4} \cdot \frac{1}{3} \cdot 0.8 V_{DD}} = 7.5K\Omega$$
Propagation Delay in Static CMOS Family

In typical process with Minimum-sized $M_1$ and $M_2$:
- $R_{PD}$; 2.5KΩ
- $R_{PU}$; 3$R_{PD}$ = 7.5KΩ
- $C_{IN}$; 2fF
Propagation Delay in Static CMOS Family

In typical process with Minimum-sized $M_1$ and $M_2$:

- $R_{PD}$; 2.5KΩ
- $R_{PU}$; $3R_{PD} = 7.5$KΩ
- $C_{IN}$; 2fF

How long does it take for a signal to propagate from $x$ to $z$?
Propagation Delay in Static CMOS Family

Consider:

For HL output transition, $C_L$ charged to $V_{DD}$

Ideally:
Propagation Delay in Static CMOS Family

For HL output transition, $C_L$ charged to $V_{DD}$

Actually:

What is the transition time $t_{HL}$?
Propagation Delay in Static CMOS Family
Propagation Delay in Static CMOS Family

For HL output transition, $C_L$ charged to $V_{DD}$

$$V_{OUT} = F + (1 - F) e^{-\frac{t}{\tau}} = 0 + (V_{DD} - 0)e^{-\frac{t}{R_P D C_L}}$$

$$\frac{V_{DD}}{e} = V_{DD} e^{-\frac{t_1}{R_P D C_L}}$$

$t_1 = R_P D C_L$

If $V_{TRIP}$ is close to $V_{DD}/2$, $t_{HL}$ is close to $t_1$
Propagation Delay in Static CMOS Family

For HL output transition, $C_L$ charged to $V_{DD}$

Summary:

$t_{LH} \approx R_{PU} C_L$

$t_{HL} \approx R_{PD} C_L$
Propagation Delay in Static CMOS Family

In typical process with Minimum-sized $M_1$ and $M_2$:

\[ t_{HL} \equiv R_{PD}C_L \equiv 2.5\,\text{K}\cdot2\,\text{fF}=5\,\text{ps} \]

\[ t_{LH} \equiv R_{PU}C_L \equiv 7.5\,\text{K}\cdot2\,\text{fF}=15\,\text{ps} \]

Note: LH transition is much slower than HL transition
Propagating Delay in Static CMOS Family

Defn: The Propagation Delay of a gate is defined to be the sum of $t_{HL}$ and $t_{LH}$, that is, $t_{PROP}=t_{HL}+t_{LH}$

$$t_{PROP} = t_{HL} + t_{LH} \cong C_L (R_{PU} + R_{PD})$$

Propagation delay represents a fundamental limit on the speed a gate can be clocked.

For basic two-inverter cascade in static CMOS logic:

In typical process with minimum-sized $M_1$ and $M_2$:

$$t_{PROP} = t_{HL} + t_{LH} \cong 20 \mu \text{sec}$$
Propogation Delay in Static CMOS Family

The propagation delay through k levels of logic is approximately the sum of the individual delays in the same path.
Propagation Delay in Static CMOS Family

Example:

\[ t_{HL} = t_{HL4} + t_{HL3} + t_{HL2} + t_{HL1} \]
\[ t_{LH} = t_{LH4} + t_{LH3} + t_{LH2} + t_{HL1} \]
\[ t_{PROP} = t_{LH} + t_{HL} = (t_{LH4} + t_{HL3} + t_{HL2} + t_{HL1}) + (t_{HL4} + t_{LH3} + t_{HL2} + t_{HL1}) \]
\[ t_{PROP} = t_{LH} + t_{HL} = (t_{LH4} + t_{HL4}) + (t_{LH3} + t_{HL3}) + (t_{HL2} + t_{HL2}) + (t_{HL1} + t_{HL1}) \]
\[ t_{PROP} = t_{PROP4} + t_{PROP3} + t_{PROP2} + t_{PROP1} \]
Propagation Delay in Static CMOS Family

Propagation through k levels of logic

\[ t_{HL} + t_{HLk} + t_{LH(k-1)} + t_{HL(k-2)} + \cdots + t_{XY1} \]

\[ t_{LH} + t_{LHk} + t_{HL(k-1)} + t_{LH(k-2)} + \cdots + t_{YX1} \]

where \( x=H \) and \( Y=L \) if \( k \) odd and \( X=L \) and \( Y=h \) if \( k \) even

\[ t_{PROP} = \sum_{i=1}^{k} t_{PROP_k} \]
Device Sizing

Degrees of Freedom?

Will consider the inverter first
Device Sizing

Degrees of Freedom?

Strategies?
Device Sizing

- Since not ratio logic, \( V_H \) and \( V_L \) are independent of device sizes for this inverter

- With \( L_1 = L_2 = L_{\text{min}} \), there are 2 degrees of freedom (\( W_1 \) and \( W_2 \))

Sizing Strategies

- Minimum Size

- Fixed \( V_{\text{TRIP}} \)

- Equal rise-fall times (equal worst-case rise and fall times)

- Minimum power dissipation

- Minimum time required to drive a given load

- Minimum input capacitance
Device Sizing

Sizing Strategy: minimum sized

\[ R_{PD} = \frac{L_1}{\mu_n C_{OX} W_1 (V_{DD} - V_{Tn})} \]

\[ R_{PU} = \frac{L_2}{\mu_p C_{OX} W_2 (V_{DD} + V_{Tp})} \]

\[ C_{in} = C_{OX} (W_1 L_1 + W_2 L_2) \]
Device Sizing

Sizing Strategy: minimum sized

$W_1 = W_2 = W_{MIN}$

also provides minimum input capacitance

$t_{LH}$ is longer than $t_{HL}$

$t_{HL} = R_{PD}C_L$

$t_{HL} = 3R_{PD}C_L$

$$V_{TRIP} = \frac{(0.2V_{DD}) + (V_{DD} - 0.2V_{DD})\sqrt{1}}{1 + \sqrt{3}} = 0.42V_{DD}$$
Device Sizing

Sizing strategy: Equal (worst-case) rise and fall times
Device Sizing

Sizing strategy: Equal (worst-case) rise and fall times

\[
\frac{t_{\text{IH}}}{t_{\text{IL}}} = \frac{R_{\text{PU}}C_{\text{IN}}}{R_{\text{PD}}C_{\text{IN}}} \Rightarrow R_{\text{PU}} = R_{\text{PD}}
\]

Thus

\[
\frac{L_1}{u_nC_{\text{OX}}W_1(V_{\text{DD}}-V_{\text{Tn}})} = \frac{L_2}{u_pC_{\text{OX}}W_2(V_{\text{DD}}+V_{\text{Tp}})}
\]

with \(L_1 = L_2\) and \(V_{\text{Tp}} = -V_{\text{Tn}}\) we must have

\[
\frac{W_2}{W_1} = \frac{\mu_n}{\mu_p}
\]

What about the second degree of freedom?

\(V_{\text{TRIP}} = ?\)
Device Sizing

Sizing strategy: Equal (worst-case) rise and fall times

\[ W_2 = \frac{\mu_n}{\mu_p} \]

\[ V_{\text{trip}} = \frac{(V_{\text{tn}}) + (V_{\text{dd}} + V_{\text{tp}}) \sqrt{\frac{\mu_p}{\mu_n} \frac{W_2}{W_1} \frac{L_1}{L_2}}}{1 + \sqrt{\frac{\mu_p}{\mu_n} \frac{W_2}{W_1} \frac{L_1}{L_2}}} = \frac{0.2V_{\text{dd}} + 0.8V_{\text{dd}}}{2} = \frac{V_{\text{dd}}}{2} \]
Device Sizing

Sizing strategy: Fixed $V_{\text{TRIP}}$
Device Sizing

**Sizing strategy: Fixed \( V_{\text{TRIP}} \)**

Set \( V_{\text{TRIP}} = \frac{V_{\text{DD}}}{2} \)

\[
V_{\text{TRIP}} = \frac{(0.2V_{\text{DD}}) + (V_{\text{DD}} - 0.2V_{\text{DD}})}{1 + \sqrt{\frac{\mu_p W_2 L_1}{\mu_n W_1 L_2}}} = \frac{V_{\text{DD}}}{2}
\]

Solving, obtain

\[
\frac{W_2}{W_1} = \frac{\mu_n}{\mu_p}
\]

Observe this is the same sizing as was obtained for equal worst-case rise and fall times.

This is no coincidence and these properties guide the definition of the process parameters provided by the foundry.
Device Sizing

Sizing Strategies

- Minimum Size
- Fixed $V_{TRIP}$
- Equal rise-fall times
  (equal worst-case rise and fall times)
- Minimum power dissipation
- Minimum time required to drive a given load
- Minimum input capacitance
The reference inverter

Assume $\mu_n/\mu_p = 3$  
$L_n = L_p = L_{MIN}$  
$W_n = W_{MIN}$  
$W_p = 3W_n$

$C_{REF} \overset{\text{def}}{=} C_{INREF} = 4C_{OX} W_{MIN} L_{MIN}$

$R_{PDREF} = \frac{L_{MIN}}{\mu_n C_{OX} W_{MIN} (V_{DD} - V_{Tn})} = \frac{L_{MIN}}{\mu_n C_{OX} W_{MIN} (0.8V_{DD})}$

- Have sized the reference inverter with $W_p/W_n = \mu_n/\mu_p$
- In standard processes, provides $V_{TRIP}$, $V_{DD}/2$ and $t_{HL}$, $t_{LH}$
- Any other sizing strategy could have been used for the reference inverter but this is most convenient
The reference inverter pair

Assume $\mu_n/\mu_p = 3$, $L_n = L_p = L_{\text{MIN}}$, $W_n = W_{\text{MIN}}$, $W_p = 3W_n$

\[ C_{L1} = C_{\text{REF}} = 4C_{\text{OX}}W_{\text{MIN}}L_{\text{MIN}} \]

\[ t_{\text{REF}} = \begin{align*}
    \text{def} & \quad t_{\text{PROPREF}} = t_{\text{HLREF}} + t_{\text{LHREF}} = 2R_{\text{PDREF}}C_{\text{REF}}
\end{align*} \]
**Reference Inverter**

The reference inverter pair

Assume $\mu_n/\mu_p = 3$  
$L_n = L_p = L_{\text{MIN}}$  
$W_n = W_{\text{MIN}}$, $W_p = 3W_n$

Summary: parameters defined from reference inverter:

$$C_{\text{REF}} = 4C_{\text{OX}} W_{\text{MIN}} L_{\text{MIN}}$$

$$R_{\text{PDREF}} = \frac{\mu_n C_{\text{OX}} W_{\text{MIN}}}{L_{\text{MIN}}} \left( V_{\text{DD}} - V_{\text{Tn}} \right)$$

$$t_{\text{REF}} = 2R_{\text{PDREF}} C_{\text{REF}}$$

$$C_{\text{REF}} = 4C_{\text{OX}} W_{\text{MIN}} L_{\text{MIN}}$$
Propagation Delay

How does the propagation delay compare for a minimum-sized strategy to that of an equal rise/fall sizing strategy?

Minimum Sized

\[ W_2 = W_1 = W_{MIN} \]

Reference Inverter

\[ W_2 = (\mu_n/\mu_p)W_1, \quad W_1 = W_{MIN} \]

\[ t_{PROP} = t_{REF} \]
Device Sizing

The minimum-sized inverter pair

\[ C_{REF} = 4C_{OX} W_{MIN} L_{MIN} \]

\[ C_{L1} = 2C_{OX} W_{MIN} L_{MIN} = 0.5C_{REF} \]

\[ R_{PDn} = \frac{L_{MIN}}{\mu_n C_{OX} W_{MIN} (V_{DD} - V_{Tn})} = R_{PDREF} \]

\[ R_{PUp} = \frac{L_{MIN}}{\mu_p C_{OX} W_{MIN} (V_{DD} + V_{Tp})} = 3R_{PDREF} \]

\[ t_{PROP} = t_{HLREF} + t_{LHREF} = R_{PDREF} (0.5C_{REF}) + 3R_{PDREF} (0.5C_{REF}) = 2R_{PDREF} C_{REF} \]

thus \[ t_{PROP} = t_{REF} \]
Device Sizing

The minimum-sized inverter pair

Assume $\mu_n/\mu_p = 3 \quad L_n = L_p = L_{MIN} \quad W_n = W_{MIN}, \quad W_p = W_n$

\[ C_{REF} = 4C_{OX} W_{MIN} L_{MIN} \]

\[ C_{L1} = 0.5C_{REF} = 2C_{OX} W_{MIN} L_{MIN} \]

\[ R_{PDREF} = \frac{L_{MIN}}{\mu_n C_{OX} W_{MIN} (V_{DD} - V_{Tn})} \quad v_{Tn} = 2V_{DD} \]

\[ = \frac{L_{MIN}}{\mu_n C_{OX} W_{MIN} (0.8V_{DD})} \]

\[ t_{PROP} = t_{H\text{LREF}} + t_{L\text{HREF}} = R_{PDREF} (0.5C_{REF}) + 3R_{PDREF} (0.5C_{REF}) = 2R_{PDREF} C_{REF} \]

\[ t_{PROP} = t_{REFF} \]
Propagation Delay

How does the propagation delay compare for a minimum-sized strategy to that of an equal rise/fall sizing strategy?

Minimum Sized

\[ W_2 = W_1 = W_{\text{MIN}} \]

\[ t_{\text{PROP}} = t_{\text{REF}} \]

Reference Inverter

\[ W_2 = (\mu_n/\mu_p)W_1, \quad W_1 = W_{\text{MIN}} \]

\[ t_{\text{PROP}} = t_{\text{REF}} \]

Even though the \( t_{\text{LH}} \) rise time has been reduced with the equal rise/fall sizing strategy, this was done at the expense of an increase in the total load capacitance that resulted in no net change in propagation delay!