Sizing of Gates
How should $M_1$ and $M_2$ be sized?

pick $L_1 = L_2 = L_{min}$

One popular sizing strategy:
1. Pick $W_1 = W_{MIN}$ to minimize area of $M_1$
2. Pick $W_2$ to set trip-point at $V_{DD}/2$

Typically $V_{Tn} = 0.2V_{DD}$, $|V_{Tp}| = 0.2V_{DD}$

\[
V_{TRIP} = \frac{(V_{Tn}) + (V_{DD} + V_{Tp})}{\frac{1}{\mu_n W_1 L_2} + \sqrt{\frac{\mu_p W_2 L_1}{\mu_n W_1 L_2}}}.
\]

\[
V_{DD} \left(0.2V_{DD}\right) + \left(V_{DD} - 0.2V_{DD}\right) = \frac{0.2V_{DD} + (V_{DD} + 0.2V_{DD})}{\sqrt{\frac{\mu_p W_2}{\mu_n W_1}}}.
\]

\[\therefore \frac{V_{DD}}{2} = \frac{V_{DD} + 0.2V_{DD}}{1 + \sqrt{\frac{\mu_p W_2}{\mu_n W_1}}}.
\]

Solving this equation for $W_2$, obtain:

\[
W_2 = W_1 \left(\frac{\mu_n}{\mu_p}\right).
\]

Other sizing strategies are used as well and will be discussed later!
Extension of Basic CMOS Inverter to Multiple-Input Gates

Review from last time

Performs as a 2-input NOR Gate

Can be easily extended to an n-input NOR Gate
Other CMOS Logic Families

Review from last time

Enhancement Load NMOS

Enhancement Load Pseudo-NMOS

Depletion Load NMOS
Review from last time

Other CMOS Logic Families

- High and low swings are reduced
- Response time is slow on LH output transitions
- Static Power Dissipation Large when $V_{OUT}$ is low
- Very economical process
- Termed “ratio logic” ($V_H$ or $V_L$ dependent upon device sizes)
- Compact layout (no wells !)
- Degree of freedom in sizing required to establish $V_L$
Other CMOS Logic Families

Review from last time

- High and low swings are reduced
- Response time is slow on LH output transitions
- Static Power Dissipation Large when $V_{OUT}$ is low
- Termed “ratio” logic
Review from last time

Other CMOS Logic Families

- $V_{TD} < 0$
  - Low swing is reduced
  - Static Power Dissipation Large when $V_{OUT}$ is low
  - Very economical process
  - Termed “ratio” logic
  - Compact layout (no wells !)
  - Dominant MOS logic until about 1985
  - Depletion device not available in most processes today
Switch-level model of Static CMOS inverter (neglecting diffusion parasitics)
Review from last time

**Propagation Delay in Static CMOS Family**

Since operating in triode through most of transition:

\[
I_D \approx \frac{\mu C_{OX} W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} \approx \frac{\mu C_{OX} W}{L} (V_{GS} - V_T) V_{DS}
\]

\[
R_{PD} = \frac{L_1}{\mu_n C_{OX} W (V_{DD} - V_{TN})}
\]

\[
I_b = \frac{\mu C_{OX} W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} \approx \frac{\mu C_{OX} W}{L} (V_{GS} - V_T) V_{DS}
\]

\[
R_{PU} = \frac{L_2}{\mu_p C_{OX} W (V_{DD} + V_{TP})}
\]

\[
C_{IN} = C_{OX} \left( W_1 L_1 + W_2 L_2 \right)
\]
Review from last time

**Propagation Delay in Static CMOS Family**

For HL output transition, $C_L$ charged to $V_{DD}$

$t_{LH} \cong t_2 = R_{PU} C_L$

Summary:

$t_{LH} \cong R_{PU} C_L$

$t_{HL} \cong R_{PD} C_L$
Review from last time

Propagation Delay in Static CMOS Family

In typical process with Minimum-sized $M_1$ and $M_2$:

\[ t_{\text{HL}} \approx R_{PD}C_L \approx 2.5K \times 2fF = 5\text{ps} \]
\[ t_{\text{LH}} \approx R_{PU}C_L \approx 7.5K \times 2fF = 15\text{ps} \]

Note: LH transition is much slower than HL transition
Defn: The Propagation Delay of a gate is defined to be the sum of $t_{HL}$ and $t_{LH}$, that is, $t_{PROP} = t_{HL} + t_{LH}$

$$t_{PROP} = t_{HL} + t_{LH} \approx C_L (R_{PU} + R_{PD})$$

Propagation delay represents a fundamental limit on the speed a gate can be clocked.

For basic two-inverter cascade in static CMOS logic

In typical process with minimum-sized $M_1$ and $M_2$:

$$t_{PROP} = t_{HL} + t_{LH} \approx 20 \text{ } p\text{sec}$$
The propagation delay through k levels of logic is approximately the sum of the individual delays in the same path.
Review from last time

Propagation Delay in Static CMOS Family

Example:

\[ t_{HL} = t_{HL4} + t_{LH3} + t_{HL2} + t_{LH1} \]

\[ t_{LH} = t_{LH4} + t_{HL3} + t_{LH2} + t_{HL1} \]

\[ t_{PROP} = t_{LH} + t_{HL} = (t_{LH4} + t_{HL3} + t_{LH2} + t_{HL1}) + (t_{HL4} + t_{LH3} + t_{HL2} + t_{LH1}) \]

\[ t_{PROP} = t_{LH} + t_{HL} = (t_{LH4} + t_{HL4}) + (t_{HL3} + t_{LH3}) + (t_{LH2} + t_{HL2}) + (t_{LH1} + t_{HL1}) \]

\[ t_{PROP} = t_{PROP4} + t_{PROP3} + t_{PROP2} + t_{PROP1} \]
Review from last time

Propagation Delay in Static CMOS Family

Propagation through \( k \) levels of logic

\[
\begin{align*}
    t_{HL} & = t_{HLk} + t_{LH(k-1)} + t_{HL(k-2)} + \cdots + t_{XY1} \\
    t_{LH} & = t_{LHk} + t_{HL(k-1)} + t_{LH(k-2)} + \cdots + t_{YX1}
\end{align*}
\]

where \( x=H \) and \( Y=L \) if \( k \) odd and \( X=L \) and \( Y=h \) if \( k \) even

\[
t_{PROP} = \sum_{i=1}^{k} t_{PROPk}
\]

The propagation delay is dependent upon the capacitive loading and PU/PD capabilities of the logic and can not be obtained until device sizes are known.
Digital Circuit Design

- Hierarchical Design
- Basic Logic Gates
- Properties of Logic Families
- Characterization of CMOS Inverter
- Static CMOS Logic Gates
  - Ratio Logic
- Propagation Delay
  - Simple analytical models
  - Elmore Delay
- Sizing of Gates

• Propagation Delay with Multiple Levels of Logic
• Optimal driving of Large Capacitive Loads
• Power Dissipation in Logic Circuits
• Other Logic Styles
• Array Logic
• Ring Oscillators

- done
- partial
Device Sizing

Strategies?

Degrees of Freedom?

Will consider the inverter first
Device Sizing

- Since not ratio logic, $V_H$ and $V_L$ are independent of device sizes for this inverter

- With $L_1=L_2=L_{\text{min}}$, there are 2 degrees of freedom ($W_1$ and $W_2$)

Sizing Strategies

- Minimum Size

- Fixed $V_{\text{TRIP}}$

- Equal rise-fall times
  (equal worst-case rise and fall times)

- Minimum power dissipation

- Minimum time required to drive a given load

- Minimum input capacitance
Device Sizing

Assume $V_{Tn} = 0.2V_{DD}$, $V_{Tp} = -0.2V_{DD}$, $\mu_n/\mu_p = 3$, $L_1 = L_2 = L_{min}$

**Sizing Strategy:** minimum sized

$W_n = ?, W_p, V_{trip} = ?, t_{HL} = ?, t_{LH} = ?$

$W_1 = W_2 = W_{MIN}$

Also provides minimum input capacitance

$t_{LH}$ is longer than $t_{HL}$

$t_{HL} = R_{PD} C_L$

$t_{LH} = 3 R_{PD} C_L$

$$V_{TRIP} = \frac{(0.2V_{dd}) + (V_{dd} - 0.2V_{dd}) \sqrt{1}}{1 + \sqrt{\frac{1}{3}}} = 0.42V_{dd}$$
Device Sizing

Assume $V_{Tn} = 0.2V_{DD}$, $V_{Tp} = -0.2V_{DD}$, $\mu_n/\mu_p = 3$, $L_1 = L_2 = L_{\text{min}}$

**Sizing strategy: Equal rise and fall times**

$W_n = ?, W_p$, $V_{\text{trip}} = ?, t_{HL} = ?, t_{LH} = ?$

$$R_{PD} = \frac{L_{\text{min}}}{\mu_n C_{OX} W_1(0.8V_{DD})}$$

$$R_{PU} = \frac{L_{\text{min}}}{3\mu_n C_{OX} W_2(0.8V_{DD})}$$
Device Sizing

Assume $V_{Tn} = 0.2V_{DD}$, $V_{Tp} = -0.2V_{DD}$, $\mu_n/\mu_p = 3$, $L_1 = L_2 = L_{\text{min}}$

**Sizing strategy: Equal rise and fall times**

$\frac{t_{\text{LH}}}{t_{\text{HL}}} = \frac{R_{PU}C_{IN}}{R_{PD}C_{IN}} \Rightarrow R_{PU} = R_{PD}$

Thus

$$\frac{L_1}{u_nC_{OX}W_1(V_{DD} - V_{Tn})} = \frac{L_2}{u_pC_{OX}W_2(V_{DD} + V_{Tp})}$$

with $L_1 = L_2$ and $V_{Tp} = -V_{Tn}$ we must have

$$\frac{W_2}{W_1} = \frac{\mu_n}{\mu_p}$$

What about the second degree of freedom?

$V_{\text{TRIP}} = ?$
Device Sizing

Assume $V_{TN} = 0.2V_{DD}$, $V_{TP} = -0.2V_{DD}$, $\mu_n/\mu_p = 3$, $L_1 = L_2 = L_{\text{min}}$

**Sizing strategy: Equal (worst-case) rise and fall times**

$W_n = ?, W_p$, $V_{\text{trip}} = ?, t_{HL} = ?, t_{LH} = ?$

\[
\frac{W_2}{W_1} = \frac{\mu_n}{\mu_p}
\]

\[
V_{\text{TRIP}} = \frac{(V_{TN}) + (V_{DD} + V_{TP})}{\mu_p \frac{W_2}{W_1} \frac{L_1}{L_2}} + \sqrt{1 + \frac{\mu_p \frac{W_2}{W_1} \frac{L_1}{L_2}}{\mu_n \frac{W_1}{W_1} \frac{L_1}{L_2}}} = \frac{0.2V_{DD} + 0.8V_{DD}}{2} = \frac{V_{DD}}{2}
\]

$t_{HL} = t_{LH} = R_{pd}C_L = \frac{L_{\text{min}}}{\mu_n C_{OX} W_{\text{min}} (0.8V_{DD})} C_L$
Device Sizing

Assume $V_{Tn} = 0.2V_{DD}$, $V_{Tp} = -0.2V_{DD}$, $\mu_n/\mu_p = 3$, $L_1 = L_2 = L_{min}$

**Sizing strategy:** Fixed $V_{TRIP} = V_{DD} / 2$

$W_n = ?, W_p$, $V_{trip} = ?, t_{HL} = ?, t_{LH} = ?$
Device Sizing

Assume \( V_{Tn} = 0.2V_{DD}, \ V_{Tp} = -0.2V_{DD}, \ \mu_n/\mu_p = 3, \ L_1 = L_2 = L_{\text{min}} \)

**Sizing strategy:** Fixed \( V_{\text{TRIP}} = V_{DD}/2 \)

\[
W_n = ?, \ W_p, \ V_{\text{trip}} = ?, \ t_{HL} = ?, \ t_{LH} = ?
\]

Set \( V_{\text{TRIP}} = V_{DD}/2 \)

\[
V_{\text{TRIP}} = \left( \frac{0.2V_{dd}}{2} \right) + \left( V_{dd} - 0.2V_{dd} \right) \sqrt{\frac{\mu_p W_2 L_1}{\mu_n W_1 L_2}} - \frac{V_{dd}}{2}
\]

Solving, obtain

\[
\frac{W_2}{W_1} = \frac{\mu_n}{\mu_p}
\]

Observe this is the same sizing as was obtained for equal worst-case rise and fall times so \( t_{HL} = t_{LH} = R_{pd}C_L \)

This is no coincidence and these properties guide the definition of the process parameters provided by the foundry
Device Sizing

Assume $V_{Tn} = 0.2V_{DD}$, $V_{Tp} = -0.2V_{DD}$, $\mu_n/\mu_p = 3$, $L_1 = L_2 = L_{\text{min}}$

Sizing Strategies

- Minimum Size
- Fixed $V_{\text{TRIP}}$
- Equal rise-fall times
  (equal worst-case rise and fall times)
- Minimum power dissipation
- Minimum time required to drive a given load
- Minimum input capacitance
**Device Sizing**

Assume $V_{Tn}=0.2V_{DD}$, $V_{Tp}=-0.2V_{DD}$, $\mu_n/\mu_p=3$, $L_1=L_2=L_{\text{min}}$

### Sizing Strategy Summary

<table>
<thead>
<tr>
<th>Size</th>
<th>Minimum Size</th>
<th>$V_{\text{TRIP}}=V_{DD}/2$</th>
<th>Equal Rise/Fall</th>
</tr>
</thead>
<tbody>
<tr>
<td>$W_n=W_p=W_{\text{min}}$</td>
<td>$W_n=W_{\text{min}}$</td>
<td>$W_n=W_{\text{min}}$</td>
<td>$W_n=W_{\text{min}}$</td>
</tr>
<tr>
<td>$L_p=L_n=L_{\text{min}}$</td>
<td>$W_p=3W_{\text{min}}$</td>
<td>$W_p=3W_{\text{min}}$</td>
<td>$W_p=3W_{\text{min}}$</td>
</tr>
</tbody>
</table>

- $t_{\text{HL}} = R_{pd}C_L$
- $t_{\text{LH}} = 3R_{pd}C_L$
- $t_{\text{PROP}} = 4R_{pd}C_L$
- $V_{\text{trip}} = V_{\text{TRIP}}=0.42V_{DD}$
- $V_{\text{TRIP}}=0.5V_{DD}$
- $V_{\text{TRIP}}=0.5V_{DD}$

• For a fixed load $C_L$, the minimum-sized structure has a higher $t_{\text{PROP}}$ but if the load is another inverter, $C_L$ will also increase so the speed improvements become less apparent.
• This will be investigated later.
Reference Inverter

The reference inverter

Assume \( \mu_n/\mu_p = 3 \)  
\( L_n = L_p = L_{MIN} \)  
\( W_n = W_{MIN}, \ W_p = 3W_n \)

\[ C_{REF} = C_{INREF} = 4C_{OX}W_{MIN}L_{MIN} \]

\[ R_{PDREF} = \frac{L_{MIN}}{\mu_nC_{OX}W_{MIN}(V_{DD} - V_{Tn})} = \frac{L_{MIN}}{0.8V_{DD}} \]

- Have sized the reference inverter with \( W_p/W_n = \mu_n/\mu_p \)
- In standard processes, provides \( V_{TRIP} \approx V_{DD}/2 \) and \( t_{HL} \approx t_{LH} \)
- Any other sizing strategy could have been used for the reference inverter but this is most convenient
The reference inverter pair

Assume \( \frac{\mu_n}{\mu_p} = 3 \)  
\[ L_n = L_p = L_{\text{MIN}} \quad W_n = W_{\text{MIN}}, \quad W_p = 3W_n \]

\[ C_{L1} = C_{\text{REF}} = 4C_{\text{OX}} W_{\text{MIN}} L_{\text{MIN}} \]

\[ t_{\text{REF}} = t_{\text{PROPREF}} = t_{\text{HLREF}} + t_{\text{LHREF}} = 2R_{\text{PDREF}} C_{\text{REF}} \]
Reference Inverter

The reference inverter pair

Assume $\mu_n/\mu_p = 3$ \quad $L_n = L_p = L_{\text{MIN}}$ \quad $W_n = W_{\text{MIN}}$, $W_p = 3W_n$

Summary: parameters defined from reference inverter:

\[
C_{\text{REF}} = 4C_{\text{OX}} W_{\text{MIN}} L_{\text{MIN}}
\]

\[
R_{\text{PDREF}} = \frac{\mu_n C_{\text{OX}} W_{\text{MIN}}}{\left(V_{DD} - V_{Tn}\right)}
\]

\[
t_{\text{REF}} = 2R_{\text{PDREF}} C_{\text{REF}}
\]

\[
C_{\text{REF}} = 4C_{\text{OX}} W_{\text{MIN}} L_{\text{MIN}}
\]
Propagation Delay

How does the propagation delay compare for a minimum-sized strategy to that of an equal rise/fall sizing strategy?

Minimum Sized

\[ W_2 = W_1 = W_{\text{MIN}} \]

Reference Inverter

\[ W_2 = (\mu_n/\mu_p)W_1, \quad W_1 = W_{\text{MIN}} \]

\[ t_{\text{PROP}} = t_{\text{REF}} \]
The minimum-sized inverter pair

\[ C_{\text{REF}} = 4C_{\text{OX}} W_{\text{MIN}} L_{\text{MIN}} \]

\[ C_{L1} = 2C_{\text{OX}} W_{\text{MIN}} L_{\text{MIN}} = 0.5C_{\text{REF}} \]

\[ R_{\text{PDn}} = \frac{L_{\text{MIN}}}{\mu_n C_{\text{OX}} W_{\text{MIN}} (V_{\text{DD}} - V_{Tn})} = R_{\text{PDREF}} \]

\[ V_{Tn} = 2V_{DD} \]

\[ R_{\text{PUP}} = \frac{L_{\text{MIN}}}{\mu_p C_{\text{OX}} W_{\text{MIN}} (V_{\text{DD}} + V_{Tp})} = 3R_{\text{PDREF}} \]

\[ t_{\text{PROP}} = t_{\text{HLREF}} + t_{\text{LHREF}} = R_{\text{PDREF}} \left( 0.5C_{\text{REF}} \right) + 3R_{\text{PDREF}} \left( 0.5C_{\text{REF}} \right) = 2R_{\text{PDREF}} C_{\text{REF}} \]

Thus \( t_{\text{PROP}} = t_{\text{REFF}} \)
Device Sizing

The minimum-sized inverter pair

Assume \( \mu_n/\mu_p = 3 \)  
\( L_n = L_p = L_{MIN} \)  
\( W_n = W_{MIN}, W_p = W_n \)

\[
C_{REF} = 4C_{OX} W_{MIN} L_{MIN}
\]

\[
C_{L1} = 0.5C_{REF} = 2C_{OX} W_{MIN} L_{MIN}
\]

\[
R_{PDREF} = \frac{L_{MIN}}{\mu_n C_{OX} W_{MIN} (V_{DD} - V_{Tn})} = \frac{L_{MIN}}{\mu_n C_{OX} W_{MIN} (0.8V_{DD})}
\]

\[
t_{PROP} = t_{HLREF} + t_{LHREF} = R_{PDREF} \left( 0.5C_{REF} \right) + 3R_{PDREF} \left( 0.5C_{REF} \right) = 2R_{PDREF} C_{REF}
\]

\[
t_{PROP} = t_{REF}
\]
How does the propagation delay compare for a minimum-sized strategy to that of an equal rise/fall sizing strategy?

**Minimum Sized**

\[ W_2 = W_1 = W_{\text{MIN}} \]

\[ t_{\text{PROP}} = t_{\text{REF}} \]

**Reference Inverter**

\[ W_2 = (\mu_n/\mu_p)W_1, \quad W_1 = W_{\text{MIN}} \]

\[ t_{\text{PROP}} = t_{\text{REF}} \]

Even though the \( t_{\text{LH}} \) rise time has been reduced with the equal rise/fall sizing strategy, this was done at the expense of an increase in the total load capacitance that resulted in no net change in propagation delay!
Will consider now the multiple-input gates

Will consider both minimum sizing and equal worst-case rise/fall

Will assume $C_L$ (not shown) = $C_{REF}$

Note: worst-case has been added since fall time in NOR gates or rise time in NAND gates depends upon how many transistors are conducting
Sizing of Multiple-Input Gates

Analysis strategy: Express delays in terms of those of reference inverter

Reference Inverter

\[ C_{\text{REF}} = C_{\text{IN}} = 4C_{\text{OX}} W_{\text{MIN}} L_{\text{MIN}} \]

\[ R_{\text{PDREF}} = \frac{L_{\text{MIN}}}{\mu_n C_{\text{OX}} W_{\text{MIN}} (V_{\text{DD}} - V_{\text{Tn}})} \quad \frac{V_{\text{Tn}}}{V_{\text{DD}}} = \frac{L_{\text{MIN}}}{\mu_n C_{\text{OX}} W_{\text{MIN}} (0.8V_{\text{DD}})} \]

\[ t_{\text{REF}} = t_{\text{HLREF}} + t_{\text{LHREF}} = 2R_{\text{PDREF}} C_{\text{REF}} \]

Assume \( \mu_n/\mu_p = 3 \)

\( W_n = W_{\text{MIN}}, \quad W_p = 3W_{\text{MIN}} \)

In 0.5\( \mu \) proc \( t_{\text{REF}} = 20\text{ps}, \quad C_{\text{REF}} = 4fF, R_{\text{PDREF}} = 2.5K \)

\( L_n = L_p = L_{\text{MIN}} \)
Device Sizing

Multiple Input Gates:

2-input NOR

Equal Worst Case Rise/Fall (and equal to that of ref inverter when driving $C_{REF}$)

Wn=?
Wp=?

Fastest response = ?
Input capacitance = ?

Minimum Sized (assume driving a load of $C_{REF}$)

Wn=Wmin
Wp=Wmin

Fastest response = ?
Slowest response = ?
Input capacitance = ?
Device Sizing

Multiple Input Gates:

2-input NOR

DERIVATIONS
Device Sizing

Multiple Input Gates:

k-input NOR (determine same characteristics as for 2-input NOR)

DERIVATIONS
Device Sizing

Multiple Input Gates:

2-input NAND  (determine same characteristics as for 2-input NOR)

DERIVATIONS
Device Sizing

Multiple Input Gates:

k-input NAND  (determine same characteristics as for 2-input NOR)
Device Sizing

Multiple Input Gates:

Comparison of NAND and NOR Gates

DERIVATIONS
Device Sizing

Equal Worse-Case Rise/Fall Device Sizing Strategy
-- (same as $V_{TRIP} = V_{DD}/2$ in typical process considered in example)
Assume $\mu_n/\mu_p = 3$ \hspace{1em} $L_n = L_p = L_{MIN}$

INV
$W_n = W_{MIN}$, $W_p = 3W_{MIN}$
$C_{IN} = C_{REF}$

k-input NOR
$W_n = W_{MIN}$, $W_p = 3kW_{MIN}$
$C_{IN} = \left(\frac{3k+1}{4}\right)C_{REF}$

k-input NOR
$W_n = kW_{MIN}$, $W_p = 3W_{MIN}$
$C_{IN} = \left(\frac{3+k}{4}\right)C_{REF}$
Device Sizing

$C_{\text{IN}}$ for $N_{\text{AND}}$ gates is considerably smaller than for NOR gates for equal worst-case rise and fall times.

$C_{\text{IN}}$ for minimum-sized structures is independent of number of inputs and much smaller than $C_{\text{IN}}$ for the equal rise/fall time case.

$R_{\text{PU}}$ gets very large for minimum-sized NOR gate.
Propagation Delay in Multiple-Levels of Logic with Stage Loading

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