Digital Circuits

Characterization of CMOS Inverter
Static CMOS Logic Gates
Digital Circuit Design

- Hierarchical Design
- Basic Logic Gates
- Properties of Logic Families
- Characterization of CMOS Inverter

- Static CMOS Logic Gates
  - Ratio Logic

- Propagation Delay
  - Simple analytical models
  - Elmore Delay

- Sizing of Gates

- Propagation Delay with Multiple Levels of Logic
- Optimal driving of Large Capacitive Loads
- Power Dissipation in Logic Circuits
- Other Logic Styles
- Array Logic
- Ring Oscillators
The basic logic gates

It suffices to characterize the inverter of a logic family and then express the performance of other gates in that family in terms of the performance of the inverter.

What characteristics are required and desirable for an inverter to form the basis for a useful logic family?
Transfer characteristics of the static CMOS inverter

Review from last time:
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

Case 3  $M_1$ sat, $M_2$ sat

$$V_{IN} = \frac{V_Tn \sqrt{\frac{\mu_n C_{Ox} W_1}{2 L_1}} + V_{DD} + V_{Tp} \sqrt{\frac{\mu_p C_{Oxp} W_2}{2 L_2}}}{\sqrt{\frac{\mu_n C_{Ox} W_1}{2 L_1}} + \sqrt{\frac{\mu_p C_{Oxp} W_2}{2 L_2}}}$$

Since $C_{Ox} = C_{Oxp} = C_{ox}$ this can be simplified to:

$$V_{IN} = \frac{V_{Tn} \sqrt{\frac{W_1}{L_1}} + V_{DD} + V_{Tp} \sqrt{\frac{\mu_p W_2}{\mu_n L_2}}}{\sqrt{\frac{W_1}{L_1}} + \sqrt{\frac{\mu_p W_2}{\mu_n L_2}}}$$

valid for:

$$V_{GS1} \geq V_{Tn} \quad V_{DS1} \geq V_{GS1} - V_{Tn} \quad V_{GS2} \leq V_{Tp} \quad V_{DS2} \leq V_{GS2} - V_{T2}$$

thus, valid for:

$$V_{IN} \geq V_{Tn} \quad V_{OUT} \geq V_{IN} - V_{Tn} \quad V_{IN} - V_{DD} \leq V_{Tp} \quad V_{OUT} - V_{DD} \leq V_{IN} - V_{DD} - V_{Tp}$$
Transfer characteristics of the static CMOS inverter
(Neglect \( \lambda \) effects)

Case 3  \( M_1 \) sat, \( M_2 \) sat

Review from last time:
Review from last time:

Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

Case 3 $M_1$ sat, $M_2$ sat
Review from last time:
Transfer characteristics of the static CMOS inverter
(Neglect \( \lambda \) effects)

Partial solution:
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

Review from last time:
Review from last time:

Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)
Transfer characteristics of the static CMOS inverter

(Neglect $\lambda$ effects)

From Case 3 analysis:

$$V_{IN} = V_{Tn} + V_{DD} + V_{Tp} \left( \frac{\mu_p W_2 L_1}{\mu_n W_1 L_2} \right)$$

$$1 + \sqrt{\frac{\mu_p W_2 L_1}{\mu_n W_1 L_2}}$$
Inverter Transfer Characteristics of Inverter Pair

\[ V_{\text{IN}} \rightarrow \quad \text{Inverter Pair} \rightarrow \quad V'_{\text{OUT}} \]

What are \( V_H \) and \( V_L \)?

Find the points on the inverter pair transfer characteristics where \( V'_{\text{OUT}} = V_{\text{IN}} \) and the slope is less than 1.
Inverter Transfer Characteristics of Inverter Pair for THIS Logic Family

\[ V_{IN} \rightarrow \text{V'OUT} \rightarrow V_{OUT} \]

\[ V_H = V_{DD} \text{ and } V_L = 0 \]

Note this is independent of device sizing for THIS logic family!!
Sizing of the Basic CMOS Inverter

The characteristic that device sizes do not need to be used to establish $V_H$ and $V_L$ logic levels is a major advantage of this type of logic.

How should $M_1$ and $M_2$ be sized?

How many degrees of freedom are there in the design of the inverter?
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How many degrees of freedom are there in the design of the inverter?

\[ \{ W_1, W_2, L_1, L_2 \} \]  

4 degrees of freedom

But in basic device model and in most performance metrics, $W_1/L_1$ and $W_2/L_2$ appear as ratios

\[ \{ W_1/L_1, W_2/L_2 \} \]  
effectively 2 degrees of freedom
How should $M_1$ and $M_2$ be sized?

$\{ W_1, W_2, L_1, L_2 \}$  
4 degrees of freedom  
Usually pick $L_1 = L_2 = L_{\text{min}}$

$\{ W_1/L_1, W_2/L_2 \}$  
effectively 2 degrees of freedom

How are $W_1$ and $W_2$ chosen?

Depends upon what performance parameters are most important for a given application!
How should $M_1$ and $M_2$ be sized?

Usually pick $L_1=L_2=L_{\text{min}}$

\[
\{ \frac{W_1}{L_1}, \frac{W_2}{L_2} \} \quad \text{2 remaining degrees of freedom}
\]

One popular sizing strategy:

1. Pick $W_1=W_{\text{MIN}}$ to minimize area of $M_1$
2. Pick $W_2$ to set trip-point at $V_{\text{DD}}/2$
How should $M_1$ and $M_2$ be sized?

pick $L_1=L_2=L_{\text{min}}$

One popular sizing strategy:
1. Pick $W_1=W_{\text{MIN}}$ to minimize area of $M_1$
2. Pick $W_2$ to set trip-point at $V_{DD}/2$

Observe Case 3 provides expression for $V_{\text{TRIP}}$

Thus, at the trip point,

$$V_{\text{OUT}} = V_{\text{IN}} = V_{\text{TRIP}} = V_{Tn} + V_{DD} + V_{Tp} \sqrt{\frac{\mu_p}{\mu_n} \frac{W_2}{W_1} \frac{L_1}{L_2}} \sqrt{1 + \frac{\mu_p}{\mu_n} \frac{W_2}{W_1} \frac{L_1}{L_2}}$$
How should \( M_1 \) and \( M_2 \) be sized?

pick \( L_1 = L_2 = L_{\text{min}} \)

One popular sizing strategy:
1. Pick \( W_1 = W_{\text{MIN}} \) to minimize area of \( M_1 \)
2. Pick \( W_2 \) to set trip-point at \( V_{DD}/2 \)

Typically \( V_{Tn} = 0.2V_{DD} \), \( |V_{Tp}| = 0.2V_{DD} \)

\[
V_{\text{TRIP}} = \frac{V_{Tn} + V_{DD} + V_{Tp} \sqrt{\frac{\mu_p}{\mu_n} \frac{W_2}{W_1} \frac{L_1}{L_2}}}{\sqrt{1 + \frac{\mu_p}{\mu_n} \frac{W_2}{W_1} \frac{L_1}{L_2}}}
\]

\[
\therefore \quad \frac{V_{DD}}{2} = \frac{0.2V_{DD} + V_{DD} - 0.2V_{DD} \sqrt{\frac{\mu_p}{\mu_n} \frac{W_2}{W_1}}}{\sqrt{1 + \frac{\mu_p}{\mu_n} \frac{W_2}{W_1}}}
\]

Solving this equation for \( W_2 \), obtain

\[
W_2 = W_1 \left( \frac{\mu_n}{\mu_p} \right)
\]

Other sizing strategies are used as well and will be discussed later!
Extension of Basic CMOS Inverter to Multiple-Input Gates

Performs as a 2-input NOR Gate

Can be easily extended to an n-input NOR Gate
Extension of Basic CMOS Inverter to Multiple-Input Gates

Performs as a 2-input NAND Gate

Can be easily extended to an n-input NAND Gate
Static CMOS Logic Family

Observe PUN is p-channel, PDN is n-channel
Static CMOS Logic Family

n-channel PDN and p-channel PUN
General Logic Family

p-channel PUN
n-channel PDN

Arbitrary PUN and PDN
Other CMOS Logic Families

Enhancement Load NMOS

Enhancement Load Pseudo-NMOS

Depletion Load NMOS
Other CMOS Logic Families

- High and low swings are reduced
- Response time is slow on LH output transitions
- Static Power Dissipation Large when $V_{OUT}$ is low
- Very economical process
- Termed “ratio logic”
- Compact layout (no wells !)

![Diagram of CMOS logic family with symbols and equations: $V_{IN} \rightarrow M_1 \rightarrow V_{OUT}$, $V_{DD} \rightarrow M_2 \rightarrow V_{OUT}$, with $V_{DD}$, $V_{OUT}$, and $V_{IN}$ as inputs, and $V_{DD} - V_{Tn}$ as output voltage swing.](image-url)
Other CMOS Logic Families

- Multiple-input gates require single transistor for each additional input

- Still useful if many inputs are required (static power does not increase with k
Other CMOS Logic Families

- High and low swings are reduced
- Response time is slow on LH output transitions
- Static Power Dissipation Large when \( V_{OUT} \) is low
- Termed “ratio” logic
Other CMOS Logic Families

- Depletion Load NMOS
- $V_{TD} < 0$
  - Low swing is reduced
  - Static Power Dissipation Large when $V_{OUT}$ is low
  - Very economical process
  - Termed “ratio” logic
  - Compact layout (no wells !)
  - Dominant MOS logic until about 1985
  - Depletion device not available in most processes today
Other CMOS Logic Families

• Reduced $V_H - V_L$
• Device sizing critical for even basic operation
• Shallow slope at $V_{TRIP}$
Other CMOS Logic Families

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Other CMOS Logic Families

- Reduced $V_{H}-V_{L}$
- Device sizing critical for even basic operation
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Static Power Dissipation in Static CMOS Family

When $V_{OUT}$ is Low, $I_{D1}=0$

When $V_{OUT}$ is High, $I_{D2}=0$

Thus, $P_{STATIC}=0$

This is a key property of the static CMOS Logic Family and is the major reason Static CMOS Logic is so dominant.

It can be shown that this zero static power dissipation property can be preserved if the PUN is comprised of n-channel devices, the PDN is comprised of n-channel devices and they are never both driven into the conducting states at the same time.
Static Power Dissipation in Ratio Logic Families

Example: Assume $V_{DD}=5V$
$V_T=1V$, $\mu C_{OX}=10^{-4}A/V^2$, $W_1/L_1=1$ and $M_2$ sized so that $V_L=V_{Tn}$

Observe:

$V_H=V_{DD}-V_T$  
If $V_{IN}=V_H$, $V_{OUT}=V_L$ so

$$I_{D1} = \frac{\mu C_{OX} W_1}{L_1} \left( V_{GS1} - V_T - \frac{V_{DS1}}{2} \right) V_{DS1}$$

$$I_{D1} = 10^{-4} \left( 5 - 1 - 1 - \frac{1}{2} \right) \cdot 1 = 0.25mA$$

$$P_L=(5V)(0.25mA)=1.25mW$$
Static Power Dissipation in Ratio Logic Families

Example:

Assume $V_{DD}=5V$, $V_T=1V$, $\mu C_{OX}=10^{-4} A/V^2$, $W_1/L_1=1$ and $M_2$ sized so that $V_L=V_T$.

$$P_L=(5V)(0.25mA)=1.25mW$$

If a circuit has 100,000 gates and half of them are in the $V_{OUT}=V_L$ state, the static power dissipation will be...
Static Power Dissipation in Ratio Logic Families

Example: Assume $V_{DD}=5V$, $V_T=1V$, $\mu C_{OX}=10^{-4}A/V^2$, $W_1/L_1=1$ and $M_2$ sized so that $V_L=V_{Tn}$

$$P_L=(5V)(0.25mA)=1.25mW$$

If a circuit has 100,000 gates and half of them are in the $V_{OUT}=V_L$ state, the static power dissipation will be

$$P_{STATIC} = \frac{1}{2} \cdot 10^5 \cdot 1.25 \, mW = 62.5\,W$$

This power dissipation is way too high and would be even larger in circuits with 100 million or more gates – the level of integration common in SoC circuits today.
Propagation Delay in Static CMOS Family

Switch-level model of Static CMOS inverter (neglecting diffusion parasitics)
Switch-level model of Static CMOS inverter (neglecting diffusion parasitics)
Propagation Delay in Static CMOS Family

Since operating in triode through most of transition:

\[ I_D = \frac{\mu C_{ox} W}{L} \left( V_{gs} - V_T - \frac{V_{ds}}{2} \right) V_{ds} = \frac{\mu C_{ox} W}{L} \left( V_{gs} - V_T \right) \]

\[ R_{PD} = \frac{L_1}{\mu n C_{ox} W_1} \left( V_{DD} - V_{Tn} \right) \]

\[ I_D = \frac{\mu C_{ox} W}{L} \left( V_{gs} - V_T + \frac{V_{ds}}{2} \right) V_{ds} = \frac{\mu C_{ox} W}{L} \left( V_{gs} - V_T \right) \]

\[ R_{PU} = \frac{L_2}{\mu p C_{ox} W_2} \left( V_{DD} + V_{Tp} \right) \]

\[ C_{IN} = C_{ox} \left( W_1 L_1 + W_2 L_2 \right) \]
Propagations Delay in Static CMOS Family

If $u_n C_{OX} = 100 \mu A V^{-2}$, $C_{OX} = 4 \text{ fF} \mu^{-2}$, $V_{TN} = V_{DD}/5$, $V_{TP} = -V_{DD}/5$, $\mu_n/\mu_p = 3$, $L_1 = W_1 = L_{MIN}$, $L_2 = W_2 = L_{MIN}$, $L_{MIN} = 0.5 \mu$ and $V_{DD} = 5V$

$$R_{PD} = \frac{1}{10^{-4} \cdot 0.8V_{DD}} = 2.5K \Omega$$

$$C_{IN} = 4 \cdot 10^{-15} \cdot 2L_{MIN}^2 = 2\text{fF}$$

$$R_{PU} = \frac{1}{10^{-4} \cdot \frac{1}{3} \cdot 0.8V_{DD}} = 7.5K \Omega$$

Example: Minimum-sized $M_1$ and $M_2$
In typical process with Minimum-sized $M_1$ and $M_2$:

- $R_{PD} \approx 2.5 \text{K}\Omega$
- $R_{PU} \approx 3R_{PD} = 7.5 \text{K}\Omega$
- $C_{IN} \approx 2 \text{fF}$
Propagation Delay in Static CMOS Family

In typical process with Minimum-sized M₁ and M₂:

\( R_{PD} \approx 2.5\, \Omega \)
\( R_{PU} \approx 3R_{PD} = 7.5\, \Omega \)
\( C_{IN} \approx 2\, fF \)

How long does it take for a signal to propagate from x to z?
Propagation Delay in Static CMOS Family

Consider:

For HL output transition, \( C_L \) charged to \( V_{DD} \)

Ideally:

\[
V_{IN} \quad V_{OUT} \\
V_{DD} \\
C_L
\]
Propagation Delay in Static CMOS Family

For HL output transition, $C_L$ charged to $V_{DD}$

What is the transition time $t_{HL}$?
Propagation Delay in Static CMOS Family

\[ V_{IN} \quad \rightarrow \quad V_{OUT} \quad C_L \]

\[ V_{IN} \quad \rightarrow \quad V_{DD} \quad R_{PU} \quad \Rightarrow \quad V_G \quad \overline{V_G} \quad \rightarrow \quad V_{OUT} \]

\[ V_{IN} \quad \rightarrow \quad R_{PD} \quad \Rightarrow \quad V_G \quad \overline{V_G} \quad \rightarrow \quad V_{OUT} \quad C_L \]
Propagation Delay in Static CMOS Family

For HL output transition, $C_L$ charged to $V_{DD}$

For HL output transition, $C_L$ charged to $V_{DD}$

\[ V_{OUT} \]

\[ V_{IN} \]

\[ V_{DD} \]

\[ V_{DD} \]

\[ e^{-1}V_{DD} \]

\[ t=0 \]

\[ t_1 \]

\[ V_{OUT} \leftarrow F + \leftarrow F e^{-\frac{t}{r}} = 0 + \leftarrow V_{DD} - 0 e^{-\frac{t}{R_{PD}C_L}} \]

\[ \frac{V_{DD}}{e} = V_{DD} e^{-\frac{t_1}{R_{PD}C_L}} \]

If $V_{TRIP}$ is close to $V_{DD}/2$, $t_{HL}$ is close to $t_1$
Propagation Delay in Static CMOS Family

For HL output transition, \( C_L \) charged to \( V_{DD} \)

\[
\begin{align*}
V_{IN} & \quad \rightarrow \quad V_{OUT} \\
C_L & \quad \downarrow
\end{align*}
\]

\[
V_{IN} \quad V_{OUT} \quad C_L
\]

\[
V_{DD} \quad t=0
\]

\[
(1-e^{-1})V_{DD} \quad V_{TRIP} \quad V_{OUT} \quad t=0 \quad t \quad t_2
\]

\[
t_{LH} \approx t_2 = R_{PU} C_L
\]

Summary:

\[
\begin{align*}
t_{LH} & \approx R_{PU} C_L \\
t_{HL} & \approx R_{PD} C_L
\end{align*}
\]
Propagation Delay in Static CMOS Family

In typical process with Minimum-sized $M_1$ and $M_2$:

$$t_{HL} \approx R_{PD}C_L \approx 2.5k\Omega \cdot 2fF = 5\text{ps}$$

$$t_{LH} \approx R_{PU}C_L \approx 7.5k\Omega \cdot 2fF = 15\text{ps}$$

Note: LH transition is much slower than HL transition
Propagation Delay in Static CMOS Family

Defn: The Propagation Delay of a gate is defined to be the sum of $t_{HL}$ and $t_{LH}$, that is, $t_{PROP} = t_{HL} + t_{LH}$

$$t_{PROP} = t_{HL} + t_{LH} \approx C_L \times R_{PU} + R_{PD}$$

Propagation delay represents a fundamental limit on the speed a gate can be clocked.

For basic two-inverter cascade in static CMOS logic

![Diagram of two-inverter cascade]

In typical process with minimum-sized $M_1$ and $M_2$:

$$t_{PROP} = t_{HL} + t_{LH} \approx 20 \text{ p sec}$$
Propagation Delay in Static CMOS Family

The propagation delay through $k$ levels of logic is approximately the sum of the individual delays in the same path.
Propagation Delay in Static CMOS Family

Example:

\[ t_{HL} = t_{HL4} + t_{HL3} + t_{HL2} + t_{LH1} \]

\[ t_{LH} = t_{LH4} + t_{HL3} + t_{LH2} + t_{HL1} \]

\[ t_{PROP} = t_{LH} + t_{HL} = (t_{LH4} + t_{HL3} + t_{LH2} + t_{HL1}) + (t_{HL4} + t_{LH3} + t_{HL2} + t_{LH1}) \]

\[ t_{PROP} = t_{LH} + t_{HL} = (t_{LH4} + t_{HL4}) + (t_{LH3} + t_{HL3}) + (t_{LH2} + t_{HL2}) + (t_{LH1} + t_{HL1}) \]

\[ t_{PROP} = t_{PROP4} + t_{PROP3} + t_{PROP2} + t_{PROP1} \]
Propagation Delay in Static CMOS Family

Propagation through $k$ levels of logic

\[ t_{HL} = t_{HLk} + t_{LH(k-1)} + t_{HL(k-2)} + \cdots + t_{XY1} \]

\[ t_{LH} = t_{LHk} + t_{HL(k-1)} + t_{LH(k-2)} + \cdots + t_{YX1} \]

where $x=H$ and $Y=L$ if $k$ odd and $X=L$ and $Y=h$ if $k$ even

\[ t_{PROP} = \sum_{i=1}^{k} t_{PROP_k} \]
End of Lecture 37