Digital Circuits

Other Logic Families
  Static Power Dissipation
  Propagation Delay – basic characterization
  Device Sizing (Inverter and multiple-input gates)
**Review from Last Time**

**Inverter Transfer Characteristics of Inverter Pair for THIS Logic Family**

- $V_{IN}$
- $V'_{OUT}$

- $V_H = V_{DD}$ and $V_L = 0$

Note this is independent of device sizing for THIS logic family!!
Sizing of the Basic CMOS Inverter

How should $M_1$ and $M_2$ be sized?

How many degrees of freedom are there in the design of the inverter?

The characteristic that device sizes do not need to be used to establish $V_H$ and $V_L$ logic levels is a major advantage of this type of logic.
How should $M_1$ and $M_2$ be sized?

pick $L_1 = L_2 = L_{\text{min}}$

One popular sizing strategy:
1. Pick $W_1 = W_{\text{MIN}}$ to minimize area of $M_1$
2. Pick $W_2$ to set trip-point at $V_{DD}/2$

Typically $V_{Tn} = 0.2V_{DD}$, $|V_{Tp}| = 0.2V_{DD}$

$$V_{TRIP} = \frac{(V_{Tn}) + (V_{DD} + V_{Tp}) \sqrt{\frac{\mu_p}{\mu_n}} \frac{W_2}{W_1} L_1}{1 + \sqrt{\frac{\mu_p}{\mu_n}} \frac{W_2}{W_1} L_2}$$

Solving this equation for $W_2$, obtain

$$W_2 = W_1 \left( \frac{\mu_n}{\mu_p} \right)$$

Other sizing strategies are used as well and will be discussed later!
Other MOS Logic Families

Review from Last Time

Enhancement Load NMOS

Enhancement Load Pseudo-NMOS

Depletion Load NMOS
Digital Circuit Design

- Hierarchical Design
- Basic Logic Gates
- Properties of Logic Families
- Characterization of CMOS Inverter
- Static CMOS Logic Gates
  - Ratio Logic
  - Propagation Delay
    - Simple analytical models
    - Elmore Delay
- Sizing of Gates
- Propagation Delay with Multiple Levels of Logic
- Optimal driving of Large Capacitive Loads
- Power Dissipation in Logic Circuits
- Other Logic Styles
- Array Logic
- Ring Oscillators

---

done

partial
Question:

Why is $|V_{T_p}| \approx V_{T_n} \approx V_{DD}/5$ in many processes?
Other CMOS/MOS Logic Families

![Diagram of CMOS/MOS Logic Family](image)

- **V\text{IN}**
- **V\text{OUT}**
- **V\text{DD}**
- **M\text{1}**
- **M\text{2}**
- Enhancement Load NMOS

Graph:

- **V\text{OUT}**
- **V\text{DD}**
- **V\text{DD} - V\text{Tn}**

Graphical representation of the CMOS/MOS Logic Family circuit and its output characteristics.
NMOS example

Enhancement Load NMOS

V_th | W1/L1 | W2/L2 | VDD
--- | --- | --- | ---
1 | 4 | 1 | 5

File: Inv Char.xls
NMOS example

$V_H = 4V$
$V_L = 0.55V$
$V_{TRIP} = 2V$
Other CMOS/MOS Logic Families

- High and low swings are reduced 😞
- Response time is slow on LH output transitions 😞
- Static Power Dissipation Large when $V_{OUT}$ is low 😞
- Very economical process 😊
- Termed “ratio logic” (because logic values dependent on device dimensions – DOF!) 😊
- May not work for some device sizes 😞
- Compact layout (no wells !) 😊
Other CMOS/MOS Logic Families

- Multiple-input gates require single transistor for each additional input
- Still useful if many inputs are required (static power does not increase with $k$)
Other CMOS/MOS Logic Families

- High and low swings are reduced
- Response time is slow on LH output transitions
- Static Power Dissipation Large when $V_{OUT}$ is low
- Multiple-input gates require single transistor for each additional input
- Termed “ratio” logic
Other CMOS/MOS Logic Families

- Depletion Load NMOS

\[ V_{IN} \rightarrow M_1 \rightarrow M_2 \rightarrow V_{OUT} \rightarrow V_{DD} \]

- \( V_{TD} < 0 \)

- Low swing is reduced
- Static Power Dissipation Large when \( V_{OUT} \) is low
- Very economical process
- Termed “ratio” logic
- Compact layout (no wells !)
- Response time slow on L-H output transitions
- Dominant MOS logic until about 1985
- Depletion device not available in most processes today
Other CMOS/MOS Logic Families

- Reduced $V_H - V_L$
- Device sizing critical for even basic operation
- Shallow slope at $V_{TRIP}$
Other CMOS/MOS Logic Families

• Reduced $V_H - V_L$
• Device sizing critical for even basic operation (DOF)
• Shallow slope at $V_{TRIP}$
Other CMOS/MOS Logic Families

- Reduced $V_H-V_L$
- Device sizing critical for even basic operation
- Shallow slope at $V_{TRIP}$
Other CMOS/MOS Logic Families

- Reduced $V_H - V_L$
- Device sizing critical for even basic operation
- Shallow slope at $V_{TRIP}$
Static Power Dissipation in Static CMOS Family

When \( V_{OUT} \) is Low, \( I_{D1} = 0 \)

When \( V_{OUT} \) is High, \( I_{D2} = 0 \)

Thus, \( P_{STATIC} = 0 \)

This is a key property of the static CMOS Logic Family and is the major reason Static CMOS Logic is so dominant

It can be shown that this zero static power dissipation property can be preserved if the PUN is comprised of p-channel devices, the PDN is comprised of n-channel devices and they are never both driven into the conducting states at the same time

Compound Gate in CMOS Process
Static Power Dissipation in Ratio Logic Families

Example:

Assume $V_{DD}=5V$

$V_T=1V$, $\mu C_{OX}=10^{-4} A/V^2$, $W_1/L_1=1$ and $M_2$ sized so that $V_L=V_{Tn}$

Observe:

$V_H=V_{DD}-V_{Tn}$

If $V_{IN}=V_H$, $V_{OUT}=V_L$ so

$I_{D1} = \frac{\mu C_{OX} W_1}{L_1} \left( V_{GS1} - V_T - \frac{V_{DS1}}{2} \right) V_{DS1}$

$I_{D1} = 10^{-4} \left( 5 - 1 - 1 - \frac{1}{2} \right) \cdot 1 = 0.25mA$

$P_L=(5V)(0.25mA)=1.25mW$
Static Power Dissipation in Ratio Logic Families

Example: Assume $V_{DD}=5V$
$V_T=1V$, $\mu C_{OX}=10^{-4}A/V^2$, $W_1/L_1=1$ and $M_2$ sized so that $V_L=V_{Tn}$

\[
P_L = (5V)(0.25mA) = 1.25mW
\]

If a circuit has 100,000 gates and half of them are in the $V_{OUT}=V_L$ state, the static power dissipation will be
Static Power Dissipation in Ratio Logic Families

Example: Assume $V_{DD}=5V$
$V_T=1V$, $\mu COX=10^{-4} A/V^2$, $W_1/L_1=1$ and $M_2$ sized so that $V_L=V_{Tn}$

$$P_L=(5V)(0.25mA)=1.25mW$$

If a circuit has 100,000 gates and half of them are in the $V_{OUT}=V_L$ state, the static power dissipation will be

$$P_{STATIC} = \frac{1}{2} 10^5 \cdot 1.25mW = 62.5W$$

This power dissipation is way too high and would be even larger in circuits with 100 million or more gates – the level of integration common in SoC circuits today.
Switch-level model of Static CMOS inverter (neglecting diffusion parasitics)
Propagation Delay in Static CMOS Family

Switch-level model of Static CMOS inverter (neglecting diffusion parasitics)
Since operating in triode through most of transition:

\[
I_D \approx \frac{\mu C_{OX} W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} \approx \frac{\mu C_{OX} W}{L} (V_{GS} - V_T) V_{DS}
\]

\[
R_{PD} = \frac{V_{DS}}{I_D} = \frac{L_1}{\mu_n C_{OX} W_1 (V_{DD} - V_{Tn})}
\]

\[
I_d = \frac{\mu C_{OX} W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} \approx \frac{\mu C_{OX} W}{L} (V_{GS} - V_T) V_{DS}
\]

\[
R_{PU} = \frac{V_{DS}}{I_D} = \frac{L_2}{\mu_p C_{OX} W_2 (V_{DD} + V_{Tp})}
\]

\[
C_{IN} = C_{OX} \left( W_1 L_1 + W_2 L_2 \right)
\]
Propagación del Retraso en la Familia de CMOS estático

\( R_{PD} = \frac{L_1}{\mu_n C_{OX} W_1 (V_{DD} - V_{Tn})} \)

\( R_{PU} = \frac{L_2}{\mu_p C_{OX} W_2 (V_{DD} + V_{TP})} \)

\( C_{IN} = C_{OX} (W_1 L_1 + W_2 L_2) \)

Ejemplo: Pequeñas dimensiones de \( M_1 \) y \( M_2 \)

Si \( \mu_n C_{OX} = 100 \mu A V^{-2}, C_{OX} = 4 \ fF \mu^{-2}, V_{Tn} = V_{DD}/5, V_{TP} = -V_{DD}/5, \mu_n / \mu_p = 3, L_1 = W_1 = L_{MIN}, L_2 = W_2 = L_{MIN}, L_{MIN} = 0.5 \mu \) y \( V_{DD} = 5 \ V \)

(Note: Este \( C_{OX} \) es somewhat larger than that in the 0.5u ON process)

\( R_{PD} = \frac{1}{10^{-4} \cdot 0.8 V_{DD}} = 2.5 K \Omega \)

\( C_{IN} = 4 \cdot 10^{-15} \cdot 2 L_{MIN}^2 = 2 fF \)

\( R_{PU} = \frac{1}{10^{-4} \cdot \frac{1}{3} \cdot 0.8 V_{DD}} = 7.5 K \Omega \)
Propagation Delay in Static CMOS Family

In typical process with Minimum-sized M₁ and M₂:
\[ R_{PD} \approx 2.5\, \text{k}\Omega \]
\[ R_{PU} \approx 3R_{PD} = 7.5\, \text{k}\Omega \]
\[ C_{IN} \approx 2\, \text{fF} \]
Propagation Delay in Static CMOS Family

How long does it take for a signal to propagate from x to y?

In typical process with Minimum-sized M₁ and M₂:

\[ R_{PD} \approx 2.5 \text{KΩ} \]
\[ R_{PU} \approx 3R_{PD} = 7.5 \text{KΩ} \]
\[ C_{IN} \approx 2 \text{fF} \]
Consider:

For HL output transition, \( C_L \) charged to \( V_{DD} \)

Ideally:
Propagation Delay in Static CMOS Family

For HL output transition, $C_L$ charged to $V_{DD}$

Actually:

What is the transition time $t_{HL}$?
Propagation Delay in Static CMOS Family
Propagation Delay in Static CMOS Family

For HL output transition, $C_L$ charged to $V_{DD}$

$$V_{IN} \rightarrow V_{OUT} \Rightarrow V_{IN} \rightarrow V_{OUT} \Rightarrow \frac{V_{IN}}{C_L}$$

$$V_{DD}$$

$$V_{OUT}(t) = F + (1-F)e^{-\frac{t}{\tau}} = 0 + (V_{DD} - 0)e^{-\frac{t}{R_{PD}C_L}}$$

$$\frac{V_{DD}}{e} = V_{DD}e^{-\frac{t_1}{R_{PD}C_L}} \quad \Rightarrow \quad t_1 = R_{PD}C_L$$

If $V_{TRIP}$ is close to $V_{DD}/2$, $t_{HL}$ is close to $t_1$
Propagación de Retraso en la Familia de CMOS Estático

Para la transición de salida de HL, la carga en CL se convierte a VDD.

Para la transición de salida de LH, la carga en CL se convierte a VDD.

**Summary:**

\[ t_{LH} \approx t_2 = R_{PU} C_L \]

\[ t_{HL} \approx R_{PD} C_L \]

Para \( V_{TRIP} \) cercano a \( V_{DD}/2 \)
Propagation Delay in Static CMOS Family

In typical process with Minimum-sized $M_1$ and $M_2$:

$$t_{HL} \approx R_{PD}C_L \approx 2.5K \cdot 2fF = 5ps$$

$$t_{LH} \approx R_{PU}C_L \approx 7.5K \cdot 2fF = 15ps$$

(Note: This $C_{OX}$ is somewhat larger than that in the 0.5u ON process)

Note: LH transition is much slower than HL transition
Propagation Delay in Static CMOS Family

Defn: The Propagation Delay of a gate is defined to be the sum of $t_{HL}$ and $t_{LH}$, that is, $t_{PROP} = t_{HL} + t_{LH}$

$$t_{PROP} = t_{HL} + t_{LH} \approx C_L (R_{PU} + R_{PD})$$

Propagation delay represents a fundamental limit on the speed a gate can be clocked

For basic two-inverter cascade in static CMOS logic

In typical process with minimum-sized $M_1$ and $M_2$:

$$t_{PROP} = t_{HL} + t_{LH} \approx 20 \mu s$$
The propagation delay through $k$ levels of logic is approximately the sum of the individual delays in the same path.
Propagation Delay in Static CMOS Family

Example:

\[ t_{HL} = t_{HL4} + t_{LH3} + t_{HL2} + t_{LH1} \]

\[ t_{LH} = t_{LH4} + t_{HL3} + t_{LH2} + t_{HL1} \]

\[ t_{PROP} = t_{LH} + t_{HL} = (t_{LH4} + t_{HL3} + t_{LH2} + t_{HL1}) + (t_{HL4} + t_{LH3} + t_{HL2} + t_{LH1}) \]

\[ t_{PROP} = t_{LH} + t_{HL} = (t_{LH4} + t_{HL4}) + (t_{LH3} + t_{HL3}) + (t_{LH2} + t_{HL2}) + (t_{LH1} + t_{HL1}) \]

\[ t_{PROP} = t_{PROP4} + t_{PROP3} + t_{PROP2} + t_{PROP1} \]
Propagation Delay in Static CMOS Family

Propagation through k levels of logic

\[ t_{HL} \approx t_{HLk} + t_{LH(k-1)} + t_{HL(k-2)} + \cdots + t_{XY1} \]

\[ t_{LH} \approx t_{LHk} + t_{HL(k-1)} + t_{LH(k-2)} + \cdots + t_{YX1} \]

where \( x=H \) and \( Y=L \) if \( k \) odd and \( X=L \) and \( Y=h \) if \( k \) even

\[ t_{PROP} = \sum_{i=1}^{k} t_{PROP_i} \]

Will return to propagation delay after we discuss device sizing
End of Lecture 37