EE 330
Lecture 37

Digital Circuits

Other Logic Families
Static Power Dissipation
Propagation Delay – basic characterization
Device Sizing (Inverter and multiple-input gates)
Review from Last Time

Inverter Transfer Characteristics of Inverter Pair for **THIS** Logic Family

\[ V_{IN} \quad \rightarrow \quad V'_{OUT} \quad \rightarrow \quad V_{OUT} \]

\[ V_H = V_{DD} \text{ and } V_L = 0 \]

Note this is independent of device sizing for **THIS** logic family !!
Sizing of the Basic CMOS Inverter

How should $M_1$ and $M_2$ be sized?

How many degrees of freedom are there in the design of the inverter?

The characteristic that device sizes do not need to be used to establish $V_H$ and $V_L$ logic levels is a major advantage of this type of logic.
How should $M_1$ and $M_2$ be sized?

pick $L_1=L_2=L_{\text{min}}$

One popular sizing strategy:
1. Pick $W_1=W_{\text{MIN}}$ to minimize area of $M_1$
2. Pick $W_2$ to set trip-point at $V_{DD}/2$

Typically $V_{Tn}=0.2V_{DD}$, $|V_{Tp}|=0.2V_{DD}$

$$V_{\text{TRIP}} = \frac{(V_{Tn}) + (V_{DD}+V_{Tp}) \sqrt{\frac{\mu_p}{\mu_n}} \frac{W_2}{L_1}}{1 + \sqrt{\frac{\mu_p}{\mu_n}} \frac{W_2}{L_1} \frac{W_2}{L_2}}$$

$$\therefore \frac{V_{DD}}{2} = \frac{(0.2V_{DD}) + (V_{DD}-0.2V_{DD}) \sqrt{\frac{\mu_p}{\mu_n}} \frac{W_2}{L_1}}{1 + \sqrt{\frac{\mu_p}{\mu_n}} \frac{W_2}{L_1} \frac{W_2}{L_2}}$$

Solving this equation for $W_2$, obtain

$$W_2 = W_1 \left( \frac{\mu_n}{\mu_p} \right)$$

Other sizing strategies are used as well and will be discussed later!
Review from Last Time

Static CMOS Logic Family

n-channel PDN and p-channel PUN

$V_H = V_{DD}$, $V_L = 0V$  (same as for inverter!)
Review from Last Time

General Logic Family

Compound Gate in CMOS Process

p-channel PUN
n-channel PDN

$V_H = V_{DD}$, $V_L = 0V$ (same as for inverter!)

Arbitrary PUN and PDN
Other CMOS Logic Families

Review from Last Time
Digital Circuit Design

- Hierarchical Design
- Basic Logic Gates
- Properties of Logic Families
- Characterization of CMOS Inverter
- Static CMOS Logic Gates
  - Ratio Logic
    - Propagation Delay
      - Simple analytical models
      - Elmore Delay
  - Sizing of Gates
- Propagation Delay with Multiple Levels of Logic
- Optimal driving of Large Capacitive Loads
- Power Dissipation in Logic Circuits
- Other Logic Styles
- Array Logic
- Ring Oscillators
Remember Question:

Why is $|V_{Tp}| \approx V_{Tn} \approx V_{DD}/2$ in many processes?
Other CMOS Logic Families

- High and low swings are reduced
- Response time is slow on LH output transitions
- Static Power Dissipation Large when $V_{\text{OUT}}$ is low
- Very economical process
- Termed “ratio logic” (because logic values dependent on device dimensions – DOF!)
- May not work for some device sizes
- Compact layout (no wells !)
Other CMOS Logic Families

Enhancement Load NMOS

- Multiple-input gates require single transistor for each additional input

- Still useful if many inputs are required (static power does not increase with k)
Other CMOS Logic Families

- High and low swings are reduced
- Response time is slow on LH output transitions
- Static Power Dissipation Large when $V_{OUT}$ is low
- Multiple-input gates require single transistor for each additional input
- Termed “ratio” logic
Other CMOS Logic Families

- Low swing is reduced
- Static Power Dissipation Large when $V_{\text{OUT}}$ is low
- Very economical process
- Termed “ratio” logic
- Compact layout (no wells !)
- Response time slow on L-H output transitions
- Dominant MOS logic until about 1985
- Depletion device not available in most processes today
Other CMOS Logic Families

- Reduced $V_{H} - V_{L}$
- Device sizing critical for even basic operation
- Shallow slope at $V_{TRIP}$
Other CMOS Logic Families

Enhancement Load
Pseudo-NMOS

- Reduced $V_H - V_L$
- Device sizing critical for even basic operation (DOF)
- Shallow slope at $V_{TRIP}$
Other CMOS Logic Families

Depletion Load NMOS

- Reduced $V_H - V_L$
- Device sizing critical for even basic operation
- Shallow slope at $V_{TRIP}$
Other CMOS Logic Families

- Reduced $V_H - V_L$
- Device sizing critical for even basic operation
- Shallow slope at $V_{TRIP}$
Static Power Dissipation in Static CMOS Family

When $V_{\text{OUT}}$ is Low, $I_{D1}=0$

When $V_{\text{OUT}}$ is High, $I_{D2}=0$

Thus, $P_{\text{STATIC}}=0$

This is a key property of the static CMOS Logic Family and is the major reason Static CMOS Logic is so dominant.

It can be shown that this zero static power dissipation property can be preserved if the PUN is comprised of p-channel devices, the PDN is comprised of n-channel devices and they are never both driven into the conducting states at the same time.
Static Power Dissipation in Ratio Logic Families

Example:

Assume \( V_{DD} = 5 \text{V} \)
\( V_T = 1 \text{V} \), \( \mu C_{OX} = 10^{-4} \text{A/V}^2 \), \( W_1/L_1 = 1 \) and \( M_2 \) sized so that \( V_L = V_{Tn} \)

Observe:

\[ V_H = V_{DD} - V_{Tn} \]

If \( V_{IN} = V_H \), \( V_{OUT} = V_L \) so

\[
I_{D1} = \frac{\mu C_{OX} W_1}{L_1} \left( V_{GS1} - V_T - \frac{V_{DS1}}{2} \right) V_{DS1}
\]

\[
I_{D1} = 10^{-4} \left( 5 - 1 - 1 - \frac{1}{2} \right) \cdot 1 = 0.25 \text{mA}
\]

\( P_L = (5 \text{V}) (0.25 \text{mA}) = 1.25 \text{mW} \)
Static Power Dissipation in Ratio Logic Families

Example: Assume $V_{DD}=5V$

$V_T=1V$, $\mu C_{OX}=10^{-4}A/V^2$, $W_1/L_1=1$ and $M_2$ sized so that $V_L=V_{Tn}$

$$P_L=(5V)(0.25mA)=1.25mW$$

If a circuit has 100,000 gates and half of them are in the $V_{OUT}=V_L$ state, the static power dissipation will be
Static Power Dissipation in Ratio Logic Families

Example:

Assume $V_{DD} = 5V$
$V_T = 1V$, $\mu C_{OX} = 10^{-4} A/V^2$, $W_1/L_1 = 1$ and $M_2$ sized so that $V_L = V_{Tn}$

$P_L = (5V)(0.25mA) = 1.25mW$

If a circuit has 100,000 gates and half of them are in the $V_{OUT} = V_L$ state, the static power dissipation will be

$$P_{STATIC} = \frac{1}{2} \cdot 10^5 \cdot 1.25mW = 62.5W$$

This power dissipation is way too high and would be even larger in circuits with 100 million or more gates – the level of integration common in SoC circuits today.
Propagation Delay in Static CMOS Family

Switch-level model of Static CMOS inverter (neglecting diffusion parasitics)
Propagation Delay in Static CMOS Family

Switch-level model of Static CMOS inverter (neglecting diffusion parasitics)
Propagagation Delay in Static CMOS Family

Since operating in triode through most of transition:

\[ I_D \approx \frac{\mu C_{ox} W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} \approx \frac{\mu C_{ox} W}{L} \left( V_{GS} - V_T \right) V_{DS} \]

\[ R_{PD} = \frac{V_{DS}}{I_D} = \frac{L_1}{\mu_n C_{ox} W_1 \left( V_{DD} - V_{Tn} \right)} \]

\[ I_D = \frac{\mu C_{ox} W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} \approx \frac{\mu C_{ox} W}{L} \left( V_{GS} - V_T \right) V_{DS} \]

\[ R_{PU} = \frac{V_{DS}}{I_D} = \frac{L_2}{\mu_p C_{ox} W_2 \left( V_{DD} + V_{Tp} \right)} \]

\[ C_{IN} = C_{ox} \left( W_1 L_1 + W_2 L_2 \right) \]
Propagation Delay in Static CMOS Family

Example: Minimum-sized $M_1$ and $M_2$

If $u_nC_{OX}=100\mu A V^{-2}$, $C_{OX}=4 \text{ fF} \mu^{-2}$, $V_{Tn}=V_{DD}/5$, $V_{TP}=-V_{DD}/5$, $\mu_n/\mu_p=3$, $L_1=W_1=L_{MIN}$, $L_2=W_2=L_{MIN}$, $L_{MIN}=0.5\mu$ and $V_{DD}=5V$

(Note: This $C_{OX}$ is somewhat larger than that in the 0.5\mu ON process)

$$R_{PD} = \frac{1}{10^{-4} \cdot 0.8V_{DD}} = 2.5K\Omega$$

$$R_{PU} = \frac{1}{10^{-4} \cdot \frac{1}{3} \cdot 0.8V_{DD}} = 7.5K\Omega$$

$$C_{IN} = 4 \cdot 10^{-15} \cdot 2L_{MN}^2 = 2fF$$
Propagation Delay in Static CMOS Family

In typical process with Minimum-sized $M_1$ and $M_2$:

$R_{PD} \approx 2.5\, \text{K}\Omega$

$R_{PU} \approx 3R_{PD} = 7.5\, \text{K}\Omega$

$C_{IN} \approx 2\, \text{fF}$
Propagation Delay in Static CMOS Family

In typical process with Minimum-sized $M_1$ and $M_2$:

$R_{PD} \approx 2.5K\Omega$

$R_{PU} \approx 3R_{PD} = 7.5K\Omega$

$C_{IN} \approx 2fF$

How long does it take for a signal to propagate from x to y?
Propagation Delay in Static CMOS Family

Consider:

For HL output transition, $C_L$ charged to $V_{DD}$

Ideally:
Propagation Delay in Static CMOS Family

For HL output transition, $C_L$ charged to $V_{DD}$

Actually:

What is the transition time $t_{HL}$?
Propagation Delay in Static CMOS Family
Propagation Delay in Static CMOS Family

For HL output transition, $C_L$ charged to $V_{DD}$

\[ V_{OUT} = F + (1 - F) e^{-\frac{t}{\tau}} = 0 + (V_{DD} - 0) e^{-\frac{t}{R_{PD}C_L}} \]

\[ \frac{V_{DD}}{e} = V_{DD} e^{-\frac{t_1}{R_{PD}C_L}} \quad t_1 = R_{PD}C_L \]

If $V_{TRIP}$ is close to $V_{DD}/2$, $t_{HL}$ is close to $t_1$
Propagation Delay in Static CMOS Family

For HL output transition, $C_L$ charged to $V_{DD}$

$t_{LH} \approx t_2 = R_{PU} C_L$

Summary:

$t_{LH} \approx R_{PU} C_L$

$t_{HL} \approx R_{PD} C_L$

For $V_{TRIP}$ close to $V_{DD}/2$
Propagation Delay in Static CMOS Family

In typical process with Minimum-sized $M_1$ and $M_2$:

$t_{HL} \approx R_{PD}C_L \approx 2.5K \cdot 2fF = 5\text{ps}$

$t_{LH} \approx R_{PU}C_L \approx 7.5K \cdot 2fF = 15\text{ps}$

(Note: This $C_{OX}$ is somewhat larger than that in the 0.5u ON process)

Note: LH transition is much slower than HL transition
Propagation Delay in Static CMOS Family

Defn: The Propagation Delay of a gate is defined to be the sum of $t_{HL}$ and $t_{LH}$, that is, $t_{PROP} = t_{HL} + t_{LH}$.

$$t_{PROP} = t_{HL} + t_{LH} \approx C_L \left( R_{PU} + R_{PD} \right)$$

Propagation delay represents a fundamental limit on the speed a gate can be clocked.

For basic two-inverter cascade in static CMOS logic:

In typical process with minimum-sized $M_1$ and $M_2$:

$$t_{PROP} = t_{HL} + t_{LH} \approx 20 \ psec$$
Propagation Delay in Static CMOS Family

The propagation delay through \( k \) levels of logic is approximately the sum of the individual delays in the same path.
Propagation Delay in Static CMOS Family

Example:

\[ t_{HL} = t_{HL4} + t_{LH3} + t_{HL2} + t_{LH1} \]

\[ t_{LH} = t_{LH4} + t_{HL3} + t_{LH2} + t_{HL1} \]

\[ t_{PROP} = t_{LH} + t_{HL} = (t_{LH4} + t_{HL3} + t_{LH2} + t_{HL1}) + (t_{HL4} + t_{LH3} + t_{HL2} + t_{LH1}) \]

\[ t_{PROP} = t_{LH} + t_{HL} = (t_{LH4} + t_{HL2} + t_{LH2} + t_{HL1}) + (t_{LH1} + t_{HL1}) \]

\[ t_{PROP} = t_{PROP4} + t_{PROP3} + t_{PROP2} + t_{PROP1} \]
Propagation Delay in Static CMOS Family

Propagation through $k$ levels of logic

$$t_{HL} = t_{HLk} + t_{LH(k-1)} + t_{HL(k-2)} + \cdots + t_{XY1}$$

$$t_{LH} = t_{LHk} + t_{HL(k-1)} + t_{LH(k-2)} + \cdots + t_{YX1}$$

where $x=H$ and $Y=L$ if $k$ odd and $X=L$ and $Y=h$ if $k$ even

$$t_{PROP} = \sum_{i=1}^{k} t_{PROP_i}$$

Will return to propagation delay after we discuss device sizing
Digital Circuit Design

- Hierarchical Design
- Basic Logic Gates
- Properties of Logic Families
- Characterization of CMOS Inverter
- Static CMOS Logic Gates
  - Ratio Logic
- Propagation Delay
  - Simple analytical models
  - Elmore Delay
- Sizing of Gates

- Propagation Delay with Multiple Levels of Logic
- Optimal driving of Large Capacitive Loads
- Power Dissipation in Logic Circuits
- Other Logic Styles
- Array Logic
- Ring Oscillators

[Partial] done
Device Sizing

Strategies?

Degrees of Freedom?

Will consider the inverter first
Device Sizing

Degrees of Freedom?

Strategies?
Device Sizing

- Since not ratio logic, $V_H$ and $V_L$ are independent of device sizes for this inverter
- With $L_1=L_2=L_{\text{min}}$, there are 2 degrees of freedom ($W_1$ and $W_2$)

Sizing Strategies

- Minimum Size
- Fixed $V_{\text{TRIP}}$
- Equal rise-fall times (equal worst-case rise and fall times)
- Minimum power dissipation
- Minimum time required to drive a given load
- Minimum input capacitance
Device Sizing

Assume $V_{Tn} = 0.2V_{DD}$, $V_{Tp} = -0.2V_{DD}$, $\mu_n/\mu_p = 3$, $L_1 = L_2 = L_{min}$

Sizing Strategy: minimum sized

$W_n = ?, \quad W_p = ?, \quad V_{trip} = ?, t_{HL} = ?, t_{LH} = ?$

$R_{PD} = \frac{L_1}{\mu_n C_{OX} W_1 (V_{DD} - V_{Tn})}$

$R_{PU} = \frac{L_2}{\mu_p C_{OX} W_2 (V_{DD} + V_{Tp})}$

$C_{IN} = C_{OX}(W_1L_1 + W_2L_2)$
Device Sizing

Assume $V_{Tn}=0.2V_{DD}$, $V_{Tp}=-0.2V_{DD}$, $\mu_n/\mu_p=3$, $L_1=L_2=L_{\text{min}}$

Sizing Strategy: minimum sized

$W_n=\?, W_p=\?, V_{\text{trip}}=\?, t_{HL}=\?, t_{LH}=\?$

$W_1=W_2=W_{\text{MIN}}$

also provides minimum input capacitance

$t_{HL}=R_{PD}C_L$

$t_{LH}=3\ R_{PD}C_L$

$t_{LH}$ is longer than $t_{HL}$

$t_{\text{PROP}}=4R_{PD}C_L$

$V_{\text{TRIP}} = \frac{(V_{Tn}) + (V_{DD} + V_{Tp}) \sqrt{\frac{\mu_p}{\mu_n} \frac{W_2}{W_1} \frac{L_1}{L_2}}}{1 + \sqrt{\frac{\mu_p}{\mu_n} \frac{W_2}{W_1} \frac{L_2}{L_1}}}$

$V_{\text{TRIP}} = \left(0.2V_{DD}\right) + \left(V_{DD} - 0.2V_{DD}\right) \sqrt{\frac{1}{3}} = 0.42V_{DD}$
Device Sizing

Assume $V_{Tn} = 0.2V_{DD}$, $V_{Tp} = -0.2V_{DD}$, $\mu_n/\mu_p = 3$, $L_1 = L_2 = L_{\text{min}}$

Sizing strategy: Equal (worst case) rise and fall times

$W_n = ?, \ W_p = ?, \ V_{\text{trip}} = ?, t_{\text{HL}} = ?, t_{\text{LH}} = ?$

$R_{PD} = \frac{L_{\text{min}}}{\mu_n C_{OX} W_1 (0.8V_{DD})}$

$R_{PU} = \frac{L_{\text{min}}}{3\mu_n C_{OX} W_2 (0.8V_{DD})}$
Device Sizing

Assume $V_{Tn} = 0.2V_{DD}$, $V_{Tp} = -0.2V_{DD}$, $\mu_n/\mu_p = 3$, $L_1 = L_2 = L_{\text{min}}$

Sizing strategy: Equal (worst case) rise and fall times

Thus

$$\frac{t_{lh}}{t_{hl}} = \frac{R_{PU}C_{IN}}{R_{PD}C_{IN}} \Rightarrow R_{PU} = R_{PD}$$

$$\frac{L_1}{u_nC_{OX}W_1(V_{DD} - V_{Tn})} = \frac{L_2}{u_pC_{OX}W_2(V_{DD} + V_{Tp})}$$

with $L_1 = L_2$ and $V_{Tp} = -V_{Tn}$ we must have

$$\frac{W_2}{W_1} = \frac{\mu_n}{\mu_p} \approx 3$$

What about the second degree of freedom?

$W_1 = W_{\text{MIN}}$

$V_{TRIP} = ?$
Device Sizing

Assume $V_{Tn} = 0.2V_{DD}$, $V_{Tp} = -0.2V_{DD}$, $\mu_n/\mu_p = 3$, $L_1 = L_2 = L_{\text{min}}$

Sizing strategy: Equal (worst-case) rise and fall times

$W_n = W_{\text{MIN}}$, $W_p = 3W_{\text{MIN}}$, $V_{\text{TRIP}} = ?, t_{HL} = ?, t_{LH} = ?$

\[
V_{\text{TRIP}} = \frac{(V_{Tn}) + (V_{DD} + V_{Tp}) \sqrt{\frac{\mu_p W_2 L_1}{\mu_n W_1 L_2}}}{1 + \sqrt{\frac{\mu_p W_2 L_1}{\mu_n W_1 L_2}}} = \frac{0.2V_{DD} + 0.8V_{DD}}{2} = \frac{V_{DD}}{2}
\]

$t_{HL} = t_{LH} = R_{pd}C_L = \frac{L_{\text{min}}}{\mu_n C_{OX} W_{\text{MIN}} (0.8V_{DD})} C_L$

$t_{\text{PROP}} = 2 R_{pd}C_L$

For a fixed $C_L$, how does $t_{\text{PROP}}$ compare for the minimum-sizing compared to equal rise/fall sizing?
Device Sizing

Assume $V_{Tn} = 0.2V_{DD}$, $V_{Tp} = -0.2V_{DD}$, $\mu_n/\mu_p = 3$, $L_1 = L_2 = L_{min}$

Sizing strategy: Fixed $V_{TRIP} = V_{DD}/2$

$W_n = ?, \ W_p = ?, \ V_{trip} = ?, \ t_{HL} = ?, \ t_{LH} = ?$
Device Sizing

Assume \( V_{Tn} = 0.2V_{DD}, \ V_{Tp} = -0.2V_{DD}, \ \mu_n/\mu_p = 3, \ L_1 = L_2 = L_{\text{min}} \)

Sizing strategy: Fixed \( V_{TRIP} = V_{DD}/2 \)

\[
W_n = ?, \ W_p = ?, \ V_{\text{trip}} = ?, t_{HL} = ?, t_{LH} = ?
\]

Set

\[
V_{TRIP} = V_{DD}/2
\]

\[
V_{TRIP} = \frac{0.2V_{DD} + (V_{DD} - 0.2V_{DD})}{1 + \frac{\mu_p W_2}{\mu_n W_1} \frac{L_1}{L_2}} = \frac{V_{DD}}{2}
\]

Solving, obtain

\[
\frac{W_2}{W_1} = \frac{\mu_n}{\mu_p}
\]

\[
W_n = W_{\text{MIN}}, \ W_p = 3W_{\text{MIN}}
\]

• This is the same sizing as was obtained for equal worst-case rise and fall times so \( t_{HL} = t_{LH} = R_{pd}C_L \)
• This is no coincidence !!! Why?
• These properties guide the definition of the process parameters provided by the foundry
Device Sizing

Assume $V_{Tn} = 0.2V_{DD}$, $V_{Tp} = -0.2V_{DD}$, $\mu_n/\mu_p = 3$, $L_1 = L_2 = L_{\text{min}}$

Sizing Strategies

- Minimum Size
- Fixed $V_{TRIP}$
- Equal rise-fall times
  (equal worst-case rise and fall times)
- Minimum power dissipation
- Minimum time required to drive a given load
- Minimum input capacitance
End of Lecture 37