Digital Circuit Design

- Inverter sizing strategy
- Multiple-input gates
- Other Logic Families
  - Static Power Dissipation
- Propagation Delay – basic characterization
- Device Sizing (Inverter and multiple-input gates)
Hierarchical Digital Design Domains:

- Behavioral:
- Structural:
- Physical

Multiple Sublevels in Each Major Level
Multiple “correct” representations at each level ➔ various optimizations are possible
Representation of Digital Systems

Standard Approach to Digital Circuit Design

1. Behavioral Description
   - Technology independent
2. RTL Description
   (must verify \((1) \Leftrightarrow (2)\))
3. RTL Compiler
   Registers and Combinational Logic Functions
4. Logic Optimizer
5. Logic Synthesis
   Generally use a standard call library for synthesis
6. Place and Route

(physically locates all gates and registers and interconnects them)

7. Layout Extraction
   • DRC
   • Back Annotation

8. Post Layout simulation
   May necessitate a return to a higher level in the design flow
The most basic logic gate: the inverter

Every logic family has to have inverters
Inverter performance is indicative of all gates
It suffices to characterize the inverter
Inverter’s $V_H$, $V_L$, and $V_{TRIP}$

Don’t legislate these quantities. Let the inverter define these by itself. The inverter-pair transfer characteristics (IPTC) define all three. The inverter transfer characteristics (ITC) defines $V_{TRIP}$

Use loop back to measure/simulate these quantities

Review from Last Lecture
Transfer characteristics of the static CMOS inverter

(Neglect $\lambda$ effects)

Vertical line at:

$$V_{\text{IN}} = \frac{(V_{\text{Tn}}) + (V_{\text{DD}} + V_{\text{Tp}}) \sqrt{\frac{\mu_p W_2 L_1}{\mu_n W_1 L_2}}}{1 + \sqrt{\frac{\mu_p W_2 L_1}{\mu_n W_1 L_2}}}$$

$$V_{\text{TRIP}} = \frac{(V_{\text{Tn}}) + (V_{\text{DD}} + V_{\text{Tp}}) \sqrt{\frac{\mu_p W_2 L_1}{\mu_n W_1 L_2}}}{1 + \sqrt{\frac{\mu_p W_2 L_1}{\mu_n W_1 L_2}}}$$
Review from Last Lecture

Inverter Transfer Characteristics of Inverter Pair for **THIS** Logic Family

\[ V_{\text{IN}} \rightarrow V'_{\text{OUT}} \]

\[ V_D = V_{\text{DD}} \quad \text{and} \quad V_L = 0 \]

Independent of sizes
Sizing of the Basic CMOS Inverter

How should $M_1$ and $M_2$ be sized?

How many degrees of freedom are there in the design of the inverter?

The characteristic that device sizes do not need to be used to establish $V_H$ and $V_L$ logic levels is a major advantage of this type of logic.
How should $M_1$ and $M_2$ be sized?

\[ \{ W_1, W_2, L_1, L_2 \} \]

How many degrees of freedom are there in the design of the inverter?

4 degrees of freedom

But in basic device model and in most performance metrics, $W_1/L_1$ and $W_2/L_2$ appear as ratios

\[ \{ W_1/L_1, W_2/L_2 \} \]

effectively 2 degrees of freedom
How should $M_1$ and $M_2$ be sized?

4 degrees of freedom 
\[ \{ W_1, W_2, L_1, L_2 \} \]

Usually pick $L_1 = L_2 = L_{\text{min}}$

That’s the whole point of Moore’s law scaling

Effectively 2 degrees of freedom 
\[ \{ W_1, W_2 \} \]

How are $W_1$ and $W_2$ chosen?

 Depends upon what performance parameters are most important for a given application!
How should $M_1$ and $M_2$ be sized?

pick $L_1=L_2=L_{\text{min}}$

One popular sizing strategy:
1. Pick $W_1=W_{\text{MIN}}$ to minimize area of $M_1$
2. Pick $W_2$ to set trip-point at $V_{\text{DD}}/2$

Thus, at the trip point,

$$V_{\text{OUT}} = V_{\text{IN}} = V_{\text{TRIP}} = \frac{V_{\text{DD}}}{2}, \quad \text{if} \quad \frac{W_2}{W_1} = \frac{\mu_n}{\mu_p}, \quad \text{and} \quad V_{\text{TP}} = -V_{\text{TN}}$$
Extension of Basic CMOS Inverter to Multiple-Input Gates

Performs as a 2-input NOR Gate

Can be easily extended to an n-input NOR Gate

\( V_H = V_{DD} \) and \( V_L = 0 \) (inherited from inverter analysis)
Extension of Basic CMOS Inverter to Multiple-Input Gates

Performs as a 2-input NAND Gate

Can be easily extended to an n-input NAND Gate

$V_H = V_{DD}$ and $V_L = 0$ (inherited from inverter analysis)
Static CMOS Logic Family

Observe PUN is p-channel, PDN is n-channel

\( V_H = V_{DD} \) and \( V_L = 0 \) (inherited from inverter analysis)
Static CMOS Logic Family

n-channel PDN and p-channel PUN

\( V_H = V_{DD}, \ V_L = 0V \) (same as for inverter!)
General Logic Family

Compound Gate in CMOS Process

p-channel PUN
n-channel PDN

\( V_H = V_{DD}, V_L = 0V \) (same as for inverter!)

Arbitrary PUN and PDN
Other MOS Logic Families

Enhancement Load NMOS

Enhancement Load Pseudo-NMOS

Depletion Load NMOS
Digital Circuit Design

- Hierarchical Design
- Basic Logic Gates
- Properties of Logic Families
- Characterization of CMOS Inverter
- Static CMOS Logic Gates
  - Ratio Logic
    - Propagation Delay
      - Simple analytical models
      - Elmore Delay
  - Sizing of Gates
- Propagation Delay with Multiple Levels of Logic
- Optimal driving of Large Capacitive Loads
- Power Dissipation in Logic Circuits
- Other Logic Styles
- Array Logic
- Ring Oscillators

done

partial
Other CMOS/MOS Logic Families

Enhancement Load NMOS

V_in
M1
M2
V_out
V_{DD}

V_{out} = \begin{cases} 
V_{DD} & \text{if } V_{in} \geq V_Tn \\
V_{DD} - V_{Tn} & \text{if } V_{in} < V_Tn 
\end{cases}

V_{in} \rightarrow V_{out}

V_{out} \rightarrow V_{in}

V_{DD} \rightarrow V_{DD}
NMOS example

Enhancement Load NMOS

V_{IN} \rightarrow M_1 \rightarrow V_{OUT} \rightarrow V_{DD} \rightarrow M_2

\begin{align*}
V_{TH} & : 1 \\
W_1/L_1 & : 4 \\
W_2/L_2 & : 1 \\
V_{DD} & : 5
\end{align*}

Inverter

Inverter Pair

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NMOS example

\[
\begin{align*}
V_{IN} & \quad V_{OUT} \\
V_{DD} & \\
M_1 & \\
& \quad V_{TH} \\
W_1/L_1 & 4 \\
W_2/L_2 & 1 \\
V_{DD} & 5 \\
& \quad V_H \\
& \quad V_L \\
& \quad V_{TRIP} \\
\end{align*}
\]

Inverter Pair

\[V_H = 4V\]
\[V_L = 0.55V\]
\[V_{TRIP} = 2V\]
Other CMOS/MOS Logic Families

- High and low swings are reduced 😞
- Response time is slow on LH output transitions 😞
- Static Power Dissipation Large when $V_{OUT}$ is low 😞
- Very economical process 😊
- Termed “ratio logic” (because logic values dependent on device W ratio – DOF!) 😊
- May not work for some device sizes 😟
- Compact layout (no wells !) 😊
Other CMOS/MOS Logic Families

- Multiple-input gates require single transistor for each additional input
- Still useful if many inputs are required (static power does not increase with k)
Other CMOS/MOS Logic Families

- High and low swings are reduced
- Response time is slow on LH output transitions
- Static Power Dissipation Large when $V_{OUT}$ is low
- Multiple-input gates require single transistor for each additional input
- Termed “ratio” logic
Other CMOS/MOS Logic Families

- Low swing is reduced
- Static Power Dissipation Large when $V_{OUT}$ is low
- Very economical process
- Termed “ratio” logic
- Compact layout (no wells !)
- Response time slow on L-H output transitions
- Dominant MOS logic until about 1985
- Depletion device not available in most processes today
Other CMOS/MOS Logic Families

- Reduced $V_H - V_L$
- Device sizing critical for even basic operation
- Shallow slope at $V_{TRIP}$
Other CMOS/MOS Logic Families

- Reduced $V_H - V_L$
- Device sizing critical for even basic operation (DOF)
- Shallow slope at $V_{TRIP}$
Other CMOS/MOS Logic Families

- Reduced $V_H - V_L$
- Device sizing critical for even basic operation
- Shallow slope at $V_{TRIP}$
When \( V_{IN} \) is Low and \( V_{OUT} \) is High, M1 is off and \( I_{D1}=0 \)

When \( V_{IN} \) is High and \( V_{OUT} \) is Low, M2 is off and \( I_{D2}=0 \)

Thus, \( P_{STATIC}=0 \)

This is a key property of the static CMOS Logic Family ➔ the major reason Static CMOS Logic is so dominant

It can be shown that this zero static power dissipation property can be preserved if the PUN is comprised of p-channel devices, the PDN is comprised of n-channel devices and they are never both driven into the conducting states at the same time
Static Power Dissipation in Ratio Logic Families

Example:

Assume $V_{DD}=5V$
$V_T=1V$, $\mu C_{OX}=10^{-4}A/V^2$, $W_1/L_1=1$ and $M_2$ sized so that $V_L$ is close to $V_{Tn}$

Observe:
$V_H=V_{DD}-V_{Tn}$

If $V_{IN}=V_H$, $V_{OUT}=V_L$ so

$$I_{D1} = \frac{\mu C_{OX} W_1}{L_1} \left( V_{GS1} - V_T - \frac{V_{DS1}}{2} \right) V_{DS1}$$

$$I_{D1} = 10^{-4} \left( 5 - 1 - 1 - \frac{1}{2} \right) \cdot 1 = 0.25mA$$

$P_L=(5V)(0.25mA)=1.25mW$
Static Power Dissipation in Ratio Logic Families

Example:

Assume $V_{DD}=5V$

$V_T=1V$, $\mu C_{OX}=10^{-4}A/V^2$, $W_1/L_1=1$ and $M_2$ sized so that $V_L$ is close to $V_{Tn}$

$$P_L=(5V)(0.25mA)=1.25mW$$

If a circuit has 100,000 gates and half of them are in the $V_{OUT}=V_L$ state, the static power dissipation will be...
Static Power Dissipation in Ratio Logic Families

Example:

Assume $V_{DD}=5V$
$V_T=1V$, $\mu C_{OX}=10^{-4}A/V^2$, $W_1/L_1=1$ and $M_2$ sized so that $V_L$ is close to $V_Tn$

$$P_L=(5V)(0.25mA)=1.25mW$$

If a circuit has 100,000 gates and half of them are in the $V_{OUT}=V_L$ state, the static power dissipation will be

$$P_{STATIC} = \frac{1}{2} 10^5 \cdot 1.25mW = 62.5W$$

This power dissipation is way too high and would be even larger in circuits with 100 million or more gates – the level of integration common in SoC circuits today
Propagation Delay in Static CMOS Family

Switch-level model of Static CMOS inverter (neglecting diffusion parasitics)
Switch-level model of Static CMOS inverter (neglecting diffusion parasitics)
Propagation Delay in Static CMOS Family

\[ I_D \approx \frac{\mu C_{OX} W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} \approx \frac{\mu C_{OX} W}{L} (V_{GS} - V_T) V_{DS} \]

\[ R_{PD} = \frac{V_{DS}}{I_D} = \frac{L_1}{\mu_n C_{OX} W_1 (V_{DD} - V_{Tn})} \]

\[ I_D = \frac{\mu C_{OX} W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} \approx \frac{\mu C_{OX} W}{L} (V_{GS} - V_T) V_{DS} \]

\[ R_{PU} = \frac{V_{DS}}{I_D} = \frac{L_2}{\mu_p C_{OX} W_2 (V_{DD} + V_{Tp})} \]

\[ C_{IN} = C_{OX} (W_1 L_1 + W_2 L_2) \]
Propagation Delay in Static CMOS Family

\[
R_{PD} = \frac{L_1}{\mu_n C_{OX} W_1 (V_{DD} - V_{Tn})}
\]
\[
R_{PU} = \frac{L_2}{\mu_p C_{OX} W_2 (V_{DD} + V_{TP})}
\]
\[
C_{IN} = C_{OX} (W_1 L_1 + W_2 L_2)
\]

Example: Minimum-sized \( M_1 \) and \( M_2 \)

If \( \mu_n C_{OX} = 100 \mu A V^{-2} \), \( C_{OX} = 4 \) fF \( \mu^{-2} \), \( V_{Tn} = V_{DD}/5 \), \( V_{TP} = -V_{DD}/5 \), \( \mu_n/\mu_p = 3 \), \( L_1 = W_1 = L_{MIN} \), \( L_2 = W_2 = L_{MIN} \), \( L_{MIN} = 0.5 \mu \) and \( V_{DD} = 5V \)

(Note: This \( C_{OX} \) is somewhat larger than that in the 0.5u ON process)

\[
R_{PD} = \frac{1}{10^{-4} \cdot 0.8V_{DD}} = 2.5K\Omega
\]
\[
R_{PU} = \frac{1}{10^{-4} \cdot \frac{1}{3} \cdot 0.8V_{DD}} = 7.5K\Omega
\]
\[
C_{IN} = 4 \cdot 10^{-15} \cdot 2L_{MN}^2 = 2fF
\]
In typical process with Minimum-sized $M_1$ and $M_2$:

$R_{PD} \approx 2.5\, \text{K}\Omega$

$R_{PU} \approx 3R_{PD} = 7.5\, \text{K}\Omega$

$C_{IN} \approx 2\, \text{fF}$
Propagation Delay in Static CMOS Family

In typical process with Minimum-sized M₁ and M₂:

\[ R_{PD} \approx 2.5\, \text{KΩ} \]
\[ R_{PU} \approx 3\, R_{PD} = 7.5\, \text{KΩ} \]
\[ C_{IN} \approx 2\, \text{fF} \]

How long does it take for a signal to propagate from x to y?
Propagation Delay in Static CMOS Family

Consider:

For HL output transition, $C_L$ charged to $V_{DD}$

Ideally:
Propagation Delay in Static CMOS Family

For HL output transition, $C_L$ charged to $V_{DD}$

Actually:

What is the transition time $t_{HL}$?
Propagation Delay in Static CMOS Family

\[ V_{IN} \rightarrow V_{OUT} \rightarrow C_L \]

\[ V_{DD} \rightarrow R_{PU} \rightarrow \overline{V_G} \rightarrow V_{OUT} \]

\[ V_{IN} \rightarrow C_{IN} \rightarrow R_{PD} \rightarrow V_G \rightarrow C_L \]
Propagation Delay in Static CMOS Family

For HL output transition, $C_L$ charged to $V_{DD}$

For $V_{IN}$ transition, $C_L$ charged to $V_{DD}$

$$V_{OUT}(t) = F + (1 - F)e^{-rac{t}{\tau}} = 0 + (V_{DD} - 0)e^{-\frac{t}{R_{PD}C_L}}$$

If $V_{TRIP}$ is close to $V_{DD}/2$, $t_{HL}$ is close to $t_1$
Propagagation Delay in Static CMOS Family

For HL output transition, $C_L$ charged to $V_{DD}$

$V_{IN}$

$V_{OUT}$

$C_L$

$V_{IN}$

$V_{OUT}$

$V_{DD}$

$t=0$

Summary:

$t_{LH} \approx t_2 = R_{PU}C_L$

$t_{HL} \approx R_{PD}C_L$

For $V_{TRIP}$ close to $V_{DD}/2$
Propagation Delay in Static CMOS Family

In typical process with Minimum-sized $M_1$ and $M_2$:

\[ t_{HL} \approx R_{PD}C_L \approx 2.5K \cdot 2fF = 5ps \]

\[ t_{LH} \approx R_{PU}C_L \approx 7.5K \cdot 2fF = 15ps \]

(Note: This $C_{OX}$ is somewhat larger than that in the 0.5u ON process)

Note: LH transition is much slower than HL transition
Propagation Delay in Static CMOS Family

Defn: The Propagation Delay of a gate is defined to be the sum of $t_{HL}$ and $t_{LH}$, that is, $t_{PROP} = t_{HL} + t_{LH}$

\[
t_{PROP} = t_{HL} + t_{LH} \approx C_L \left( R_{PU} + R_{PD} \right)
\]

Propagation delay represents a fundamental limit on the speed a gate can be clocked

For basic two-inverter cascade in static CMOS logic

\[
t_{PROP} = t_{HL} + t_{LH} \approx 20 \text{ } p \text{sec}
\]
Propagation Delay in Static CMOS Family

\[ t_{PROP} = t_{HL} + t_{LH} \approx C_L (R_{PU} + R_{PD}) \]

\[ R_{PD} = \frac{L_1}{\mu_n C_{OX} W_1 (V_{DD} - V_{Tn})} \quad R_{PU} = \frac{L_2}{\mu_p C_{OX} W_2 (V_{DD} + V_{Tp})} \quad C_{IN} = C_{OX} (W_1 L_1 + W_2 L_2) \]

\[ t_{PROP} = C_{OX} (W_1 L_1 + W_2 L_2) \left( \frac{L_1}{n C_{OX} W_1 (V_{DD} - V_T)} + \frac{L_2}{p C_{OX} W_2 (V_{DD} + V_T)} \right) \]

If \( L_2 = L_1 = L_{\text{min}} \), \( n = 3 \), \( p = 3 \),

\[ t_{PROP} = \frac{L_{\text{min}}^2}{n (V_{DD} / V_T)} (W_1 + W_2) \left( \frac{1}{W_1} + \frac{3}{W_2} \right) = \frac{L_{\text{min}}^2}{n (V_{DD} / V_T)} (4 + \frac{W_2^2}{W_1^2} + 3 \frac{W_1^2}{W_2^2}) \]

For min size: \[ W_2 = W_1 = W_{\text{min}} \]

For equal rise/fall: \[ W_2 = 3W_1 \]

For min delay: \[ W_2 = \sqrt{3} W_1 \]

\[ t_{PROP} = \frac{8L_{\text{min}}^2}{n (V_{DD} / V_T)} \quad t_{PROP} = \frac{8L_{\text{min}}^2}{n (V_{DD} / V_T)} \quad t_{PROP} = \frac{(4 + 2\sqrt{3})L_{\text{min}}^2}{n (V_{DD} / V_T)} \]
Approximate BSIM values

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<th>u</th>
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<th>VDD</th>
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</table>

For min L transistors, mobility will saturate as field strength reaches a certain level.
Propagation Delay in Static CMOS Family

The propagation delay through $k$ levels of logic is approximately the sum of the individual delays in the same path.
Propagation Delay in Static CMOS Family

Example:

\[ t_{HL} = t_{HL4} + t_{HL3} + t_{HL2} + t_{HL1} \]

\[ t_{LH} = t_{LH4} + t_{HL3} + t_{HL2} + t_{HL1} \]

\[ t_{PROP} = t_{LH} + t_{HL} = (t_{LH4} + t_{HL3} + t_{HL2} + t_{HL1}) + (t_{HL4} + t_{HL3} + t_{HL2} + t_{HL1}) \]

\[ t_{PROP} = t_{LH} + t_{HL} = (t_{LH4} + t_{HL4}) + (t_{LH3} + t_{HL3}) + (t_{HL2} + t_{HL2}) + (t_{HL1} + t_{HL1}) \]

\[ t_{PROP} = t_{PROP4} + t_{PROP3} + t_{PROP2} + t_{PROP1} \]
Propagation Delay in Static CMOS Family

Propagation through k levels of logic

\[ t_{HL} \equiv t_{HLk} + t_{LH(k-1)} + t_{HL(k-2)} + \cdots + t_{XY1} \]

\[ t_{LH} \equiv t_{LHk} + t_{HL(k-1)} + t_{LH(k-2)} + \cdots + t_{YX1} \]

where \( x=H \) and \( Y=L \) if \( k \) odd and \( X=L \) and \( Y=h \) if \( k \) even

\[ t_{PROP} = \sum_{i=1}^{k} t_{PROPk} \]

Will return to propagation delay after we discuss device sizing
End of Lecture 37