Sizing of Multiple-Input Gates
Propagation Delay with Multiple Levels of Logic
Device Sizing

Assume $V_{Tn}=0.2V_{DD}$, $V_{Tp}=-0.2V_{DD}$, $\mu_n/\mu_p=3$, $L_1=L_2=L_{min}$

### Sizing Strategy Summary

<table>
<thead>
<tr>
<th>Size</th>
<th>Minimum Size</th>
<th>$V_{TRIP}=V_{DD}/2$</th>
<th>Equal Rise/Fall</th>
</tr>
</thead>
<tbody>
<tr>
<td>W_n, W_p, L_p, L_n</td>
<td>$W_n=W_p=W_{min}$, $L_p=L_n=L_{min}$</td>
<td>$W_n=W_{min}$, $W_p=3W_{min}$, $L_p=L_n=L_{min}$</td>
<td>$W_n=W_{min}$, $W_p=3W_{min}$, $L_p=L_n=L_{min}$</td>
</tr>
<tr>
<td>$t_{HL}$</td>
<td>$R_{pd}C_L$</td>
<td>$R_{pd}C_L$</td>
<td>$R_{pd}C_L$</td>
</tr>
<tr>
<td>$t_{LH}$</td>
<td>$3R_{pd}C_L$</td>
<td>$R_{pd}C_L$</td>
<td>$R_{pd}C_L$</td>
</tr>
<tr>
<td>$t_{PROP}$</td>
<td>$4R_{pd}C_L$</td>
<td>$2R_{pd}C_L$</td>
<td>$2R_{pd}C_L$</td>
</tr>
<tr>
<td>$V_{trip}$</td>
<td>$V_{TRIP}=0.42V_{DD}$</td>
<td>$V_{TRIP}=0.5V_{DD}$</td>
<td>$V_{TRIP}=0.5V_{DD}$</td>
</tr>
</tbody>
</table>

- For a fixed load $C_L$, the minimum-sized structure has a higher $t_{PROP}$ but if the load is another inverter, $C_L$ will also increase so the speed improvements become less apparent
- This will be investigated later

Review from last time
Review from last time

Reference Inverter

The reference inverter

Assume $\mu_n/\mu_p=3 \quad L_n=L_p=L_{MIN} \quad W_n=W_{MIN}, \quad W_p=3W_n$

$$C_{REF} = C_{INREF} = 4C_{OX}W_{MIN}L_{MIN}$$

$$R_{PDREF} = \frac{L_{MIN}}{\mu_nC_{OX}W_{MIN}(V_{DD}-V_{Tn})} \quad V_{Tn}=.2V_{DD} = \frac{L_{MIN}}{\mu_nC_{OX}W_{MIN}(0.8V_{DD})}$$

- Have sized the reference inverter with $W_p/W_n=\mu_n/\mu_p$
- In standard processes, provides $V_{TRIP} \approx V_{DD}/2$ and $t_{HL} \approx t_{LH}$
- Any other sizing strategy could have been used for the reference inverter but this is most convenient
The reference inverter pair

Assume \( \frac{\mu_n}{\mu_p} = 3 \)  

\[ L_n = L_p = L_{\text{MIN}} \quad W_n = W_{\text{MIN}}, \quad W_p = 3W_n \]

\[ C_{L1} = C_{\text{REF}} = 4C_{\text{OX}}W_{\text{MIN}}L_{\text{MIN}} \]

\[ t_{\text{REF}} \quad \text{def} = t_{\text{PROPREF}} = t_{\text{HLREF}} + t_{\text{LHREF}} = 2R_{PDREF}C_{\text{REF}} \]
Reference Inverter

The reference inverter pair

Assume \( \mu_n/\mu_p = 3 \)  

\[ L_n = L_p = L_{MIN} \quad W_n = W_{MIN}, \quad W_p = 3W_n \]

Summary: parameters defined from reference inverter:

\[
C_{REF} = 4C_{OX} W_{MIN} L_{MIN} \\
R_{PDREF} = \frac{\mu_n C_{OX} W_{MIN} (V_{DD} - V_{Tn})}{L_{MIN}} \\
t_{REF} = 2R_{PDREF} C_{REF} \\
C_{REF} = 4C_{OX} W_{MIN} L_{MIN}
\]
The Reference Inverter

\[ C_{\text{REF}} = C_{\text{IN}} = 4C_{\text{OX}} W_{\text{MIN}} L_{\text{MIN}} \]

\[ R_{\text{PDREF}} = \frac{L_{\text{MIN}}}{\mu_n C_{\text{OX}} W_{\text{MIN}} (V_{DD} - V_{Tn})} \quad V_{Tn} = 2V_{DD} \]

\[ t_{\text{HLREF}} = t_{\text{LHREF}} = R_{\text{PDREF}} C_{\text{REF}} \]

\[ t_{\text{REF}} = t_{\text{HLREF}} + t_{\text{LHREF}} = 2R_{\text{PDREF}} C_{\text{REF}} \]

Assume \( \mu_n / \mu_p = 3 \)

\( W_n = W_{\text{MIN}} \), \( W_p = 3W_{\text{MIN}} \)

\( L_n = L_p = L_{\text{MIN}} \)

In 0.5u proc \( t_{\text{REF}} = 20\text{ps}, C_{\text{REF}} = 4\text{fF}, R_{\text{PDREF}} = 2.5\text{K} \)
Propagation Delay

How does the propagation delay compare for a minimum-sized strategy to that of an equal rise/fall sizing strategy?

Minimum Sized

\[ W_2 = W_1 = W_{\text{MIN}} \]

Reference Inverter

\[ W_2 = (\mu_n/\mu_p)W_1, \quad W_1 = W_{\text{MIN}} \]

\[ t_{\text{PROP}} = t_{\text{REF}} \]
Device Sizing

The minimum-sized inverter pair

\[ C_{\text{REF}} = 4C_{\text{OX}}W_{\text{MIN}}L_{\text{MIN}} \]

\[ C_{L1} = 2C_{\text{OX}}W_{\text{MIN}}L_{\text{MIN}} = 0.5C_{\text{REF}} \]

\[ R_{\text{PDn}} = \frac{L_{\text{MIN}}}{\mu_n C_{\text{OX}} W_{\text{MIN}} (V_{\text{DD}} - V_{Tn})} \quad v_{Tn} = 2V_{\text{DD}} = R_{\text{PDREF}} \]

\[ R_{\text{PUp}} = \frac{L_{\text{MIN}}}{\mu_p C_{\text{OX}} W_{\text{MIN}} (V_{\text{DD}} + V_{Tp})} \quad v_{Tn} = 2V_{\text{DD}} = 3R_{\text{PDREF}} \]

\[ t_{\text{PROP}} = t_{\text{HLREF}} + t_{\text{LHREF}} = R_{\text{PDREF}} \left( 0.5C_{\text{REF}} \right) + 3R_{\text{PDREF}} \left( 0.5C_{\text{REF}} \right) = 2R_{\text{PDREF}} C_{\text{REF}} \]

thus \[ t_{\text{PROP}} = t_{\text{REFF}} \]
Device Sizing

The minimum-sized inverter pair

Assume $\mu_n/\mu_p = 3$  
$L_n = L_p = L_{MIN}$  
$W_n = W_{MIN}$, $W_p = W_n$

$C_{REF} = 4C_{OX}W_{MIN}L_{MIN}$

$C_{L1} = 0.5C_{REF} = 2C_{OX}W_{MIN}L_{MIN}$

$$R_{PDREF} = \frac{L_{MIN}}{\mu_n C_{OX} W_{MIN} (V_{DD} - V_{Tn})} = \frac{L_{MIN}}{\mu_n C_{OX} W_{MIN} (0.8V_{DD})}$$

$t_{PROP} = t_{HLREF} + t_{LHREF} = R_{PDREF} (0.5C_{REF}) + 3R_{PDREF} (0.5C_{REF}) = 2R_{PDREF} C_{REF}$

$t_{PROP} = t_{REFF}$
By how much did tHL improve?

Why was there no net change in tPROP?

Propagation Delay

How does the propagation delay compare for a minimum-sized strategy to that of an equal rise/fall sizing strategy?

Minimum Sized

\[ W_2 = W_1 = W_{\text{MIN}} \]

\[ t_{\text{PROP}} = t_{\text{REF}} \]

Reference Inverter

\[ W_2 = \left( \frac{\mu_n}{\mu_p} \right) W_1, \quad W_1 = W_{\text{MIN}} \]

\[ t_{\text{PROP}} = t_{\text{REF}} \]

They are the same!

Even though the tLH rise time has been reduced with the equal rise/fall sizing strategy, this was done at the expense of an increase in the total load capacitance that resulted in no net change in propagation delay!
Will consider now the multiple-input gates

Will consider both minimum sizing and equal worst-case rise/fall

Will assume \( C_L \) (not shown) = \( C_{\text{REF}} \)

Note: worst-case has been added since fall time in NOR gates or rise time in NAND gates depends upon how many transistors are conducting
Sizing of Multiple-Input Gates

Analysis strategy: Express delays in terms of those of reference inverter

Reference Inverter

\[
C_{REF} = C_{IN} = 4C_{OX} W_{MIN} L_{MIN}
\]

\[
R_{PDREF} = \frac{L_{MIN}}{\mu_n C_{OX} W_{MIN} (V_{DD} - V_{Tn})} = \frac{L_{MIN}}{\mu_n C_{OX} W_{MIN} (0.8V_{DD})}
\]

Assume \( \frac{\mu_n}{\mu_p} = 3 \)

\( W_n = W_{MIN}, W_p = 3W_{MIN} \)

In 0.5u proc \( t_{REF} = 20\)ps, \( C_{REF} = 4fF, R_{PDREF} = 2.5K \)

\[
t_{HLREF} = t_{LHREF} = R_{PDREF} C_{REF}
\]

\[
t_{REF} = t_{HLREF} + t_{LHREF} = 2R_{PDREF} C_{REF}
\]

\( L_n = L_p = L_{MIN} \)
Device Sizing

Multiple Input Gates:

2-input NOR  2-input NAND  k-input NOR  k-input NAND

Equal Worst Case Rise/Fall (and equal to that of ref inverter when driving $C_{REF}$)

Wn=?
Wp=?

Fastest response ($t_{HL}$ or $t_{WL}$) = ?
Worst case response ($t_{PROP}$, usually of most interest)?
Input capacitance = ?

Minimum Sized (assume driving a load of $C_{REF}$)

Wn=Wmin
Wp=Wmin

Fastest response ($t_{HL}$ or $t_{WL}$) = ?
Slowest response ($t_{HL}$ or $t_{WL}$) = ?
Worst case response ($t_{PROP}$, usually of most interest)?
Input capacitance = ?
Device Sizing

Equal Worst Case Rise/Fall (and equal to that of ref inverter when driving $C_{REF}$)

Multiple Input Gates: 2-input NOR

DERIVATIONS

$W_n =$?

$W_p =$?
Device Sizing

Equal Worst Case Rise/Fall (and equal to that of ref inverter when driving $C_{REF}$)

Multiple Input Gates:

2-input NOR

**DERIVATIONS**

Fastest response ($t_{HL}$ or $t_{HL}$) = ?

Worst case response ($t_{PROP}$, usually of most interest)?

Input capacitance = ?
Device Sizing

Equal Worst Case Rise/Fall (and equal to that of ref inverter when driving $C_{REF}$)

Multiple Input Gates:

k-input NOR (determine same characteristics as for 2-input NOR)

DERIVATIONS
Device Sizing

Equal Worst Case Rise/Fall (and equal to that of ref inverter when driving $C_{REF}$)

Multiple Input Gates:

2-input NAND (determine same characteristics as for 2-input NOR)

DERIVATIONS

$W_n = ?$
$W_p = ?$
Device Sizing

Equal Worst Case Rise/Fall (and equal to that of ref inverter when driving $C_{\text{REF}}$)

Multiple Input Gates:

2-input NAND (determine same characteristics as for 2-input NOR)

**DERIVATIONS**

Fastest response ($t_{\text{HL}}$ or $t_{\text{HL}}$) = ?

Worst case response ($t_{\text{PROP}}$, usually of most interest)?

Input capacitance = ?
Device Sizing

Equal Worst Case Rise/Fall (and equal to that of ref inverter when driving $C_{\text{REF}}$)

Multiple Input Gates:

k-input NAND (determine same characteristics as for 2-input NOR)

DERIVATIONS
Device Sizing

Multiple Input Gates:

Comparison of NAND and NOR Gates

DERIVATIONS
Device Sizing

Equal Worse-Case Rise/Fall Device Sizing Strategy

-- (same as $V_{TRIP} = V_{DD}/2$ in typical process considered in example)

Assume $\mu_n/\mu_p = 3$  $L_n = L_p = L_{\text{MIN}}$

INV

$W_n = W_{\text{MIN}}$,  $W_p = 3W_{\text{MIN}}$

$C_{\text{IN}} = C_{\text{REF}}$

$k$-input NOR

$W_n = W_{\text{MIN}}$,  $W_p = 3kW_{\text{MIN}}$

$C_{\text{IN}} = \left(\frac{3k+1}{4}\right)C_{\text{REF}}$

$k$-input NOR

$W_n = kW_{\text{MIN}}$,  $W_p = 3W_{\text{MIN}}$

$C_{\text{IN}} = \left(\frac{3+k}{4}\right)C_{\text{REF}}$
Device Sizing

Multiple Input Gates:

- 2-input NOR
- 2-input NAND
- k-input NOR
- k-input NAND

Equal Worst Case Rise/Fall (and equal to that of ref inverter when driving $C_{REF}$)
- $W_n =$?
- $W_p =$?
- Fastest response ($t_{HL}$ or $t_{HL}$) = ?
- Worst case response ($t_{PROP}$, usually of most interest)?
- Input capacitance = ?

Minimum Sized (assume driving a load of $C_{REF}$)

- $W_n = W_{min}$
- $W_p = W_{min}$
- Fastest response ($t_{HL}$ or $t_{HL}$) = ?
- Slowest response ($t_{HL}$ or $t_{HL}$) = ?
- Worst case response ($t_{PROP}$, usually of most interest)?
- Input capacitance = ?
Device Sizing

Minimum Sized (assume driving a load of $C_{REF}$)

$W_n=W_{min}$

$W_p=W_{min}$

Input capacitance = ?

Fastest response ($t_{HL}$ or $t_{HL}$) = ?

Slowest response ($t_{HL}$ or $t_{HL}$) = ?

Worst case response ($t_{PROP}$, usually of most interest)?
Device Sizing

$C_{IN}$ for $N_{AND}$ gates is considerably smaller than for NOR gates for equal worst-case rise and fall times.

$C_{IN}$ for minimum-sized structures is independent of number of inputs and much smaller than $C_{IN}$ for the equal rise/fall time case.

$R_{PU}$ gets very large for minimum-sized NOR gate.
Propagation Delay in Multiple-Levels of Logic with Stage Loading
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Analysis strategy: Express delays in terms of those of reference inverter

Reference Inverter

\[ C_{\text{REF}} = C_{\text{IN}} = 4C_{\text{OX}} W_{\text{MIN}} L_{\text{MIN}} \]

\[ \frac{R_{\text{PDREF}}}{L_{\text{MIN}}} = \frac{\mu_n C_{\text{OX}} W_{\text{MIN}} (V_{\text{DD}} - V_{Tn})}{\mu_n C_{\text{OX}} W_{\text{MIN}} (0.8V_{\text{DD}})} = \frac{V_{Tn} = 2V_{\text{DD}}}{L_{\text{MIN}}} \]

\[ t_{\text{REF}} = t_{\text{HLREF}} + t_{\text{LHREF}} = 2R_{\text{PDREF}} C_{\text{REF}} \]

Assume \( \mu_n / \mu_p = 3 \)

\( W_n = W_{\text{MIN}}, \quad W_p = 3W_{\text{MIN}} \)

In 0.5u proc \( t_{\text{REF}} = 20\)ps, \( C_{\text{REF}} = 4fF, R_{\text{PDREF}} = 2.5K \)

\( L_n = L_p = L_{\text{MIN}} \)
Propagation Delay in Multiple-Levels of Logic with Stage Loading

What loading will a gate see?
Propagation Delay in Multiple-Levels of Logic with Stage Loading

What loading will a gate see?

- Input capacitance to other gates
- Any load capacitors
- Parasitic interconnect capacitances
Propagation Delay with Stage Loading

$t_{REF} = 2R_{PDref}C_{REF}$

$C_{REF} = C_{IN} = 4C_{OX}W_{MIN}L_{MIN}$

$F_{I_C} = \frac{C}{C_{REF}}$

$F_{I_G} = \frac{C_{INk}}{C_{REF}}$

$F_{I_i} = \frac{C_{INi}}{C_{REF}}$

$F_I = \sum_{Gates} C_{INGi} + \sum_{Capacities} C_{INCi} + \sum_{Interconnects} C_{INli}$

$F_I$ can be expressed either in units of capacitance or normalized to $C_{REF}$

Most commonly $F_I$ is normalized but must determine from context
Propagation Delay in Multiple-Levels of Logic with Stage Loading

DERIVATIONS

Neglect interconnect capacitance, assume load of $10C_{REF}$ on F output
Propagation Delay Through Multiple Stages of Logic with Stage Loading

(assuming gate drives are all same as that of reference inverter)

Identify the gate path from A to F

\[ t_{\text{PROP}k} = t_{\text{REF}F_{I(k+1)}} \]

Propagation delay from A to F:

\[ t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^{n} F_{I(k+1)} \]
Digital Circuit Design

- Hierarchical Design
- Basic Logic Gates
- Properties of Logic Families
- Characterization of CMOS Inverter
- Static CMOS Logic Gates
  - Ratio Logic
- Propagation Delay
  - Simple analytical models
  - Elmore Delay
- Sizing of Gates

- Propagation Delay with Multiple Levels of Logic
- Optimal driving of Large Capacitive Loads
  - Power Dissipation in Logic Circuits
  - Other Logic Styles
  - Array Logic
  - Ring Oscillators

- done
- partial
Overdrive Factors

The factor by which the devices are scaled above those of the reference inverter is termed the overdrive factor, OD.

Scaling all widths by a constant does not compromise the symmetry between the rise and fall times.

Judicious use of overdrive can dramatically improve the speed of digital circuits.

Large overdrive factors are often used.
End of Lecture 38