EE 330
Lecture 39
Digital Circuits

Sizing of Gates
Propagation Delay with Multiple Levels of Logic
Optimal driving of Large Capacitive Loads
Digital Circuit Design

• Hierarchical Design
• Basic Logic Gates
• Properties of Logic Families
• Characterization of CMOS Inverter
• Static CMOS Logic Gates
  – Ratio Logic
• Propagation Delay
  – Simple analytical models
• Sizing of Gates

Review from last time

→ Propagation Delay with Multiple Levels of Logic
  – Elmore Delay
→ Optimal driving of Large Capacitive Loads
→ Power Dissipation in Logic Circuits
• Other Logic Styles
• Array Logic
• Ring Oscillators
Device Sizing

Equal Rise/Fall Device Sizing Strategy (with same drive capability as ref inverter)
-- (same as $V_{TRIP} = V_{DD}/2$ in typical process considered in example)

Assume $\mu_n/\mu_p = 3$, $L_n = L_p = L_{MIN}$

**INV**

- $W_n = W_{MIN}$
- $W_p = 3W_{MIN}$
- $C_{IN} = C_{REF}$

**k-input NOR**

- $W_n = W_{MIN}$
- $W_p = 3kW_{MIN}$
- $C_{IN} = \left(\frac{3k+1}{4}\right)C_{REF}$

**k-input NAND**

- $W_n = kW_{MIN}$
- $W_p = 3W_{MIN}$
- $C_{IN} = \left(\frac{3+k}{4}\right)C_{REF}$
Review from last time

**Device Sizing**

- $C_{IN}$ for $N_{AND}$ gates is considerably smaller than for NOR gates for equal worst-case rise and fall times.

- $C_{IN}$ for minimum-sized structures is independent of number of inputs and much smaller than $C_{IN}$ for the equal rise/fall time case.

- $R_{PU}$ gets very large for minimum-sized NOR gate.
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Analysis strategy: Express delays in terms of those of reference inverter

Reference Inverter

\[ C_{\text{REF}} = C_{\text{IN}} = 4C_{\text{OX}} W_{\text{MIN}} L_{\text{MIN}} \]

\[ R_{\text{PDREF}} = \frac{L_{\text{MIN}}}{\mu_n C_{\text{OX}} W_{\text{MIN}} (V_{\text{DD}} - V_{Tn})} \quad V_{Tn} = 2V_{\text{DD}} = \frac{L_{\text{MIN}}}{\mu_n C_{\text{OX}} W_{\text{MIN}} (0.8V_{\text{DD}})} \]

\[ t_{\text{REF}} = t_{\text{HLREF}} + t_{\text{LHREF}} = 2R_{\text{PDREF}} C_{\text{REF}} \]

Assume \( \mu_n / \mu_p = 3 \)

\( W_n = W_{\text{MIN}}, \quad W_p = 3W_{\text{MIN}} \)

In 0.5u proc \( t_{\text{REF}} = 20\text{ps}, \quad C_{\text{REF}} = 4fF, \quad R_{\text{PDREF}} = 2.5K \)

\( L_n = L_p = L_{\text{MIN}} \)
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Analysis strategy: Express delays in terms of those of reference inverter

Reference Inverter

Assume $\mu_n/\mu_p = 3$

$W_n = W_{MIN}, \quad W_p = 3W_{MIN}$

In 0.5u proc $t_{REF} = 20\text{ps}, \quad C_{REF} = 4\text{fF}, \quad R_{PDREF} = 2.5\text{K}$

Note: Even though $C_{REF}$, $R_{PDREF}$ and $T_{REF}$ may not be real accurate, they are “faithful” in that they do a good job of characterizing relative timing performance between different circuits. As such, better accuracy can be obtained by treating $C_{REF}$, $R_{PDREF}$ and $T_{REF}$ as process parameters and these parameters can be obtained by simulation from the cascade of two reference inverters.
Review from last time

Propagation Delay with Stage Loading

\[ t_{\text{REF}} = 2R_{\text{PDref}} C_{\text{REF}} \]
\[ C_{\text{REF}} = C_{\text{IN}} = 4C_{\text{OX}} W_{\text{MIN}} L_{\text{MIN}} \]

Fl of a capacitor

\[ F_{\text{IC}} = \frac{C}{C_{\text{REF}}} \]

Fl of a gate (input k)

\[ F_{\text{IG}} = \frac{C_{\text{INk}}}{C_{\text{REF}}} \]

Fl of an interconnect

\[ F_{\text{I}} = \frac{C_{\text{INI}}}{C_{\text{REF}}} \]

Overall Fl

\[ F_{\text{I}} = \sum_{\text{Gates}} C_{\text{INGi}} + \sum_{\text{Capacitances}} C_{\text{INCi}} + \sum_{\text{Interconnects}} C_{\text{INli}} \]
Review from last time

Propagation Delay Through Multiple Stages of Logic with Stage Loading

(assuming gate drives are all same as that of reference inverter)

Identify the gate path from A to F

\[ t_{PROP_k} = t_{REF} F_{I(k+1)} \]

Propagation delay from A to F:

\[ t_{PROP} = t_{REF} \sum_{k=1}^{n} F_{I(k+1)} \]
Overdrive Factors

The factor by which the devices are scaled above those of the reference inverter is termed the overdrive factor, OD.

Scaling all widths by a constant does not compromise the symmetry between the rise and fall times.

Judicious use of overdrive can dramatically improve the speed of digital circuits.

Large overdrive factors are often used.
Define the Overdrive Factor of the equal rise/fall inverter to be the factor by which PU and PD resistors are scaled relative to those of the reference inverter.

$$R_{PDEFF} = \frac{R_{PDREF}}{OD} \quad R_{PUEFF} = \frac{R_{PUREF}}{OD} = \frac{R_{PDREF}}{OD}$$

It thus follows that

$$t_{HL} = t_{LH} = \frac{R_{PDREF}}{OD} \quad C = R_{PDREF} C_{REF} \frac{F_{IL}}{OD}$$

$$t_{PROP} = t_{LH} + t_{HL} = t_{REF} \frac{F_{IL}}{OD}$$

The OD may be larger or smaller than 1.
Review from last time

Propagation Delay in Multiple-Levels of Logic with Stage Loading

Notation:

\[ t_k = t_{\text{PROP}k} \]

Propagation delay from A to F:

\[ t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^{n} \frac{F_{l(k+1)}}{OD_k} \]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

• Equal rise/fall (no overdrive)

• Equal rise/fall with overdrive

• Minimum Sized

• Asymmetric overdrive

• Combination of equal rise/fall, minimum size and overdrive

\[
t_{PROP} = t_{REF} \sum_{k=1}^{n} F_{I(k+1)}
\]

\[
t_{PROP} = t_{REF} \sum_{k=1}^{n} \frac{F_{I(k+1)}}{OD_k}
\]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

*Will consider an example with the five cases*

- Equal rise/fall (no overdrive)
- Equal rise/fall with overdrive
- Minimum Sized
- Asymmetric Overdrive
- Combination of equal rise/fall, minimum size and overdrive

*Will develop the analysis methods as needed*
Driving Notation

- Equal rise/fall (no overdrive)
- Equal rise/fall with overdrive
- Minimum Sized
- Asymmetric Overdrive

Notation will be used only if it is not clear from the context what sizing is being used
Define the Asymmetric Overdrive Factors of the stage to be the factors by which PU and PD resistors are scaled relative to those of the reference inverter.

\[
R_{PDEFF} = \frac{R_{PDREF}}{OD_{HL}} \quad R_{PUEFF} = \frac{R_{PUREF}}{OD_{LH}} \frac{R_{PDREF}}{OD_{LH}}
\]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Asymmetric Overdrive Notation
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Overdrive Notation

Equal Rise/Fall with overdrive OD

Examples

Equal Rise/Fall with overdrive of 8

Rise/Fall may be different with overdrive $OD_{HL}$ and $OD_{LH}$

If $W_n - W_{MIN}$, minimum sized inverter
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Asymmetric Overdrive

\[ t_{\text{HL}} = \frac{R_{\text{PDREF}}}{\text{OD}_{\text{HL}}} C_L = (R_{\text{PDREF}} C_{\text{REF}}) \left( \frac{C_L}{C_{\text{REF}}} \right) = \frac{1}{2} \frac{t_{\text{REF}}}{\text{OD}_{\text{HL}}} \frac{F_{\text{IL}}}{\text{OD}_{\text{HL}}} \]

\[ t_{\text{LH}} = \frac{R_{\text{PUREF}}}{\text{OD}_{\text{LH}}} C_L = (R_{\text{PDREF}} C_{\text{REF}}) \left( \frac{C_L}{C_{\text{REF}}} \right) = \frac{1}{2} \frac{t_{\text{REF}}}{\text{OD}_{\text{LH}}} \frac{F_{\text{IL}}}{\text{OD}_{\text{LH}}} \]

\[ t_{\text{PROP}} = t_{\text{HL}} + t_{\text{LH}} = \frac{1}{2} t_{\text{REF}} F_{\text{IL}} \left( \frac{1}{\text{OD}_{\text{HL}}} + \frac{1}{\text{OD}_{\text{LH}}} \right) \]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Asymmetric Overdrive

\[ t_{\text{PROP}} = \frac{1}{2} t_{\text{REF}} F_{\text{IL}} \left( \frac{1}{OD_{\text{HL}}} + \frac{1}{OD_{\text{LH}}} \right) \]

Thus, for a cascade of \( n \) gates

\[ t_{\text{PROP}} = \frac{1}{2} t_{\text{REF}} \sum_{i=1}^{n} F_{i(i+1)} \left( \frac{1}{OD_{\text{HL}_i}} + \frac{1}{OD_{\text{LH}_i}} \right) \]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

*Equal rise-fall gates, no overdrive*

\[ t_{\text{REF}} = 2t_{\text{HL}} \]

In 0.5μm proc, \( t_{\text{REF}} = 20\text{ps}, \ C_{\text{REF}} = 4\text{fF}, R_{\text{PDREF}} = 2.5\text{K} \)
Propagating Delay in Multiple-Levels of Logic with Stage Loading

*Equal rise-fall gates, no overdrive*

<table>
<thead>
<tr>
<th>$C_{IN}/C_{REF}$</th>
<th>Equal Rise/Fall</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inverter</td>
<td>$1$</td>
</tr>
<tr>
<td>NOR</td>
<td>$\frac{3k+1}{4}$</td>
</tr>
<tr>
<td>NAND</td>
<td>$\frac{3+k}{4}$</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Overdrive</th>
<th>Equal Rise/Fall</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inverter HL</td>
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<td>$1$</td>
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<tr>
<td>NOR HL</td>
<td>$1$</td>
</tr>
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<td></td>
<td>$1$</td>
</tr>
<tr>
<td>NAND HL</td>
<td>$1$</td>
</tr>
<tr>
<td></td>
<td>$1$</td>
</tr>
</tbody>
</table>

$$t_{PROP}/t_{REF} = \sum_{k=1}^{n} F_{I(k+1)}$$

$$t_{PROP} = t_{REF} \sum_{k=1}^{5} F_{k+1}$$
Equal rise-fall gates, no overdrive

In 0.5u proc \( t_{REF}=20ps, C_{REF}=4fF, R_{PDREF}=2.5K \)

\[
t_{PROP} = t_{REF} \sum_{k=1}^{5} F_{k+1}
\]

\[
t_{PROP} = t_{REF} (10.25 + 4.25 + 4.25 + 1.25 + 12.5)
\]

\[
t_{PROP} = 32.5t_{REF}
\]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Equal rise-fall gates, with overdrive

In 0.5u proc  \( t_{REF}=20\text{ps} \),  
\( C_{REF}=4fF, R_{PDREF}=2.5K \)

\[
t_{PROP} = t_{REF} \sum_{k=1}^{n} \frac{F_{k+1}}{OD_k}
\]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

*Equal rise-fall gates, with overdrive*

<table>
<thead>
<tr>
<th>C&lt;sub&gt;IN&lt;/sub&gt;/C&lt;sub&gt;REF&lt;/sub&gt;</th>
<th>Equal Rise/Fall</th>
<th>Equal Rise/Fall (with OD)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inverter</td>
<td>1</td>
<td>OD</td>
</tr>
<tr>
<td>NOR</td>
<td>$\frac{3k+1}{4}$</td>
<td>$\frac{3k+1}{4} \cdot OD$</td>
</tr>
<tr>
<td>NAND</td>
<td>$\frac{3+k}{4}$</td>
<td>$\frac{3+k}{4} \cdot OD$</td>
</tr>
<tr>
<td>Overdrive</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Inverter</td>
<td></td>
<td></td>
</tr>
<tr>
<td>HL</td>
<td>1</td>
<td>OD</td>
</tr>
<tr>
<td>LH</td>
<td>1</td>
<td>OD</td>
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<tr>
<td>NOR</td>
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<tr>
<td>HL</td>
<td>1</td>
<td>OD</td>
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<tr>
<td>LH</td>
<td>1</td>
<td>OD</td>
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<tr>
<td>NAND</td>
<td></td>
<td></td>
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<tr>
<td>HL</td>
<td>1</td>
<td>OD</td>
</tr>
<tr>
<td>LH</td>
<td>1</td>
<td>OD</td>
</tr>
</tbody>
</table>

$$t_{PROP}/t_{REF} = \sum_{k=1}^{n} F_{k+1}$$

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} \frac{F_{k+1}}{OD_{k}}$$
Equal rise-fall gates, with overdrive

In 0.5u proc \( t_{\text{REF}} = 20\text{ps}, \)  
\( C_{\text{REF}} = 4\text{fF}, R_{\text{PDREF}} = 2.5\text{K} \)

\[
t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^{n} \frac{F_{k+1}}{OD_k}
\]

\[
t_{\text{PROP}} = t_{\text{REF}} \left( \frac{14.25}{8} + \frac{13}{1} + \frac{4.25}{6} + \frac{5}{1} + \frac{12.5}{4} \right)
\]

\[
t_{\text{PROP}} = t_{\text{REF}} \left( 1.78 + 13 + 0.71 + 5 + 3.13 \right)
\]

\[
t_{\text{PROP}} = 23.62 t_{\text{REF}}
\]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

*Minimum-sized gates*

\[ t_{\text{PROP}} = t_{\text{REF}} \cdot ? \]

In 0.5u proc \( t_{\text{REF}}=20\,\text{ps} \), 
\( C_{\text{REF}}=4\,\text{fF} \), \( R_{\text{PDREF}}=2.5\,\text{K} \)
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Minimum-sized gates

![Diagram of logic gates with propagation delay components]

\[ t_{\text{PROP}} = t_{\text{REF}} \cdot ? \]
Propagation Delay with Minimum-Sized Gates

\[ t_{\text{PROP}} = t_{\text{REF}} \cdot \]?

\[ t_{\text{PROP}} = R_{PD} C_L + R_{PU} C_L \]

\[ t_{\text{PROP}} = \left( \frac{R_{PDREF}}{O_D_{HL}} + \frac{R_{PDREF}}{O_D_{LH}} \right) C_L \]

\[ t_{\text{PROP}} = R_{PDREF} \left( \frac{1}{O_D_{HL}} + \frac{1}{O_D_{LH}} \right) (C_{REF} F_{\text{LOAD}}) \]

\[ t_{\text{PROP}} = \left( \frac{1}{O_D_{HL}} + \frac{1}{O_D_{LH}} \right) (R_{PDREF} C_{REF}) F_{\text{LOAD}} \]

But recall

\[ t_{\text{REF}} = 2 C_{REF} R_{PDREF} \]

Thus

\[ t_{\text{PROP}} = \left( \frac{1}{O_D_{HL}} + \frac{1}{O_D_{LH}} \right) \left( \frac{t_{\text{REF}}}{2} \right) F_{\text{LOAD}} \]

Now, for \( k \) levels of logic

\[ t_{\text{PROP}} = \frac{t_{\text{REF}}}{2} \sum_{k=1}^{n} F_{(k+1)} \left( \frac{1}{O_D_{HLk}} + \frac{1}{O_D_{LHk}} \right) \]

Note: Derivation essentially identical to that used previously for gates with asymmetric OD.
Propagation Delay with Minimum-Sized Gates

\[ t_{\text{PROP}} = t_{\text{REF}} \bullet \left( \frac{1}{2} \sum_{k=1}^{n} F_{l(k+1)} \left( \frac{1}{\text{OD}_{\text{HL}k}} + \frac{1}{\text{OD}_{\text{LH}k}} \right) \right) \]

Still need \( \text{OD}_{\text{HL}} \) and \( \text{OD}_{\text{LH}} \)

Still need \( F_{l} \)
Propagation Delay with minimum-sized gates

\[ OD_{HL} = ? \]
\[ OD_{HL} = 1 \]
\[ OD_{LH} = \frac{1}{3k} \]

\[ FI = 2C_{OX}W_{\text{MIN}}L_{\text{MIN}} \]
\[ C_{\text{REF}} = 4C_{OX}W_{\text{MIN}}L_{\text{MIN}} \]
\[ FI = \frac{C_{\text{REF}}}{2} \]
Propagating Delay in Multiple-Levels of Logic with Stage Loading

**Minimum-sized gates**

<table>
<thead>
<tr>
<th>Combination</th>
<th>Equal Rise/Fall</th>
<th>Equal Rise/Fall (with OD)</th>
<th>Minimum Sized</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$C_{IN}/C_{REF}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Inverter</td>
<td>1</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>NOR</td>
<td>$\frac{3k+1}{4}$</td>
<td>$\frac{3k+1}{4} \cdot OD$</td>
<td></td>
</tr>
<tr>
<td>NAND</td>
<td>$\frac{3+k}{4}$</td>
<td>$\frac{3+k}{4} \cdot OD$</td>
<td></td>
</tr>
<tr>
<td>Overdrive</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Inverter</td>
<td>1</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>HL</td>
<td>1</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>LH</td>
<td>1</td>
<td>1</td>
<td></td>
</tr>
<tr>
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<td>1</td>
<td>1</td>
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</tr>
<tr>
<td>HL</td>
<td>1</td>
<td>1</td>
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<td>LH</td>
<td>1</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>NAND</td>
<td>1</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>HL</td>
<td>1</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>LH</td>
<td>1</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

$\begin{align*}
  OD_{HL} &= 1 \\
  OD_{HL} &= \frac{1}{k} \\
  OD_{LH} &= \frac{1}{3k} \\
  OD_{LH} &= \frac{1}{3} \\
  F_{L}=\frac{C_{REF}}{2}
\end{align*}$
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Minimum-sized gates

<table>
<thead>
<tr>
<th></th>
<th>Equal Rise/Fall</th>
<th>Equal Rise/Fall (with OD)</th>
<th>Minimum Sized</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{IN}/C_{REF}$</td>
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<td></td>
</tr>
<tr>
<td>Inverter</td>
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<td>OD</td>
<td>$1/2$</td>
</tr>
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<td>NOR</td>
<td>$\frac{3k+1}{4}$</td>
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<tr>
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</tr>
<tr>
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<td>$1$</td>
<td>OD</td>
<td>$1$</td>
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<tr>
<td>LH</td>
<td>$1$</td>
<td>OD</td>
<td>$1/3$</td>
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<td>OD</td>
<td>$1/3$</td>
</tr>
<tr>
<td>LH</td>
<td>$1$</td>
<td>OD</td>
<td></td>
</tr>
</tbody>
</table>

$t_{PROP}/t_{REF} = \sum_{k=1}^{n} \frac{F_{(k+1)}}{OD_{k}}$

$OD_{HL} = 1/k$

$OD_{LH} = 1$

$F_{L} = \frac{C_{REF}}{2}$
Minimum-sized gates

Minimum-sized gates

\[ F_{i2} = \frac{13}{2} \]

\[ F_{i3} = 1 \]

\[ F_{i4} = 1 \]

\[ F_{i5} = \frac{1}{2} \]

\[ F_{i6} = 12.5 \]

\[ t_{\text{PROP}} = t_{\text{REF}} \cdot \left( \frac{1}{2} \sum_{k=1}^{5} F_{i(k+1)} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right) \]

\[ t_{\text{PROP}} = t_{\text{REF}} \cdot \frac{1}{2} \left( \frac{13}{2} \cdot (3 + 3) + 1(12 + 1) + 1(6 + 10) + \frac{1}{2} (9 + 12.5 + 2 + 3) \right) \]

\[ t_{\text{PROP}} = 63.25 \cdot t_{\text{REF}} \]

\[ C = 50fF \]

\[ C_{\text{REF}} \]

\[ \frac{C}{C_{\text{REF}}} = \frac{50fF}{4fF} = 12.5 \]
Propagagation Delay in Multiple-Levels of Logic with Stage Loading

Asymmetric-sized gates

\[ t_{\text{PROP}} = t_{\text{REF}} \cdot ? \]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Asymmetric-sized gates

<table>
<thead>
<tr>
<th>Gate Type</th>
<th>Equal Rise/Fall</th>
<th>Equal Rise/Fall (with OD)</th>
<th>Minimum Sized</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inverter</td>
<td>1</td>
<td>OD</td>
<td>1/2</td>
</tr>
<tr>
<td>NOR</td>
<td>$\frac{3k+1}{4}$</td>
<td>$\frac{3k+1}{4} \cdot OD$</td>
<td>1/2</td>
</tr>
<tr>
<td>NAND</td>
<td>$\frac{3+k}{4}$</td>
<td>$\frac{3+k}{4} \cdot OD$</td>
<td>1/2</td>
</tr>
</tbody>
</table>

Overdrive

<table>
<thead>
<tr>
<th>Gate Type</th>
<th>Equal Rise/Fall</th>
<th>Minimum Sized</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inverter</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>HL</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>LH</td>
<td>1</td>
<td>1/3</td>
</tr>
<tr>
<td>NOR</td>
<td></td>
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<td>HL</td>
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<td>1/k</td>
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<tr>
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<td>1/3</td>
</tr>
<tr>
<td>LH</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

Following an approach similar to that used for characterizing the minimum-sized gates, the normalized input capacitance can be found.

\[
\frac{t_{\text{PROP}}}{t_{\text{REF}}} = \left( 1 + \frac{1}{2} \sum_{k=1}^{n} \frac{F_{l(k+1)}}{OD_k} \left( \frac{1}{\text{OD}_{HLk}} + \frac{1}{\text{OD}_{LHk}} \right) \right)
\]

\[
t_{\text{PROP}} = t_{\text{REF}} \cdot \left( 1 + \frac{1}{2} \sum_{k=1}^{n} \frac{F_{l(k+1)}}{OD_k} \left( \frac{1}{\text{OD}_{HLk}} + \frac{1}{\text{OD}_{LHk}} \right) \right)
\]
## Propagation Delay in Multiple-Levels of Logic with Stage Loading

### Asymmetric-sized gates

<table>
<thead>
<tr>
<th>$C_{IN}/C_{REF}$</th>
<th>Equal Rise/Fall</th>
<th>Equal Rise/Fall (with OD)</th>
<th>Minimum Sized</th>
<th>Asymmetric OD ($OD_{HL}$, $OD_{LH}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Inverter</strong></td>
<td>1</td>
<td>$OD$</td>
<td>1/2</td>
<td>$OD_{HL} + 3 \cdot OD_{LH}$</td>
</tr>
<tr>
<td>$NOR$</td>
<td>$\frac{3k+1}{4}$</td>
<td>$\frac{3k+1}{4} \cdot OD$</td>
<td>1/2</td>
<td>$OD_{HL} + 3k \cdot OD_{LH}$</td>
</tr>
<tr>
<td>$NAND$</td>
<td>$\frac{3+k}{4}$</td>
<td>$\frac{3+k}{4} \cdot OD$</td>
<td>1/2</td>
<td>$k \cdot OD_{HL} + 3 \cdot OD_{LH}$</td>
</tr>
</tbody>
</table>

| Overdrive        |                  |                           |               |                                     |
| Inverter         |                  |                           |               |                                     |
| $HL$             | 1                | $OD$                      | 1             | $OD_{HL}$                           |
| $LH$             | 1                | $OD$                      | 1/3           | $OD_{LH}$                           |
| **NOR**          |                  |                           |               |                                     |
| $HL$             | 1                | $OD$                      | 1             | $OD_{HL}$                           |
| $LH$             | 1                | $OD$                      | 1/(3k)        | $OD_{LH}$                           |
| **NAND**         |                  |                           |               |                                     |
| $HL$             | 1                | $OD$                      | 1/k           | $OD_{HL}$                           |
| $LH$             | 1                | $OD$                      | 1/3           | $OD_{LH}$                           |

$$t_{PROP}/t_{REF} = \sum_{k=1}^{n} F_{(k+1)} \cdot \frac{1}{OD_k}$$

$$t_{PROP} = t_{REF} \cdot \left( \frac{1}{2} \sum_{k=1}^{5} F_{(k+1)} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right)$$
Propagations Delay in Multiple-Levels of Logic with Stage Loading

Asymmetric-sized gates

\[ \text{PROP} = t_{\text{REF}} \cdot \left( \frac{1}{2} \sum_{k=1}^{5} F_{l(k+1)} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right) \]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

*Mixture of Minimum-sized gates, equal rise/fall gates and OD*

\[ t_{PROP} = t_{REF} \cdot ? \]
Driving Notation

- Equal rise/fall (no overdrive)
- Equal rise/fall with overdrive
- Minimum Sized
- Asymmetric Overdrive
Propagation Delay in Multiple-Levels of Logic with Stage Loading

*Mixture of Minimum-sized gates, equal rise/fall gates and OD*

\[
\begin{align*}
t_{\text{PROP}} &= t_{\text{REF}} \cdot \left( \sum_{k=1}^{5} \frac{F_{i(k+1)}}{2} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right) \\
\end{align*}
\]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

*Mixture of Minimum-sized gates, equal rise/fall gates and OD*

\[
\begin{align*}
  t_{\text{PROP}} &= t_{\text{REF}} \cdot \left( \frac{1}{2} \sum_{k=1}^{5} F_{l(k+1)} \left( \frac{1}{OD_{\text{HLk}}} + \frac{1}{OD_{\text{LHk}}} \right) \right)
\end{align*}
\]
Summary
Propagation Delay in Multiple-Levels of Logic with Stage Loading

- Equal rise/fall (no overdrive)
- Equal rise/fall with overdrive
- Minimum Sized
- Asymmetric overdrive
- Combination of equal rise/fall, minimum size and overdrive
Summary

Propagation Delay in Multiple-Levels of Logic with Stage Loading

<table>
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<th>$C_{IN}/C_{REF}$</th>
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</tr>
</tbody>
</table>

Overdrive

<table>
<thead>
<tr>
<th>$t_{PROP}/t_{REF}$</th>
<th>$\sum_{k=1}^{n} F_{i(k+1)}$</th>
<th>$\sum_{k=1}^{n} F_{i(k+1)} \cdot OD_k$</th>
<th>$\frac{1}{2} \sum_{k=1}^{n} F_{i(k+1)} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right)$</th>
<th>$\frac{1}{2} \sum_{k=1}^{n} F_{i(k+1)} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right)$</th>
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<td></td>
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<td></td>
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<td>LH</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Driving Large Capacitive Loads

Example

Assume driving by a reference inverter

Assume $C_L = 1000C_{REF}$

In 0.5u proc $t_{REF}=20\text{ps}$,
$C_{REF}=4fF, R_{PDREF}=2.5K$

$t_{PROP}=?$
Driving Large Capacitive Loads

Example

Assume driving by a reference inverter

Assume $C_L = 1000C_{REF}$

$t_{PROP} = 1000t_{REF}$

$t_{PROP}$ is too long!

In 0.5u proc $t_{REF} = 20\text{ps}$, $C_{REF} = 4\text{fF}, R_{PDREF} = 2.5\text{K}$
Driving Large Capacitive Loads

Example

Assume first stage is a reference inverter

Assume $C_L = 1000C_{REF}$

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} \frac{F_{l(k+1)}}{OD_k}$$

$$t_{PROP} = t_{REF} \sum_{k=1}^{2} \frac{F_{l(k+1)}}{OD_k}$$
Driving Large Capacitive Loads

Example

Assume first stage is a reference inverter

Assume $C_L = 1000C_{REF}$

$\sum_{k=1}^{2} I(k+1) F_{t} = t_{OD}$

$\begin{pmatrix} 111000 \\ 1000 \\ 1000 \\ 11 \\ 1000 \end{pmatrix} + = \begin{pmatrix} 1 \\ 0 \\ 0 \\ 1001 \end{pmatrix}$

$\begin{pmatrix} t_{PROP} \end{pmatrix} = \begin{pmatrix} t_{REF} \end{pmatrix} \left( \sum_{k=1}^{2} \frac{F_{t}(k+1)}{OD_{k}} \right) = t_{REF} (1000 + 1)$

$t_{PROP} = t_{REF} (1001)$

Delay of second inverter is really small but overall delay is even longer than before!
Driving Large Capacitive Loads

Example

Assume first stage is a reference inverter

Assume $C_L = 1000C_{REF}$

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} \frac{F_{l(k+1)}}{OD_k}$$

$$t_{PROP} = t_{REF} \sum_{k=1}^{3} \frac{F_{l(k+1)}}{OD_k}$$
Driving Large Capacitive Loads

Example

Assume first stage is a reference inverter

\[ \text{Assume } C_L = 1000C_{\text{REF}} \]

\[ t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^{3} \frac{F_{l(k+1)}}{OD_k} \]

\[ t_{\text{PROP}} = t_{\text{REF}} \left( \frac{1}{10} + \frac{1}{10} + \frac{1}{1000} \right) = t_{\text{REF}} \left( 10 + 10 + 10 \right) \]

\[ t_{\text{PROP}} = 30t_{\text{REF}} \]

Dramatic reduction is propagation delay (over a factor of 30!)

What is the fastest way to drive a large capacitive load?
Optimal Driving of Capacitive Loads

Assume first stage is a reference inverter

Need to determine the number of stages, n, and the OD factors for each stage to minimize $t_{PROP}$.

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} \frac{F_{I(k+1)}}{OD_k}$$

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} \frac{\theta_k}{\theta_{k-1}}$$

where $\theta_0 = 1$, $\theta_n = C_L/C_{REF}$

This becomes an n-parameter optimization (minimization) problem!

Unknown parameters: $\{\theta_1, \theta_2, ..., \theta_{n-1}, n\}$
Optimal Driving of Capacitive Loads

Assume first stage is a reference inverter

\[ t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^{n} \frac{\theta_k}{\theta_{k-1}} \]

Order reduction strategy: Assume overdrive of stages increases by the same factor clear until the load

\[ \theta^n C_{\text{REF}} = C_L \]

This becomes a 2-parameter optimization (minimization) problem!

Unknown parameters: \( \{\theta, n\} \)
End of Lecture 39
Optimal Driving of Capacitive Loads

\[ t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^{n} \frac{\theta_k}{\theta_{k-1}} \]

\[ t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^{n} \frac{\theta^k}{\theta^{k-1}} \]

\[ \theta^n C_{\text{REF}} = C_L \]

\[ t_{\text{PROP}} = t_{\text{REF}} n\theta \]

\[ \theta^n C_{\text{REF}} = C_L \]

Unknown parameters: \( \{\theta, n\} \)

Thus obtain an expression for \( t_{\text{PROP}} \) in terms of only \( \theta \)

\[ t_{\text{PROP}} = t_{\text{REF}} \left( \frac{\theta}{\ln(\theta)} \right) \left( \ln \left( \frac{C_L}{C_{\text{REF}}} \right) \right) \]
Optimal Driving of Capacitive Loads

\[ t_{\text{PROP}} = t_{\text{REF}} \frac{\theta}{\ln(\theta)} \left[ \ln \frac{C_L}{C_{\text{REF}}} \right] \]

Is suffices to minimize the function

\[ f(\theta) = \frac{\theta}{\ln(\theta)} \]

\[ \frac{df}{d\theta} = \frac{\ln(\theta) - \theta \cdot \left( \frac{1}{\theta} \right)}{(\ln(\theta))^2} = 0 \]

\[ \ln(\theta) - 1 = 0 \quad \Rightarrow \quad \theta = e \]

\[ n = \frac{1}{\ln(\theta)} \ln \left( \frac{C_L}{C_{\text{REF}}} \right) \quad \Rightarrow \quad n = \ln \left( \frac{C_L}{C_{\text{REF}}} \right) \]
Optimal Driving of Capacitive Loads

\[ \theta_{\text{OPT}} = e \]
\[ n_{\text{OPT}} = \ln \left( \frac{C_L}{C_{\text{REF}}} \right) \]
\[ t_{\text{PROP}} = t_{\text{REF}} \frac{\theta}{\ln(\theta)} \left[ \ln \frac{C_L}{C_{\text{REF}}} \right] = n\theta \]
Optimal Driving of Capacitive Loads

\[ f = \frac{\theta}{\ln(\theta)} \]

minimum at \( \theta = e \) but shallow inflection point for \( 2 < \theta < 3 \)

practically pick \( \theta = 2, \theta = 2.5, \) or \( \theta = 3 \)

since optimization may provide non-integer for \( n \), must pick close integer
Optimal Driving of Capacitive Loads

- Often termed a pad driver
- Often used to drive large internal busses as well
- Generally included in standard cells or in cell library
- Device sizes can become very large
- Odd number of stages will cause signal inversion but usually not a problem
Optimal Driving of Capacitive Loads

Example: Design a pad driver for driving a load capacitance of 10pF, determine $t_{\text{PROP}}$ for the pad driver, and compare this with the propagation delay for driving the pad with a minimum-sized reference inverter.

In 0.5u proc $t_{\text{REF}}=20\text{ps}$, $C_{\text{REF}}=4\text{fF}$, $R_{\text{PDREF}}=2.5\text{K}$

$$n_{\text{OPT}} = \ln \left( \frac{C_L}{C_{\text{REF}}} \right) = \ln \left( \frac{10\text{pF}}{4\text{fF}} \right) = 7.8$$

Select $n=8$, $\theta=2.5$

$$W_{nk} = 2.5^{k-1}, \quad W_{pk} = 3 \cdot 2.5^{k-1}$$
Optimal Driving of Capacitive Loads

Example: Design a pad driver for driving a load capacitance of 10pF, determine $t_{PROP}$ for the pad driver, and compare this with the propagation delay for driving the pad with a minimum-sized reference inverter.

In 0.5u proc $t_{REF}=20ps$, $C_{REF}=4fF$, $R_{PDREF}=2.5\,k\Omega$

$W_{nk}=2.5^{k-1}$, $W_{pk}=3\cdot2.5^{k-1}$

<table>
<thead>
<tr>
<th>$k$</th>
<th>$n$-channel</th>
<th>$L_{n}=L_p=L_{MIN}$</th>
<th>$p$-channel</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1 $W_{MIN}$</td>
<td>3 $W_{MIN}$</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>2.5 $W_{MIN}$</td>
<td>7.5 $W_{MIN}$</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>6.25 $W_{MIN}$</td>
<td>18.75 $W_{MIN}$</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>15.6 $W_{MIN}$</td>
<td>46.9 $W_{MIN}$</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>39.1 $W_{MIN}$</td>
<td>117.2 $W_{MIN}$</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>97.7 $W_{MIN}$</td>
<td>293.0 $W_{MIN}$</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>244.1 $W_{MIN}$</td>
<td>732.4 $W_{MIN}$</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>610.4 $W_{MIN}$</td>
<td>1831.1 $W_{MIN}$</td>
<td></td>
</tr>
</tbody>
</table>

Note devices in last stage are very large!
Optimal Driving of Capacitive Loads

Example: Design a pad driver for driving a load capacitance of 10pF, determine $t_{PROP}$ for the pad driver, and compare this with the propagation delay for driving the pad with a minimum-sized reference inverter.

In 0.5u proc $t_{REF}=20\text{ps}$, $C_{REF}=4\text{fF}, R_{PDREF}=2.5K$

$$t_{PROP} \approx n\theta t_{REF} = 8 \cdot 2.5 \cdot t_{REF} = 20 t_{REF}$$

More accurately:

$$t_{PROP} = t_{REF} \left( \sum_{k=1}^{7} \theta + \frac{1}{\theta} \frac{C_L}{C_{REF}} \right) = t_{REF} \left( 17.5 + \frac{1}{610} \cdot 2500 \right) = 21.6 t_{REF}$$
Optimal Driving of Capacitive Loads

Example: Design a pad driver for driving a load capacitance of 10pF, determine $t_{\text{PROP}}$ for the pad driver, and compare this with the propagation delay for driving the pad with a minimum-sized reference inverter.

In 0.5µm proc $t_{\text{REF}}=20\text{ps}$, $C_{\text{REF}}=4\text{fF}, R_{\text{PDREF}}=2.5\text{K}$

$W_{nK}=2.5^{k-1}, \quad W_{pk} = 3 \cdot 2.5^{k-1}$

If driven directly with the minimum-sized reference inverter

$$t_{\text{PROP}} = t_{\text{REF}} \frac{C_L}{C_{\text{REF}}} = 2500t_{\text{REF}}$$

Note an improvement in speed by a factor of

$$r = \frac{2500}{20} = 125$$
Propagation Delay in “Logic Effort” approach

Propagation delay for equal rise/fall gates was derived to be

\[ t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^{3} \frac{F_l(k+1)}{OD_k} \]

Delay calculations with “logical effort” approach

Author’s definition:

\[ t_{\text{PROP}} = \sum_{k=1}^{n} f_k \]

where \( f_k \) is the “effort delay” of stage \( k \)

\[ f_k = g_k h_k \]

\( g_k \) = logical effort

\( h_k \) = electrical effort
Propagation Delay in “Logic Effort” approach

\[ t_{PROP} = \sum_{k=1}^{n} f_k \quad f_k = g_k h_k \]

\( f_k \) = “effort delay” of stage \( k \)

\( g_k \) = logical effort

\( h_k \) = electrical effort

Logic Effort is the ratio of the input capacitance of a gate to the input capacitance of an inverter that can deliver the same output current.

Electrical Effort is the ratio of the gate load capacitance to the input capacitance of a gate.
Propagagation Delay in “Logic Effort” approach

$$t_{\text{PROP}} = \sum_{k=1}^{n} f_k$$

$$f_k = g_k h_k$$

Logic Effort ($g$) is the ratio of the input capacitance of a gate to the input capacitance of an inverter that can deliver the same output current.

Electrical Effort ($h$) is the ratio of the gate load capacitance to the input capacitance of a gate.

$$g_k = \frac{C_{\text{IN}_k}}{C_{\text{REF}} \cdot \text{OD}_k}$$

$$h_k = \frac{C_{\text{REF}} \cdot F_{\text{I}_k+1}}{C_{\text{IN}_k}}$$
Propagation Delay in “Logic Effort” approach

\[ t_{\text{PROP}} = \sum_{k=1}^{n} f_k \]

\[ f_k = g_k h_k \]

\[ g_k = \frac{C_{\text{IN}_k}}{C_{\text{REF} \cdot \text{OD}_k}} \]

\[ h_k = \frac{C_{\text{REF} \cdot F_{l(k+1)}}}{C_{\text{IN}_k}} \]

\[ f_k = \frac{F_{l(k+1)}}{\text{OD}_k} \]
Propagation Delay in “Logic Effort” approach

\[ t_{\text{PROP}} = \sum_{k=1}^{n} f_k = \sum_{k=1}^{n} g_k h_k = \sum_{k=1}^{n} \frac{F_k(k+1)}{OD_k} \]

- Note with the exception of the \( t_{\text{REF}} \) that was omitted in the text, this expression is identical to what we have derived previously.

- Probably more tedious to use the “Logical Effort” approach.

- Extensions to asymmetric overdrive factors may not be trivial.

- Extensions to include parasitics may be tedious as well.

- Logical Effort is widely used throughout the industry.
Elmore Delay Calculations

- Interconnects have a distributed resistance and a distributed capacitance
  - Often modeled as resistance/unit length and capacitance per unit length
- These delay the propagation of the signal
- Effectively a transmission line
  - Analysis is really complicated
- Can have much more complicated geometries
Elmore Delay Calculations

Can have much more complicated geometries
Elmore Delay Calculations

For $X_1 < X_2 < X_3$
Elmore Delay Calculations

A lumped element model of transmission line

Even this lumped model is 4-th order and a closed-form solution is very tedious!

Need a quick (and reasonably good) approximation to the delay of a delay line!!
Elmore Delay Calculations

Elmore delay: \[ t_{PD} = \sum_{i=1}^{n} \left( \sum_{j=1}^{i} C_i R_j \right) \]

- Numbering is critical (resistors and capacitors numbered from input to output)
- As stated, only applies to this specific structure
Elmore Delay Calculations

Elmore delay: \[ t_{PD} = \sum_{i=1}^{n} \left( C_i \sum_{j=1}^{i} R_j \right) \]

- Note error in text on Page 161

\[ t_{pd} = \sum_{i} R_{n-i} C_i = \sum_{i=1}^{N} C_i \sum_{j=i}^{i} R_j \]
Elmore Delay Calculations

Elmore delay[1] is a simple approximation to the delay through an RC network in an electronic system. It is often used in applications such as logic synthesis, delay calculation, static timing analysis, placement and routing, since it is simple to compute (especially in tree structured networks, which are the vast majority of signal nets within ICs) and is reasonably accurate. Even where it is not accurate, it is usually faithful, in the sense that reducing the Elmore delay will almost always reduce the true delay, so it is still useful in optimization.

From Wikipedia:

Elmore delay[1] is a simple approximation to the delay through an RC network in an electronic system. It is often used in applications such as logic synthesis, delay calculation, static timing analysis, placement and routing, since it is simple to compute (especially in tree structured networks, which are the vast majority of signal nets within ICs) and is reasonably accurate. Even where it is not accurate, it is usually faithful, in the sense that reducing the Elmore delay will almost always reduce the true delay, so it is still useful in optimization.

Elmore Delay Calculations

Example:

\[
\begin{align*}
\text{Elmore delay:} & \quad t_{PD} = \sum_{i=1}^{4} \left( C_i \sum_{j=1}^{i} R_j \right) \\
& \quad t_{PD} = \sum_{i=1}^{4} (t_i) \\
& \text{where} \quad t_i = C_i \sum_{j=1}^{i} R_j \quad j = 1, 2, 3, 4
\end{align*}
\]

What is really happening?

- Creating 4 first-order circuits
- Delay to \(V_1, V_2, V_3\) and \(V_4\) calculated separately by considering capacitors one at a time and assuming others are 0
Elmore Delay Calculations

Extensions:

Lumped Network Model:
Elmore Delay Calculations

Extensions:

1. Create a lumped element model

![Lumped Element Model Diagram]

2. Create a path from input to output

![Path Diagram]
Elmore Delay Calculations

Extensions:

3. Renumber elements along path from input to output and neglect off-path elements

4. Use Elmore Delay equation for elements on this RC network

\[ t_{PD} = \sum_{i=1}^{4} \left( C_i \sum_{j=1}^{i} R_j \right) \]
Elmore Delay Calculations

How is a resistive load handled?
Elmore Delay Calculations

Example with resistive load:

Elmore delay:

\[ t_{PD} = \sum_{i=1}^{4} \left( C_i \sum_{j=1}^{i} R_j \right) \]

where

\[ t_{PD} = \sum_{i=1}^{4} (t_i) \]

\[ t_i = C_i \sum_{j=1}^{i} R_j \quad j = 1, 2, 3 \]

\[ t_4 = C_4 \left( \frac{\sum_{j=1}^{4} R_j}{\sum_{j=1}^{4} R_j} \right) / R_5 \]
Elmore Delay Calculations

With resistive load:

Elmore delay: \[ t_{PD} = \sum_{i=1}^{n-1} \left( C_i \sum_{j=1}^{i} R_j \right) + C_n \left( \frac{\sum_{j=1}^{n} R_j}{R_L} \right) \]
Ring Oscillators
Device Sizing

Multiple Input Gates: