EE 330
Lecture 39
Digital Circuits

Propagation Delay in Multiple Levels of Logic
Optimally Driving Large Capacitive Loads
Digital Circuit Design

- Hierarchical Design
- Basic Logic Gates
- Properties of Logic Families
- Characterization of CMOS Inverter
- Static CMOS Logic Gates
  - Ratio Logic
- Propagation Delay
  - Simple analytical models
  - Elmore Delay
- Sizing of Gates

- Propagation Delay with Multiple Levels of Logic
- Optimal driving of Large Capacitive Loads
- Power Dissipation in Logic Circuits
- Other Logic Styles
- Array Logic
- Ring Oscillators
Review from last time

Propagation Delay in Multiple-Levels of Logic with Stage Loading

Analysis strategy: Express delays in terms of those of reference inverter

\[ C_{\text{REF}} = C_{\text{IN}} = 4C_{\text{OX}}W_{\text{MIN}}L_{\text{MIN}} \]

\[ R_{\text{PDREF}} = \frac{L_{\text{MIN}}}{\mu_n C_{\text{OX}} W_{\text{MIN}} (V_{\text{DD}} - V_{Tn})} \quad V_{Tn} = 0.8V_{\text{DD}} \]

\[ t_{\text{REF}} = t_{\text{HLREF}} + t_{\text{LHREF}} = 2R_{\text{PDREF}} C_{\text{REF}} \]

\[ L_n = L_p = L_{\text{MIN}} \]

Reference Inverter

Assume \( \mu_n/\mu_p = 3 \)

\[ W_n = W_{\text{MIN}}, \quad W_p = 3W_{\text{MIN}} \]

In 0.5u proc \( t_{\text{REF}} = 20\text{ps}, \quad C_{\text{REF}} = 4fF, \quad R_{\text{PDREF}} = 2.5\text{K} \)
Propagation Delay with Stage Loading

**Review from last time**

Propagates Delay $t_{REF} = 2R_{PD_{ref}} C_{REF}$

$C_{REF} = C_{IN} = 4C_{OX} W_{MIN} L_{MIN}$

**Fl of a capacitor**

$F_{IC} = \frac{C}{C_{REF}}$

**Fl of a gate (input k)**

$F_{IG} = \frac{C_{INK}}{C_{REF}}$

**Fl of an interconnect**

$F_{I_i} = \frac{C_{I_{INi}}}{C_{REF}}$

**Overall Fl**

$F_I = \sum_{\text{Gates}} C_{INGi} + \sum_{\text{Capacitances}} C_{INCi} + \sum_{\text{Interconnects}} C_{INli}$
Review from last time

Propagation Delay Through Multiple Stages of Logic with Stage Loading

(assuming gate drives are all same as that of reference inverter)

Identify the gate path from A to F

\[ t_{\text{PROP}k} = t_{\text{REF}} F_{I(k+1)} \]

Propagation delay from A to F:

\[ t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^{n} F_{I(k+1)} \]
Overdrive Factors

The factor by which the devices are scaled above those of the reference inverter is termed the overdrive factor, OD.

Scaling all widths by a constant does not compromise the symmetry between the rise and fall times.

Judicious use of overdrive can dramatically improve the speed of digital circuits.

Large overdrive factors are often used.
Define the Asymmetric Overdrive Factors of the stage to be the factor by which PU and PD resistors are scaled relative to those of the reference inverter.

\[
R_{\text{PDEFF}} = \frac{R_{\text{PDREF}}}{OD_{\text{HL}}} \quad R_{\text{PUEFF}} = \frac{R_{\text{PUREF}}}{OD_{\text{LH}}}
\]

If inverter sized for equal rise/fall, define OD by \(OD_{\text{HL}} = OD_{\text{LH}} = OD\)

\[
t_{\text{HL}} = t_{\text{LH}} = \frac{R_{\text{PDREF}}}{OD} C_L = R_{\text{PDREF}} C_{\text{REF}} \frac{F_{\text{IL}}}{OD}
\]

\[
t_{\text{PROP}} = t_{\text{LH}} + t_{\text{HL}} = t_{\text{REF}} \frac{F_{\text{IL}}}{OD}
\]

OD may be larger or smaller than 1
Propagation Delay with Over-drive Capability

Example

Compare the propagation delays. Assume the OD is 900 in the second case and 30 in the third case.

\[ V_{IN} \rightarrow O_D \rightarrow V_{OUT} \]

\[ C_L = 900C_{REF} \]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Notation:

\[ t_k = t_{PROP_k} \]

Propagation delay from A to F:

\[ t_{PROP} = t_{REF} \sum_{k=1}^{n} \frac{F_{l(k+1)}}{OD_k} \]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Will consider an example with the five cases

- Equal rise/fall (no overdrive)
- Equal rise/fall with overdrive
- Minimum Sized
- Asymmetric Overdrive
- Combination of equal rise/fall, minimum size and overdrive

Will develop the analysis methods as needed
Propagation Delay in Multiple-Levels of Logic with Stage Loading

- Equal rise/fall (no overdrive)
- Equal rise/fall with overdrive
- Minimum Sized
- Asymmetric overdrive

Combination of equal rise/fall, minimum size and overdrive
Drive Notation

- Equal rise/fall (no overdrive)
- Equal rise/fall with overdrive
- Minimum Sized
- Asymmetric Overdrive

Notation will be used only if it is not clear from the context what sizing is being used
Define the Asymmetric Overdrive Factors of the stage to be the factors by which PU and PD resistors are scaled relative to those of the reference inverter.

Recall:

\[
R_{PDEFF} = \frac{R_{PDREF}}{OD_{HL}} \quad \quad R_{PUEFF} = \frac{R_{PUREF}}{OD_{LH}}
\]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Asymmetric Overdrive

\[ V_{IN} \xrightarrow{\text{V}} V_{OUT} \]

\[ C_L \]

\[ t_{PROP} = t_{HL} + t_{LH} = t_{REF} \frac{F_{IL}}{OD} \]

If inverter is not equal rise/fall

\[ t_{HL} = \frac{R_{PDREF}}{OD_{HL}} C_L = \frac{1}{2} t_{REF} \frac{F_{IL}}{OD_{HL}} \]

\[ t_{LH} = \frac{R_{PUREF}}{OD_{LH}} C_L = \frac{1}{2} t_{REF} \frac{F_{IL}}{OD_{LH}} \]

\[ t_{PROP} = t_{HL} + t_{LH} = \frac{1}{2} t_{REF} F_{IL} \left( \frac{1}{OD_{HL}} + \frac{1}{OD_{LH}} \right) \]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

**Overdrive Notation**

Equal Rise/Fall with overdrive OD

Rise/Fall may be different with overdrive $OD_{HL}$ and $OD_{LH}$

**Examples**

Equal Rise/Fall with overdrive of 8

If $W_n = W_{MIN}$, minimum sized inverter
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Equal rise-fall gates, no overdrive

$t_{\text{REF}} = 2t_{\text{HLREF}}$

$t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^{n} F_{k+1}$

In 0.5u proc  $t_{\text{REF}} = 20\text{ps}$,  
$C_{\text{REF}} = 4\text{fF}$, $R_{\text{PDREF}} = 2.5\text{K}$
Propagation Delay in Multiple-Levels of Logic with Stage Loading

*Equal rise-fall gates, no overdrive*

<table>
<thead>
<tr>
<th>( C_{IN}/C_{REF} )</th>
<th>Equal Rise/Fall</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inverter</td>
<td>1</td>
</tr>
<tr>
<td>( 3k+1 )</td>
<td></td>
</tr>
<tr>
<td>( 3+k )</td>
<td></td>
</tr>
<tr>
<td>NOR</td>
<td>( \frac{4}{3} )</td>
</tr>
<tr>
<td>( \frac{4}{3} )</td>
<td></td>
</tr>
<tr>
<td>NAND</td>
<td>( \frac{k}{4} )</td>
</tr>
<tr>
<td>( \frac{k}{4} )</td>
<td></td>
</tr>
</tbody>
</table>

**Overdrive**

<table>
<thead>
<tr>
<th>( \text{Inverter} )</th>
<th>( \text{NOR} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>HL</td>
<td>( 1 )</td>
</tr>
<tr>
<td>( 1 )</td>
<td></td>
</tr>
<tr>
<td>LH</td>
<td>( 1 )</td>
</tr>
<tr>
<td>( 1 )</td>
<td></td>
</tr>
</tbody>
</table>

\[
\begin{align*}
C_{IN}/C_{REF} & = \frac{\sum_{k=1}^{n} F_{(k+1)}}{t_{PROP}/t_{REF}} \\
t_{PROP} & = t_{REF} \sum_{k=1}^{5} F_{k+1}
\end{align*}
\]
Equal rise-fall gates, no overdrive

In 0.5um proc $t_{REF} = 20\text{ps}$, $C_{REF} = 4\text{fF}, R_{PDREF} = 2.5\text{K}

$t_{PROP} = t_{REF} \sum_{k=1}^{5} F_{k+1}$

$t_{PROP} = t_{REF} (10.25 + 4.25 + 4.25 + 1.25 + 12.5)$

$t_{PROP} = 32.5t_{REF}$

$F_{l2} = 10.25$
$F_{l3} = 4.25$
$F_{l4} = 4.25$
$F_{l5} = 1.25$
$F_{l6} = 12.5$
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Equal rise-fall gates, with overdrive

In 0.5μm process, $t_{REF} = 20$ ps, $C_{REF} = 4$ fF, $R_{PDREF} = 2.5$ K

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} \frac{F_{k+1}}{OD_k}$$
Propagation Delay in Multiple-Levels of Logic with Stage Loading

*Equal rise-fall gates, with overdrive*

<table>
<thead>
<tr>
<th>$C_{IN}/C_{REF}$</th>
<th>Equal Rise/Fall</th>
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<tbody>
<tr>
<td><strong>Inverter</strong></td>
<td>1</td>
<td>OD</td>
</tr>
<tr>
<td><strong>NOR</strong></td>
<td>$\frac{3k+1}{4}$</td>
<td>$\frac{3k+1}{4} \cdot OD$</td>
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<td><strong>NAND</strong></td>
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<td>$\frac{3+k}{4} \cdot OD$</td>
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<table>
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<tr>
<th>Overdrive</th>
<th></th>
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<tbody>
<tr>
<td><strong>Inverter</strong></td>
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<td></td>
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<tr>
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</tbody>
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$t_{PROP}/t_{REF} = \sum_{k=1}^{n} F_{i(k+1)}$  
$t_{PROP} = t_{REF} \sum_{k=1}^{n} \frac{F_{i(k+1)}}{\text{OD}_{k}}$
Equal rise-fall gates, with overdrive

In 0.5u proc $t_{\text{REF}}=20\text{ps}$, $C_{\text{REF}}=4fF, R_{PD\text{REF}}=2.5K$
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Minimum-sized gates

In 0.5u proc  \( t_{\text{REF}}=20\text{ps}, \)
\( C_{\text{REF}}=4\text{fF}, R_{P_{\text{DREF}}}=2.5\text{K} \)
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Minimum-sized gates

\[ t_{PROP} = t_{REF} \cdot \frac{50 \text{fF}}{20 \text{fF}} \]
Propagation Delay with Minimum-Sized Gates

\[ t_{\text{PROP}} = t_{\text{REF}} \cdot ? \]

\[ t_{\text{PROP}} = R_{\text{PD}} C_L + R_{\text{PU}} C_L \]

\[ t_{\text{PROP}} = \left( \frac{R_{\text{PDREF}}}{O_{DH}} + \frac{R_{\text{PDREF}}}{O_{DL}} \right) C_L \]

\[ t_{\text{PROP}} = R_{\text{PDREF}} \left( \frac{1}{O_{DH}} + \frac{1}{O_{DL}} \right) (C_{\text{REF}} F_{\text{LOAD}}) \]

\[ t_{\text{PROP}} = \left( \frac{1}{O_{DH}} + \frac{1}{O_{DL}} \right) \left( R_{\text{PDREF}} C_{\text{REF}} \right) F_{\text{LOAD}} \]

But recall

\[ t_{\text{REF}} = 2C_{\text{REF}} R_{\text{PDREF}} \]

Thus

\[ t_{\text{PROP}} = \left( \frac{1}{O_{DH}} + \frac{1}{O_{DL}} \right) \left( t_{\text{REF}} \frac{1}{2} \right) F_{\text{LOAD}} \]

Now, for \( k \) levels of logic

\[ t_{\text{PROP}} = \frac{t_{\text{REF}}}{2} \sum_{k=1}^{n} F_{\text{l}(k+1)} \left( \frac{1}{O_{DHk}} + \frac{1}{O_{DLk}} \right) \]

\[ t_{\text{PROP}} = t_{\text{REF}} \cdot \left( \frac{1}{2} \sum_{k=1}^{n} F_{\text{l}(k+1)} \left( \frac{1}{O_{DHk}} + \frac{1}{O_{DLk}} \right) \right) \]
Propagation Delay with Minimum-Sized Gates

\[ t_{\text{PROP}} = t_{\text{REF}} \cdot \left( \frac{1}{2} \sum_{k=1}^{n} F_{l(k+1)} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right) \]

Still need \( OD_{HL} \) and \( OD_{LH} \)

Still need \( F_{l} \)
Propagation Delay with minimum-sized gates

$$\text{OD}_{HL} = 1$$

$$\text{OD}_{LH} = \frac{1}{3k}$$

$$\text{OD}_{HL} = \frac{1}{k}$$

$$\text{OD}_{LH} = \frac{1}{3}$$

$$\text{FI} = 2 \text{C}_{OX} W_{\text{MIN}} L_{\text{MIN}}$$

$$\text{C}_{\text{REF}} = 4 \text{C}_{OX} W_{\text{MIN}} L_{\text{MIN}}$$

$$\text{FI} = \frac{\text{C}_{\text{REF}}}{2}$$
Propagation Delay in Multiple-Levels of Logic with Stage Loading

**Minimum-sized gates**

<table>
<thead>
<tr>
<th></th>
<th>( C_{IN}/C_{REF} )</th>
<th>Equal Rise/Fall</th>
<th>Equal Rise/Fall (with OD)</th>
<th>Minimum Sized</th>
</tr>
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<tbody>
<tr>
<td>Inverter</td>
<td>1</td>
<td></td>
<td>OD</td>
<td></td>
</tr>
<tr>
<td>NOR</td>
<td>( \frac{3k+1}{4} )</td>
<td></td>
<td>OD</td>
<td></td>
</tr>
<tr>
<td>NAND</td>
<td>( \frac{3+k}{4} )</td>
<td></td>
<td>OD</td>
<td></td>
</tr>
<tr>
<td>Overdrive</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Inverter</td>
<td>1</td>
<td></td>
<td>OD</td>
<td></td>
</tr>
<tr>
<td>HL</td>
<td></td>
<td></td>
<td>OD</td>
<td></td>
</tr>
<tr>
<td>LH</td>
<td>1</td>
<td></td>
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<td>OD</td>
<td></td>
</tr>
<tr>
<td>( t_{PROP}/t_{REF} )</td>
<td>( \sum_{k=1}^{n} F_{(k+1)} )</td>
<td>( \sum_{k=1}^{n} \frac{F_{(k+1)}}{OD_k} )</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

\[
OD_{HL} = 1
\]

\[
OD_{LH} = \frac{1}{3k}
\]

\[
OD_{HL} = \frac{1}{k}
\]

\[
OD_{LH} = \frac{1}{3}
\]

\[
F_{L} = \frac{C_{REF}}{2}
\]
## Propagation Delay in Multiple-Levels of Logic with Stage Loading

### Minimum-sized gates

<table>
<thead>
<tr>
<th></th>
<th>Equal Rise/Fall</th>
<th>Equal Rise/Fall (with OD)</th>
<th>Minimum Sized</th>
</tr>
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<tbody>
<tr>
<td></td>
<td>$C_{IN}/C_{REF}$</td>
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<td></td>
</tr>
<tr>
<td>Inverter</td>
<td>1</td>
<td>OD</td>
<td>1/2</td>
</tr>
<tr>
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<td>$\frac{3k+1}{4}$</td>
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</tr>
<tr>
<td>NAND</td>
<td>$\frac{3+k}{4}$</td>
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</tr>
<tr>
<td>Inverter</td>
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<td></td>
</tr>
<tr>
<td>LH</td>
<td>1</td>
<td>OD</td>
<td>1/3</td>
</tr>
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<tr>
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<td>1</td>
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<td>1/3</td>
</tr>
</tbody>
</table>

$$t_{PROP}/t_{REF} = \sum_{k=1}^{n} \frac{F_{i(k+1)}}{OD_k}$$

$$\text{OD}_{HL} = 1$$

$$\text{OD}_{LH} = \frac{1}{3k}$$

$$\text{OD}_{HL} = 1/k$$

$$\text{OD}_{LH} = \frac{1}{3}$$

$$F_I = \frac{C_{REF}}{2}$$
Minimum-sized gates

\[
\begin{align*}
F_{i2} &= \frac{13}{2} \\
F_{i3} &= 1 \\
F_{i4} &= 1 \\
F_{i5} &= \frac{1}{2} \\
F_{i6} &= 12.5
\end{align*}
\]

\[
t_{\text{PROP}} = t_{\text{REF}} \cdot \left( \frac{1}{2} \sum_{k=1}^{5} F_{i(k+1)} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right)
\]

\[
t_{\text{PROP}} = \frac{1}{2} \left( \frac{13}{3} \cdot 3 + 1(12+1) + 1(6+10) + \frac{1}{2} (9+1) + 12.5(2+3) \right)
\]

\[
t_{\text{PROP}} = 63.25 \cdot t_{\text{REF}}
\]

\[
\frac{C}{C_{\text{REF}}} \rightarrow \frac{20fF}{4fF} = 5
\]

\[
\frac{C}{C_{\text{REF}}} \rightarrow \frac{50fF}{4fF} = 12.5
\]

50fF

A

20fF
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Asymmetric-sized gates

\[ t_{PROP} = t_{REF} \cdot \text{?} \]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Asymmetric-sized gates

<table>
<thead>
<tr>
<th>C_{IN}/C_{REF}</th>
<th>Equal Rise/Fall</th>
<th>Equal Rise/Fall (with OD)</th>
<th>Minimum Sized</th>
<th>Asymmetric OD (OD_{HL}, OD_{LH})</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inverter</td>
<td>1</td>
<td>OD</td>
<td>1/2</td>
<td>OD_{HL} + 3 \cdot OD_{LH}</td>
</tr>
<tr>
<td>NOR</td>
<td>\frac{3k+1}{4}</td>
<td>\frac{3k+1}{4} \cdot OD</td>
<td>1/2</td>
<td>OD_{HL} + 3k \cdot OD_{LH}</td>
</tr>
<tr>
<td>NAND</td>
<td>\frac{3+k}{4}</td>
<td>\frac{3+k}{4} \cdot OD</td>
<td>1/2</td>
<td>\frac{k}{4} \cdot OD_{HL} + 3 \cdot OD_{LH}</td>
</tr>
</tbody>
</table>

Overdrive

| Inverter       | HL             | OD                        | 1             | OD_{HL} |
|                | LH             | OD                        | 1/3           | OD_{LH} |
| NOR            | HL             | OD                        | 1             | OD_{HL} |
|                | LH             | OD                        | 1/(3k)        | OD_{LH} |
| NAND           | HL             | OD                        | 1/k           | OD_{HL} |
|                | LH             | OD                        | 1/3           | OD_{LH} |

\[
t_{PROP}/t_{REF} = \sum_{k=1}^{n} F_{i(k+1)} \cdot \frac{1}{OD_k} \quad \sum_{k=1}^{n} F_{i(k+1)} \cdot \frac{1}{OD_k} = \frac{1}{2} \sum_{k=1}^{n} F_{i(k+1)} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right)
\]

\[
t_{PROP} = t_{REF} \cdot \left( \frac{1}{2} \sum_{k=1}^{n} F_{i(k+1)} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right)
\]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Asymmetric-sized gates

\[
{t_{\text{PROP}}} = t_{\text{REF}} \cdot \left( \frac{1}{2} \sum_{k=1}^{5} F_{l(k+1)} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right)
\]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

*Mixture of Minimum-sized gates, equal rise/fall gates and OD*

$t_{PROP} = t_{REF} \cdot ?$
Driving Notation

- Equal rise/fall (no overdrive)

- Equal rise/fall with overdrive

- Minimum Sized

- Asymmetric Overdrive
Propagation Delay in Multiple-Levels of Logic with Stage Loading

*Mixture of Minimum-sized gates, equal rise/fall gates and OD*

\[ t_{\text{PROP}} = t_{\text{REF}} \cdot \left( \frac{1}{2} \sum_{k=1}^{5} F_{(k+1)} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right) \]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

*Mixture of Minimum-sized gates, equal rise/fall gates and OD*

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t_{\text{PROP}} = t_{\text{REF}} \cdot \left( \frac{1}{2} \sum_{k=1}^{5} F_{l(k+1)} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right)
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Propagation Delay in Multiple-Levels of Logic with Stage Loading

- Equal rise/fall (no overdrive)

- Equal rise/fall with overdrive

- Minimum Sized

- Asymmetric overdrive

Combination of equal rise/fall, minimum size and overdrive
Define the Overdrive Factor of the stage to be the factor by which PU and PD resistors are scaled relative to those of the reference inverter.

\[ R_{PDEFF} = \frac{R_{PDREF}}{OD_{HL}} \quad R_{PUEFF} = \frac{R_{PUREF}}{OD_{LH}} \]

If inverter sized for equal rise/fall, \( OD_{HL} = OD_{LH} = OD \)

\[ t_{HL} = t_{LH} = \frac{R_{PDREF}}{OD} C_{L} = R_{PDREF} C_{REF} \frac{F_{IL}}{OD} \]

\[ t_{PROP} = t_{LH} + t_{HL} = t_{REF} \frac{F_{IL}}{OD} \]

OD may be larger or smaller than 1.
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Overdrive

If inverter is not equal rise/fall

\[ t_{\text{PROP}} = t_{\text{HL}} + t_{\text{IL}} = t_{\text{REF}} \frac{F_{\text{IL}}}{OD} \]

\[ t_{\text{HL}} = \frac{R_{\text{PDREF}}}{OD_{\text{HL}}} C_{L} = \frac{1}{2} t_{\text{REF}} \frac{F_{\text{IL}}}{OD_{\text{HL}}} \]

\[ t_{\text{IL}} = \frac{R_{\text{PUREF}}}{OD_{\text{IL}}} C_{L} = \frac{1}{2} t_{\text{REF}} \frac{F_{\text{IL}}}{OD_{\text{IL}}} \]

\[ t_{\text{PROP}} = t_{\text{HL}} + t_{\text{IL}} = \frac{1}{2} t_{\text{REF}} F_{\text{IL}} \left( \frac{1}{OD_{\text{HL}}} + \frac{1}{OD_{\text{IL}}} \right) \]
Driving Large Capacitive Loads

Example

Assume CL = 1000CREF

In 0.5u proc tREF = 20ps, CREF = 4fF, RPREF = 2.5K
Driving Large Capacitive Loads

Example

Assume driving by a reference inverter

Assume $C_L = 1000C_{REF}$

$t_{PROP} = 1000t_{REF}$

t$_{PROP}$ is too long!

In 0.5u proc $t_{REF} = 20\text{ps}$,
$C_{REF} = 4\text{fF}, R_{PDREF} = 2.5\text{K}$
Driving Large Capacitive Loads

Example

Assume first stage is a reference inverter

\[ t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^{n} \frac{F_{I(k+1)}}{\text{OD}_k} \]

Assume \( C_L = 1000 C_{\text{REF}} \)

\[ t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^{2} \frac{F_{I(k+1)}}{\text{OD}_k} \]
Driving Large Capacitive Loads

Example

Assume first stage is a reference inverter

Assume $C_L = 1000 C_{REF}$

$$t_{PROP} = \sum_{k=1}^{2} \frac{F_{l(k+1)}}{OD_k}$$

$$t_{PROP} = t_{REF} \left( \frac{1}{1000} + \frac{1}{1000} \right) = t_{REF} (1000 + 1)$$

$$t_{PROP} = t_{REF} (1001)$$

Delay of second inverter is really small but overall delay is even longer than before!
Driving Large Capacitive Loads

Example

Assume first stage is a reference inverter

\[ t_{\text{PROP}} = ? \]

\[ t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^{n} \frac{F_{l(k+1)}}{OD_k} \]

Assume \( C_L = 1000C_{\text{REF}} \)

\[ t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^{3} \frac{F_{l(k+1)}}{OD_k} \]
Driving Large Capacitive Loads

Example

Assume first stage is a reference inverter

Assume \( C_L = 1000C_{REF} \)

\[
\begin{align*}
\sum_{k=1}^{3} I(k+1) & \text{PROP REF} \\
F t = t_{OD} \end{align*}
\]

\[
\begin{align*}
t_{PROP} = & t_{REF} \sum_{k=1}^{3} \frac{F_{l(k+1)}}{OD_k} \\
& \left( \frac{1}{10} + \frac{1}{100} + \frac{1}{1000} \right) = t_{REF} \left( 10 + 10 + 10 \right) \\
& t_{PROP} = 30t_{REF}
\end{align*}
\]

Dramatic reduction is propagation delay (over a factor of 30!)

What is the fastest way to drive a large capacitive load?
Optimal Driving of Capacitive Loads

Assume first stage is a reference inverter

Need to determine the number of stages, \( n \), and the OD factors for each stage to minimize \( t_{\text{PROP}} \).

\[
\begin{align*}
t_{\text{PROP}} &= t_{\text{REF}} \sum_{k=1}^{n} \frac{F_{l(k+1)}}{\text{OD}_k} \\
&= t_{\text{REF}} \sum_{k=1}^{n} \frac{\theta_k}{\theta_{k-1}}
\end{align*}
\]

where \( \theta_0 = 1 \), \( \theta_n = \frac{C_L}{C_{\text{REF}}} \)

This becomes an \( n \)-parameter optimization (minimization) problem!

Unknown parameters: \( \{\theta_1, \theta_2, \ldots, \theta_{n-1}, n\} \)
Optimal Driving of Capacitive Loads

Assume first stage is a reference inverter

Order reduction strategy: Assume overdrive of stages increases by the same factor clear until the load

This becomes a 2-parameter optimization (minimization) problem!

Unknown parameters: \( \{\theta, n\} \)

With one constraint \( \theta^n C_{\text{REF}} = C_L \)
Optimal Driving of Capacitive Loads

\[
t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^{n} \frac{\theta_k}{\theta_{k-1}}
\]

Unknown parameters: \( \{\theta, n\} \)

Thus obtain an expression for \( t_{\text{PROP}} \) in terms of only \( \theta \)

\[
t_{\text{PROP}} = t_{\text{REF}} n \theta
\]

\[
\theta^n C_{\text{REF}} = C_L
\]

\[
n = \frac{1}{\ln(\theta)} \ln \left( \frac{C_L}{C_{\text{REF}}} \right)
\]

\[
t_{\text{PROP}} = t_{\text{REF}} \frac{\theta}{\ln(\theta)} \left[ \ln \left( \frac{C_L}{C_{\text{REF}}} \right) \right]
\]
Optimal Driving of Capacitive Loads

\[ t_{\text{PROP}} = t_{\text{REF}} \frac{\theta}{\ln(\theta)} \left[ \ln \frac{C_L}{C_{\text{REF}}} \right] \]

It suffices to minimize the function

\[ f(\theta) = \frac{\theta}{\ln(\theta)} \]

\[ \frac{df}{d\theta} = \frac{\ln(\theta) - \theta \cdot \left( \frac{1}{\theta} \right)}{(\ln(\theta))^2} = 0 \]

\[ \ln(\theta) - 1 = 0 \quad \rightarrow \quad \theta = e \]

\[ n = \frac{1}{\ln(\theta)} \ln \left( \frac{C_L}{C_{\text{REF}}} \right) \quad \rightarrow \quad n = \ln \left( \frac{C_L}{C_{\text{REF}}} \right) \]
Optimal Driving of Capacitive Loads

\[ \theta_{OPT} = e \]

\[ n_{OPT} = \ln \left( \frac{C_L}{C_{REF}} \right) \]

\[ t_{PROP} = t_{REF} \frac{\theta}{\ln(\theta)} \ln \left( \frac{C_L}{C_{REF}} \right) = t_{REF} e \ln \left( \frac{C_L}{C_{REF}} \right) = n\theta \]
Optimal Driving of Capacitive Loads

\[ f = \frac{\theta}{\ln(\theta)} \]

minimum at \( \theta = e \) but shallow inflection point for \( 2 < \theta < 3 \)

practically pick \( \theta = 2, \theta = 2.5, \) or \( \theta = 3 \)

since optimization may provide non-integer for \( n \), must pick close integer
Optimal Driving of Capacitive Loads

- Often termed a pad driver
- Often used to drive large internal busses as well
- Generally included in standard cells or in cell library
- Device sizes can become very large
- Odd number of stages will cause signal inversion but usually not a problem
Optimal Driving of Capacitive Loads

Example: Design a pad driver for driving a load capacitance of 10pF, determine $t_{\text{PROP}}$ for the pad driver, and compare this with the propagation delay for driving the pad with a minimum-sized reference inverter.

In 0.5u proc $t_{\text{REF}}=20\text{ps}$, $C_{\text{REF}}=4\text{fF}$, $R_{\text{PDREF}}=2.5\text{K}$

$$n_{\text{OPT}} = \ln \left( \frac{C_L}{C_{\text{REF}}} \right) = \ln \left( \frac{10\text{pF}}{4\text{fF}} \right) = 7.8$$

Select $n=8$, $\theta=2.5$

$$W_{nk} = 2.5^{k-1}, \quad W_{pk} = 3 \cdot 2.5^{k-1}$$
Optimal Driving of Capacitive Loads

Example: Design a pad driver for driving a load capacitance of 10pF, determine $t_{\text{PROP}}$ for the pad driver, and compare this with the propagation delay for driving the pad with a minimum-sized reference inverter.

In 0.5u proc, $t_{\text{REF}}=20\text{ps}$, $C_{\text{REF}}=4\text{fF}, R_{\text{PDREF}}=2.5\text{k}$

$W_{nk}=2.5^{k-1}$, $W_{pk}=3 \cdot 2.5^{k-1}$

<table>
<thead>
<tr>
<th>$k$</th>
<th>n-channel</th>
<th>$W_{\text{MIN}}$</th>
<th>$p$-channel</th>
<th>$W_{\text{MIN}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>$W_{\text{MIN}}$</td>
<td>3</td>
<td>$W_{\text{MIN}}$</td>
</tr>
<tr>
<td>2</td>
<td>2.5</td>
<td>$W_{\text{MIN}}$</td>
<td>7.5</td>
<td>$W_{\text{MIN}}$</td>
</tr>
<tr>
<td>3</td>
<td>6.25</td>
<td>$W_{\text{MIN}}$</td>
<td>18.75</td>
<td>$W_{\text{MIN}}$</td>
</tr>
<tr>
<td>4</td>
<td>15.6</td>
<td>$W_{\text{MIN}}$</td>
<td>46.9</td>
<td>$W_{\text{MIN}}$</td>
</tr>
<tr>
<td>5</td>
<td>39.1</td>
<td>$W_{\text{MIN}}$</td>
<td>117.2</td>
<td>$W_{\text{MIN}}$</td>
</tr>
<tr>
<td>6</td>
<td>97.7</td>
<td>$W_{\text{MIN}}$</td>
<td>293.0</td>
<td>$W_{\text{MIN}}$</td>
</tr>
<tr>
<td>7</td>
<td>244.1</td>
<td>$W_{\text{MIN}}$</td>
<td>732.4</td>
<td>$W_{\text{MIN}}$</td>
</tr>
<tr>
<td>8</td>
<td>610.4</td>
<td>$W_{\text{MIN}}$</td>
<td>1831.1</td>
<td>$W_{\text{MIN}}$</td>
</tr>
</tbody>
</table>

Note devices in last stage are very large!
Optimal Driving of Capacitive Loads

Example: Design a pad driver for driving a load capacitance of 10pF, determine $t_{\text{PROP}}$ for the pad driver, and compare this with the propagation delay for driving the pad with a minimum-sized reference inverter.

In 0.5u proc $t_{\text{REF}}=20\text{ps}$, $C_{\text{REF}}=4\text{fF}$, $R_{\text{PDREF}}=2.5\text{K}$

$W_{nk}=2.5^{k-1}$, $W_{pk} = 3 \cdot 2.5^{k-1}$

$t_{\text{PROP}} = n \theta t_{\text{REF}} = 8 \cdot 2.5 \cdot t_{\text{REF}} = 20t_{\text{REF}}$

More accurately:

$t_{\text{PROP}} = t_{\text{REF}} \left( \sum_{k=1}^{7} \theta + \frac{1}{\theta^{7}} \frac{C_{L}}{C_{\text{REF}}} \right) = t_{\text{REF}} \left( 17.5 + \frac{1}{610} \frac{2500}{610} \right) = 21.6t_{\text{REF}}$
Optimal Driving of Capacitive Loads

Example: Design a pad driver for driving a load capacitance of 10pF, determine $t_{\text{PROP}}$ for the pad driver, and compare this with the propagation delay for driving the pad with a minimum-sized reference inverter.

In 0.5μm proc $t_{\text{REF}}=20\text{ps}, C_{\text{REF}}=4\text{fF}, R_{\text{PDREF}}=2.5\text{K}$

If driven directly with the minimum-sized reference inverter

$$t_{\text{PROP}} = t_{\text{REF}} \frac{C_L}{C_{\text{REF}}} = 2500 t_{\text{REF}}$$

Note an improvement in speed by a factor of

$$r = \frac{2500}{20} = 125$$
End of Lecture 39
Propagation delay for equal rise/fall gates was derived to be

\[ t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^{3} \frac{F_l(k+1)}{OD_k} \]

Delay calculations with “logical effort” approach

Author’s definition:

\[ t_{\text{PROP}} = \sum_{k=1}^{n} f_k \]

where \( f_k \) is the “effort delay” of stage \( k \)

\[ f_k = g_k h_k \]

\( g_k = \) logical effort

\( h_k = \) electrical effort
Propagation Delay in “Logic Effort” approach

\[ t_{\text{PROP}} = \sum_{k=1}^{n} f_k \]

\[ f_k = g_k h_k \]

\( f_k \) = “effort delay” of stage \( k \)

\( g_k \) = logical effort

\( h_k \) = electrical effort

Logic Effort is the ratio of the input capacitance of a gate to the input capacitance of an inverter that can deliver the same output current.

Electrical Effort is the ratio of the gate load capacitance to the input capacitance of a gate.

\[ \text{Gate} \]

\[ V_{\text{IN}} \] \rightarrow \[ \text{Gate} \] \rightarrow \[ V_{\text{OUT}} \]

\[ F_{\text{ILCREF}} \]
Propagation Delay in “Logic Effort” approach

\[ t_{\text{PROP}} = \sum_{k=1}^{n} f_k \quad f_k = g_k h_k \]

Logic Effort \((g)\) is the ratio of the input capacitance of a gate to the input capacitance of an inverter that can deliver the same output current.

Electrical Effort \((h)\) is the ratio of the gate load capacitance to the input capacitance of a gate.

\[ g_k = \frac{C_{\text{IN}k}}{C_{\text{REF}} \cdot \text{OD}_k} \quad h_k = \frac{C_{\text{REF}} \cdot F_i k + 1}{C_{\text{IN}k}} \]
Propagation Delay in “Logic Effort” approach

\[ t_{\text{PROP}} = \sum_{k=1}^{n} f_k \]

\[ f_k = g_k h_k \]

\[ g_k = \frac{C_{\text{IN}_k}}{C_{\text{REF}} \cdot \text{OD}_k} \]

\[ h_k = \frac{C_{\text{REF}} \cdot F_{l(k+1)}}{C_{\text{IN}_k}} \]

\[ f_k = \frac{F_{l(k+1)}}{\text{OD}_k} \]

\[ t_{\text{PROP}} = \sum_{k=1}^{n} f_k = \sum_{k=1}^{n} g_k h_k = \sum_{k=1}^{n} \frac{F_{l(k+1)}}{\text{OD}_k} \]
Propagation Delay in “Logic Effort” approach

\[ t_{\text{PROP}} = \sum_{k=1}^{n} f_k = \sum_{k=1}^{n} g_k h_k = \sum_{k=1}^{n} \frac{F_{l(k+1)}}{\text{OD}_k} \]

• Note with the exception of the \( t_{\text{REF}} \) that was omitted in the text, this expression is identical to what we have derived previously

  • Probably more tedious to use the “Logical Effort” approach

  • Extensions to asymmetric overdrive factors may not be trivial

  • Extensions to include parasitics may be tedious as well

  • Logical Effort is widely used throughout the industry
Elmore Delay Calculations

- Interconnects have a distributed resistance and a distributed capacitance
  - Often modeled as resistance/unit length and capacitance per unit length
- These delay the propagation of the signal
- Effectively a transmission line
  - Analysis is really complicated
- Can have much more complicated geometries
Elmore Delay Calculations

Can have much more complicated geometries
Elmore Delay Calculations

For $X_1 < X_2 < X_3$
Elmore Delay Calculations

A lumped element model of transmission line

Even this lumped model is 4-th order and a closed-form solution is very tedious!

Need a quick (and reasonably good) approximation to the delay of a delay line!!
Elmore Delay Calculations

Elmore delay: \[ t_{PD} = \sum_{i=1}^{n} \left( C_i \sum_{j=1}^{i} R_j \right) \]

- Numbering is critical (resistors and capacitors numbered from input to output)
- As stated, only applies to this specific structure
Elmore Delay Calculations

Elmore delay:

$$t_{PD} = \sum_{i=1}^{n} \left( C_i \sum_{j=1}^{i} R_j \right)$$

• Note error in text on Page 161

$$t_{pd} = \sum_{i} R_{n-i} C_i = \sum_{i=1}^{N} C_i \sum_{j=i}^{i} R_j$$
Elmore delay[1] is a simple approximation to the delay through an RC network in an electronic system. It is often used in applications such as logic synthesis, delay calculation, static timing analysis, placement and routing, since it is simple to compute (especially in tree structured networks, which are the vast majority of signal nets within ICs) and is reasonably accurate. Even where it is not accurate, it is usually faithful, in the sense that reducing the Elmore delay will almost always reduce the true delay, so it is still useful in optimization.

Elmore Delay Calculations

Example:

\[
\begin{align*}
\text{Elmore delay:} & \quad t_{PD} = \sum_{i=1}^{4} \left( C_i \sum_{j=1}^{i} R_j \right) \\
& \quad t_{PD} = \sum_{i=1}^{4} (t_i) \\
\text{where} & \quad t_i = C_i \sum_{j=1}^{i} R_j \\
& \quad j = 1, 2, 3, 4
\end{align*}
\]

What is really happening?

- Creating 4 first-order circuits
- Delay to \( V_1 \), \( V_2 \), \( V_3 \) and \( V_4 \) calculated separately by considering capacitors one at a time and assuming others are 0
Elmore Delay Calculations

Extensions:

Lumped Network Model:
Elmore Delay Calculations

Extensions:

1. Create a lumped element model

![Lumped Element Model Diagram]

2. Create a path from input to output

![Path from Input to Output Diagram]
Elmore Delay Calculations

Extensions:

3. Renumber elements along path from input to output and neglect off-path elements

4. Use Elmore Delay equation for elements on this RC network

\[ t_{PD} = \sum_{i=1}^{4} \left( C_i \sum_{j=1}^{i} R_j \right) \]
Elmore Delay Calculations

How is a resistive load handled?
Elmore Delay Calculations

Example with resistive load:

\[
\text{Elmore delay: } t_{PD} = \sum_{i=1}^{4} \left( C_i \sum_{j=1}^{i} R_j \right)
\]

where

\[
t_{PD} = \sum_{i=1}^{4} (t_i)
\]

\[
t_i = C_i \sum_{j=1}^{i} R_j \quad j = 1, 2, 3
\]

\[
t_4 = C_4 \left( \sum_{j=1}^{4} R_j \right) // R_5
\]
Elmore Delay Calculations

With resistive load:

\[
V_{IN} \quad R_1 \quad C_1 \quad R_2 \quad C_2 \quad R_3 \quad C_3 \quad \cdots \quad R_n \quad C_n \quad V_{OUT}
\]

Elmore delay:

\[
t_{PD} = \sum_{i=1}^{n-1} \left( C_i \sum_{j=1}^{i} R_j \right) + C_n \left( \sum_{j=1}^{n} R_j \right) / R_L
\]
Ring Oscillators
Device Sizing

Multiple Input Gates: