Digital Circuits

Multiple-input gates
Propagation Delay – basic characterization
Device Sizing
Review from Last Time

Transfer characteristics of the static CMOS inverter
(Neglect \( \lambda \) effects)
Review from Last Time

Transfer characteristics of the static CMOS inverter

(Neglect $\lambda$ effects)

From Case 3 analysis:

$$V_{\text{IN}} = \left( V_{\text{Tn}} \right) + \left( V_{\text{DD}} + V_{\text{Tp}} \right) \frac{\mu_p W_2 L_1}{\mu_n W_1 L_2} \sqrt{1 + \frac{\mu_p W_2 L_1}{\mu_n W_1 L_2}}$$
Inverter Transfer Characteristics of Inverter Pair

What are $V_H$ and $V_L$?

Find the points on the inverter pair transfer characteristics where $V_{OUT}'=V_{IN}$ and the slope is less than 1.
Inverter Transfer Characteristics of Inverter Pair for THIS Logic Family

Note this is independent of device sizing for THIS logic family !!
Sizing of the Basic CMOS Inverter

The characteristic that device sizes do not need to be used to establish $V_H$ and $V_L$ logic levels is a major advantage of this type of logic.

How should $M_1$ and $M_2$ be sized?

How many degrees of freedom are there in the design of the inverter?
How should $M_1$ and $M_2$ be sized?

How many degrees of freedom are there in the design of the inverter?

$$\{ W_1, W_2, L_1, L_2 \}$$

4 degrees of freedom

But in basic device model and in most performance metrics, $W_1/L_1$ and $W_2/L_2$ appear as ratios

$$\{ W_1/L_1, W_2/L_2 \}$$

effectively 2 degrees of freedom
How should $M_1$ and $M_2$ be sized?

{ $W_1, W_2, L_1, L_2$}  
4 degrees of freedom  
Usually pick $L_1 = L_2 = L_{\text{min}}$

{ $W_1/L_1, W_2/L_2$}  
effectively 2 degrees of freedom

How are $W_1$ and $W_2$ chosen?

Depends upon what performance parameters are most important for a given application!
How should $M_1$ and $M_2$ be sized?

One popular sizing strategy:

1. Pick $W_1 = W_{\text{MIN}}$ to minimize area of $M_1$
2. Pick $W_2$ to set trip-point at $V_{DD}/2$

Usually pick $L_1 = L_2 = L_{\text{min}}$

$\{ W_1/L_1, W_2/L_2 \}$ 2 remaining degrees of freedom
How should $M_1$ and $M_2$ be sized?

pick $L_1=L_2=L_{\text{min}}$

One popular sizing strategy:

1. Pick $W_1=W_{\text{MIN}}$ to minimize area of $M_1$
2. Pick $W_2$ to set trip-point at $V_{DD}/2$

Observe Case 3 provides expression for $V_{\text{TRIP}}$

Thus, at the trip point,

$$V_{\text{OUT}} = V_{\text{IN}} = V_{\text{TRIP}} = \frac{(V_{Tn}) + (V_{DD} + V_{Tp})}{1 + \sqrt{\frac{\mu_p W_2 L_1}{\mu_n W_1 L_2}}},$$
How should $M_1$ and $M_2$ be sized?

pick $L_1=L_2=L_{\text{min}}$

One popular sizing strategy:
1. Pick $W_1=W_{\text{MIN}}$ to minimize area of $M_1$
2. Pick $W_2$ to set trip-point at $V_{DD}/2$

Typically $V_{Tn}=0.2V_{DD}$, $|V_{Tp}|=0.2V_{DD}$

$$V_{\text{TRIP}} = \frac{(V_{Tn}) + (V_{DD} + V_{Tp}) \sqrt{\frac{\mu_p}{\mu_n}} \frac{W_2}{L_1}}{1 + \sqrt{\frac{\mu_p}{\mu_n}} \frac{W_2}{L_1}}$$

$$V_{DD} = \frac{0.2V_{DD}}{2} + \frac{(V_{DD} - 0.2V_{DD}) \sqrt{\frac{\mu_p}{\mu_n}} \frac{W_2}{L_1}}{1 + \sqrt{\frac{\mu_p}{\mu_n}} \frac{W_2}{L_1}}$$

Solving this equation for $W_2$, obtain

$$W_2 = W_1 \left( \frac{\mu_n}{\mu_p} \right)$$

Other sizing strategies are used as well and will be discussed later!
Extension of Basic CMOS Inverter to Multiple-Input Gates

Perform as a 2-input NOR Gate

Can be easily extended to an n-input NOR Gate
Extension of Basic CMOS Inverter to Multiple-Input Gates

Performs as a 2-input NAND Gate

Can be easily extended to an n-input NAND Gate
Static CMOS Logic Family

Observe PUN is p-channel, PDN is n-channel
Static CMOS Logic Family

n-channel PDN and p-channel PUN
General Logic Family

![Diagram of General Logic Family]

- PUN
- PDN

V\text{IN} \quad V\text{OUT}

- p-channel PUN
- n-channel PDN

Arbitrary PUN and PDN
Other CMOS Logic Families

- **Enhancement Load NMOS**
- **Enhancement Load Pseudo-NMOS**
- **Depletion Load NMOS**
Other CMOS Logic Families

- High and low swings are reduced
- Response time is slow on LH output transitions
- Static Power Dissipation Large when $V_{\text{OUT}}$ is low
- Very economical process
- Termed “ratio logic”
- Compact layout (no wells !)
Other CMOS Logic Families

- Multiple-input gates require single transistor for each additional input
- Still useful if many inputs are required (static power does not increase with k
Other CMOS Logic Families

- High and low swings are reduced
- Response time is slow on LH output transitions
- Static Power Dissipation Large when $V_{\text{OUT}}$ is low
- Termed “ratio” logic
Other CMOS Logic Families

- **Depletion Load NMOS**

- Circuit Diagram:
  - $V_{IN}$
  - $M_1$
  - $V_{OUT}$
  - $M_2$
  - $V_{DD}$

**Graph:**
- $V_{OUT}$ vs $V_{IN}$
- $V_{TD} < 0$

- **Benefits:**
  - Low swing is reduced
  - Static Power Dissipation Large when $V_{OUT}$ is low
  - Very economical process
  - Termed “ratio” logic
  - Compact layout (no wells!)
  - Dominant MOS logic until about 1985
  - Depletion device not available in most processes today

- **Symbolic Representation:**
  - $V_{TD} < 0$
  - Low swing is reduced
  - Static Power Dissipation Large when $V_{OUT}$ is low
  - Very economical process
  - Termed “ratio” logic
  - Compact layout (no wells!)
  - Dominant MOS logic until about 1985
  - Depletion device not available in most processes today
Other CMOS Logic Families

- Reduced $V_H-V_L$
- Device sizing critical for even basic operation
- Shallow slope at $V_{TRIP}$
Other CMOS Logic Families

Enhancement Load
Pseudo-NMOS

- Reduced $V_H - V_L$
- Device sizing critical for even basic operation
- Shallow slope at $V_{TRIP}$
Other CMOS Logic Families

- Reduced $V_{H}-V_{L}$
- Device sizing critical for even basic operation
- Shallow slope at $V_{TRIP}$
Other CMOS Logic Families

- Reduced $V_H - V_L$
- Device sizing critical for even basic operation
- Shallow slope at $V_{TRIP}$

Depletion Load NMOS

$V_{IN}$ $\rightarrow$ $M_1$ $\rightarrow$ $V_{OUT}$

$V_{DD}$ $\rightarrow$ $M_2$ $\rightarrow$ $V_{OUT}$

$V_{TD} < 0$

$V_{IN}$ $\rightarrow$ $V_{DD}$ $\rightarrow$ $M_2$ $\rightarrow$ $V_{OUT}$

$V_{OUT}$

$V_{DD}$

$V_{OUT}$ $\rightarrow$ $V_{DD}$

$V_{IN}$ $\rightarrow$ $V_{DD}$

$V_{DD}$ $\rightarrow$ $V_{IN}$

$V_{TP}$ $\rightarrow$ $V_{IN}$

$V_{DD}$ $\rightarrow$ $V_{TP}$

$V_{TN}$ $\rightarrow$ $V_{IN}$

$V_{DD}$ $\rightarrow$ $V_{TN}$
Static Power Dissipation in Static CMOS Family

When $V_{OUT}$ is Low, $I_{D1} = 0$

When $V_{OUT}$ is High, $I_{D2} = 0$

Thus, $P_{STATIC} = 0$

This is a key property of the static CMOS Logic Family and is the major reason Static CMOS Logic is so dominant

It can be shown that this zero static power dissipation property can be preserved if the PUN is comprised of n-channel devices, the PDN is comprised of n-channel devices and they are never both driven into the conducting states at the same time.
Static Power Dissipation in Ratio Logic Families

Example:
Assume \( V_{DD} = 5V \)
\( V_T = 1V \), \( \mu C_{OX} = 10^{-4} A/V^2 \), \( W_1/L_1 = 1 \) and \( M_2 \) sized so that \( V_L = V_{Th} \)

Observe:
\( V_H = V_{DD} - V_{Th} \)

If \( V_{IN} = V_H \), \( V_{OUT} = V_L \) so

\[
I_{D1} = \frac{\mu C_{OX} W_1}{L_1} \left( V_{GS1} - V_T - \frac{V_{DS1}}{2} \right) V_{DS1}
\]

\[
I_{D1} = 10^{-4} \left( 5 - 1 - 1 - \frac{1}{2} \right) \cdot 1 = 0.25mA
\]

\( P_L = (5V)(0.25mA) = 1.25mW \)
Static Power Dissipation in Ratio Logic Families

Example:

Assume $V_{DD}=5V$
$V_T=1V$, $\mu C_{OX}=10^{-4}A/V^2$, $W_1/L_1=1$ and $M_2$ sized so that $V_L=V_Tn$

$$P_L=(5V)(0.25mA)=1.25mW$$

If a circuit has 100,000 gates and half of them are in the $V_{OUT}=V_L$ state, the static power dissipation will be
Static Power Dissipation in Ratio Logic Families

Example:

Assume $V_{DD}=5V$

$V_T=1V$, $\mu C_{OX}=10^{-4}A/V^2$, $W_1/L_1=1$ and $M_2$ sized so that $V_L=V_{Tn}$

$$P_L=(5V)(0.25mA)=1.25mW$$

If a circuit has 100,000 gates and half of them are in the $V_{OUT}=V_L$ state, the static power dissipation will be

$$P_{STATIC} = \frac{1}{2} \cdot 10^5 \cdot 1.25mW = 62.5W$$

This power dissipation is way too high and would be even larger in circuits with 100 million or more gates – the level of integration common in SoC circuits today.
Propagation Delay in Static CMOS Family

Switch-level model of Static CMOS inverter (neglecting diffusion parasitics)
Propagation Delay in Static CMOS Family

Switch-level model of Static CMOS inverter (neglecting diffusion parasitics)
Propagation Delay in Static CMOS Family

Since operating in triode through most of transition:

\[
I_D \approx \frac{\mu C_{Ox} W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} \approx \frac{\mu C_{Ox} W}{L} (V_{GS} - V_T) V_{DS}
\]

\[
R_{PD} = \frac{L_1}{\mu_n C_{Ox} W_1 (V_{DD} - V_{Th})}
\]

\[
I_D = \frac{\mu C_{Ox} W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} \approx \frac{\mu C_{Ox} W}{L} (V_{GS} - V_T) V_{DS}
\]

\[
R_{PU} = \frac{L_2}{\mu_p C_{Ox} W_2 (V_{DD} + V_{Tp})}
\]

\[
C_{IN} = C_{Ox} \left( W_1 L_1 + W_2 L_2 \right)
\]
Propagation Delay in Static CMOS Family

If \( u_nC_{OX}=100\mu A V^{-2} \), \( C_{OX}=4 fF \mu^{-2} \), \( V_{Tn}=V_{DD}/5 \), \( V_{TP}=-V_{DD}/5 \), \( \mu_n/\mu_p=3 \), \( L_1=W_1=L_{MIN} \), \( L_2=W_2=L_{MIN} \), \( L_{MIN}=0.5\mu \) and \( V_{DD}=5V \)

\[
R_{PD} = \frac{1}{10^{-4} \cdot 0.8V_{DD}} = 2.5K\Omega \\
R_{PU} = \frac{1}{10^{-4} \cdot \frac{1}{3} \cdot 0.8V_{DD}} = 7.5K\Omega
\]

\( C_{IN} = 4 \cdot 10^{-15} \cdot 2L_{MN}^2 = 2fF \)

Example: Minimum-sized \( M_1 \) and \( M_2 \)

\[
R_{PD} = \frac{L_1}{\mu_nC_{OX}W_1(V_{DD} - V_{Tn})} \\
R_{PU} = \frac{L_2}{\mu_pC_{OX}W_2(V_{DD} + V_{TP})} \\
C_{IN} = C_{OX}(W_1L_1 + W_2L_2)
\]
In typical process with Minimum-sized $M_1$ and $M_2$:

- $R_{PD} \approx 2.5 \text{K}\Omega$
- $R_{PU} \approx 3R_{PD} = 7.5 \text{K}\Omega$
- $C_{IN} \approx 2fF$
Propagation Delay in Static CMOS Family

In typical process with Minimum-sized $M_1$ and $M_2$:

- $R_{PD} \approx 2.5\, \Omega$
- $R_{PU} \approx 3R_{PD} = 7.5\, \Omega$
- $C_{IN} \approx 2\, \text{fF}$

How long does it take for a signal to propagate from $x$ to $z$?
Propagation Delay in Static CMOS Family

Consider:

For HL output transition, $C_L$ charged to $V_{DD}$

Ideally:
For HL output transition, $C_L$ charged to $V_{DD}$

Actually:

What is the transition time $t_{HL}$?
Propagation Delay in Static CMOS Family
Propagation Delay in Static CMOS Family

For HL output transition, \( C_L \) charged to \( V_{DD} \)

\[
V_{IN} \rightarrow V_{OUT} \quad V_{DD} \quad C_L
\]

\[
V_{IN} \quad t=0
\]

\[
V_{DD} \quad e^{-t}V_{DD}
\]

\[
V_{OUT}(t) = F + (1 - F)e^{-t} = 0 + (V_{DD} - 0)e^{-\frac{t}{R_{PD}C_L}}
\]

\[
\frac{V_{DD}}{e} = V_{DD}e^{-\frac{t_1}{R_{PD}C_L}}
\]

\[
t_1 = R_{PD}C_L
\]

If \( V_{TRIP} \) is close to \( V_{DD}/2 \), \( t_{HL} \) is close to \( t_1 \)
Propagation Delay in Static CMOS Family

For HL output transition, $C_L$ charged to $V_{DD}$

$t_{LH} \approx t_2 = R_{PU}C_L$

Summary:

$t_{LH} \approx R_{PU}C_L$

$t_{HL} \approx R_{PD}C_L$
Propagation Delay in Static CMOS Family

In typical process with Minimum-sized $M_1$ and $M_2$:

- $t_{HL} \approx R_{PD}C_L \approx 2.5K \cdot 2fF = 5\text{ps}$
- $t_{LH} \approx R_{PU}C_L \approx 7.5K \cdot 2fF = 15\text{ps}$

Note: LH transition is much slower than HL transition
Propagation Delay in Static CMOS Family

Defn: The Propagation Delay of a gate is defined to be the sum of $t_{HL}$ and $t_{LH}$, that is, $t_{PROP} = t_{HL} + t_{LH}$

$$t_{PROP} = t_{HL} + t_{LH} \approx C_L (R_{PU} + R_{PD})$$

Propagation delay represents a fundamental limit on the speed a gate can be clocked.

For basic two-inverter cascade in static CMOS logic

In typical process with minimum-sized $M_1$ and $M_2$:

$$t_{PROP} = t_{HL} + t_{LH} \approx 20 p \text{ sec}$$
The propagation delay through $k$ levels of logic is approximately the sum of the individual delays in the same path.
Propagation Delay in Static CMOS Family

Example:

\[ t_{HL} = t_{HL4} + t_{LH3} + t_{HL2} + t_{LH1} \]

\[ t_{LH} = t_{LH4} + t_{HL3} + t_{LH2} + t_{HL1} \]

\[ t_{PROP} = t_{LH} + t_{HL} = (t_{LH4} + t_{HL3} + t_{LH2} + t_{HL1}) + (t_{HL4} + t_{LH3} + t_{HL2} + t_{LH1}) \]

\[ t_{PROP} = t_{LH} + t_{HL} = (t_{LH4} + t_{HL4}) + (t_{LH3} + t_{HL3}) + (t_{LH2} + t_{HL2}) + (t_{LH1} + t_{HL1}) \]

\[ t_{PROP} = t_{PROP4} + t_{PROP3} + t_{PROP2} + t_{PROP1} \]
Propagation Delay in Static CMOS Family

Propagation through $k$ levels of logic

\[ t_{HL} = t_{HLk} + t_{LH(k-1)} + t_{HL(k-2)} + \cdots + t_{XY1} \]

\[ t_{LH} = t_{LHk} + t_{HL(k-1)} + t_{LH(k-2)} + \cdots + t_{YX1} \]

where $x=H$ and $Y=L$ if $k$ odd and $X=L$ and $Y=h$ if $k$ even

\[ t_{PROP} = \sum_{i=1}^{k} t_{PROP_i} \]
Digital Circuit Design

- Hierarchical Design
- Basic Logic Gates
- Properties of Logic Families
- Characterization of CMOS
  Inverter
- Static CMOS Logic Gates
  - Ratio Logic
- Propagation Delay
  - Simple analytical models
  - Elmore Delay
- Sizing of Gates
- Propagation Delay with Multiple Levels of Logic
- Optimal driving of Large Capacitive Loads
- Power Dissipation in Logic Circuits
- Other Logic Styles
- Array Logic
- Ring Oscillators

done
partial
Device Sizing

Will consider the inverter first

Degrees of Freedom?

Strategies?
Device Sizing

Degrees of Freedom?

Strategies?
Device Sizing

- Since not ratio logic, $V_H$ and $V_L$ are independent of device sizes for this inverter
- With $L_1 = L_2 = L_{\text{min}}$, there are 2 degrees of freedom ($W_1$ and $W_2$)

Sizing Strategies

- Minimum Size
- Fixed $V_{\text{TRIP}}$
- Equal rise-fall times (equal worst-case rise and fall times)
- Minimum power dissipation
- Minimum time required to drive a given load
- Minimum input capacitance
Device Sizing

Assume $V_{tn}=0.2V_{DD}$, $V_{tp}=-0.2V_{DD}$, $\mu_n/\mu_p=3$, $L_1=L_2=L_{min}$

Sizing Strategy: minimum sized

$W_n=?$, $W_p$, $V_{trip}=?$, $t_{HL}=?$, $t_{ LH}=?$

$R_{PD} = \frac{L_1}{\mu_n C_{OX} W_1 (V_{DD} - V_{tn})}$

$R_{PU} = \frac{L_2}{\mu_p C_{OX} W_2 (V_{DD} + V_{tp})}$

$C_{IN} = C_{OX} (W_1 L_1 + W_2 L_2)$
Device Sizing

Assume $V_{Tn}=0.2V_{DD}$, $V_{Tp}=-0.2V_{DD}$, $\mu_n/\mu_p=3$, $L_1=L_2=L_{\text{min}}$

Sizing Strategy: minimum sized

$W_n=\,?\,W_p$, $V_{\text{trip}}=\,?\,t_{HL}=\,?\,t_{LH}=\,?$

$W_1=W_2=W_{\text{MIN}}$

also provides minimum input capacitance

t_{LH} \text{ is longer than } t_{HL}$

$t_{HL}=R_{\text{PD}}C_L$

$t_{LH}=3 \, R_{\text{PD}}C_L$

$$V_{\text{trip}} = \frac{(0.2V_{DD})+(V_{DD}-0.2V_{DD})\sqrt{\frac{1}{3}}}{1+\sqrt{\frac{1}{3}}} = .42V_{DD}$$
Device Sizing

Assume $V_{Tn} = 0.2V_{DD}$, $V_{Tp} = -0.2V_{DD}$, $\mu_n/\mu_p = 3$, $L_1 = L_2 = L_{min}$

Sizing strategy: Equal rise and fall times

$W_n = \square, W_p, V_{trip} = \square, t_{HL} = \square, t_{LH} = \square$

$$R_{PD} = \frac{L_{min}}{\mu_n C_{OX} W_1 (0.8V_{DD})}$$

$$R_{PU} = \frac{L_{min}}{3\mu_n C_{OX} W_2 (0.8V_{DD})}$$
Device Sizing

Assume $V_{Tn}=0.2V_{DD}$, $V_{Tp}=-0.2V_{DD}$, $\mu_n/\mu_p=3$, $L_1=L_2=L_{min}$

Sizing strategy: Equal rise and fall times

- \[
\frac{t_{LH}}{t_{HL}} = \frac{R_{PU}C_{IN}}{R_{PD}C_{IN}} \Rightarrow R_{PU}=R_{PD}
\]

Thus \[
\frac{L_1}{u_nC_{OX}W_1(V_{DD}-V_{Tn})} = \frac{L_2}{u_pC_{OX}W_2(V_{DD}+V_{Tp})}
\]

with $L_1=L_2$ and $V_{Tp}=-V_{Tn}$ we must have \[\frac{W_2}{W_1} = \frac{\mu_n}{\mu_p}\]

What about the second degree of freedom?

$V_{TRIP}=$?
Device Sizing

Assume $V_{Tn}=0.2V_{DD}$, $V_{Tp}=-0.2V_{DD}$, $\mu_n/\mu_p=3$, $L_1=L_2=L_{\text{min}}$

Sizing strategy: Equal (worst-case) rise and fall times

$W_n=?$, $W_p$, $V_{\text{trip}}=?$, $t_{HL}=?$, $t_{LH}=?$

\[
\frac{W_2}{W_1} = \frac{\mu_n}{\mu_p}
\]

\[
V_{\text{trip}} = \frac{(V_{Tn}) + (V_{DD} + V_{Tp})}{\sqrt{\frac{\mu_p W_2 L_1}{\mu_n W_1 L_2}}} = \frac{0.2V_{DD} + 0.8V_{DD}}{2} = \frac{V_{DD}}{2}
\]

$t_{HL} = t_{LH} = R_{pd}C_L = \frac{L_{\text{min}}}{\mu_n C_{OX} W_{\text{min}} (0.8V_{DD})} C_L$
Device Sizing

Assume $V_{Tn}=0.2V_{DD}$, $V_{Tp}=-0.2V_{DD}$, $\mu_n/\mu_p=3$, $L_1=L_2=L_{\text{min}}$

Sizing strategy: Fixed $V_{\text{TRIP}}=V_{DD}/2$

$W_n=\?$, $W_p$, $V_{\text{trip}}=\?$, $t_{HL}=\?$, $t_{LH}=\?$
Device Sizing

Assume \( V_{Tn} = 0.2V_{DD} \), \( V_{Tp} = -0.2V_{DD} \), \( \mu_n/\mu_p = 3 \), \( L_1 = L_2 = L_{min} \)

Sizing strategy: Fixed \( V_{TRIP} = V_{DD}/2 \)

\( W_n = ?, W_p, V_{trip} = ?, t_{HL} = ?, t_{LH} = ? \)

Set

\[
V_{TRIP} = \frac{V_{DD}}{2}
\]

\[
V_{TRIP} = \frac{0.2V_{DD} + (V_{DD} - 0.2V_{DD}) \sqrt{\frac{\mu_p W_2 L_1}{\mu_n W_1 L_2}}}{1 + \sqrt{\frac{\mu_p W_2 L_1}{\mu_n W_1 L_2}}} = \frac{V_{DD}}{2}
\]

Solving, obtain

\[
\frac{W_2}{W_1} = \frac{\mu_n}{\mu_p}
\]

Observe this is the same sizing as was obtained for equal worst-case rise and fall times so \( t_{HL} = t_{LH} = R_{pd} C_L \)

This is no coincidence and these properties guide the definition of the process parameters provided by the foundry.
Device Sizing

Assume $V_{Tn}=0.2V_{DD}$, $V_{Tp}=-0.2V_{DD}$, $\mu_n/\mu_p=3$, $L_1=L_2=L_{min}$

Sizing Strategies

- Minimum Size
- Fixed $V_{TRIP}$
- Equal rise-fall times (equal worst-case rise and fall times)
- Minimum power dissipation
- Minimum time required to drive a given load
- Minimum input capacitance
Device Sizing

Assume $V_{Tn}=0.2V_{DD}$, $V_{Tp}=-0.2V_{DD}$, $\mu_n/\mu_p=3$, $L_1=L_2=L_{min}$

**Sizing Strategy Summary**

<table>
<thead>
<tr>
<th></th>
<th>Minimum Size</th>
<th>$V_{TRIP}=V_{DD}/2$</th>
<th>Equal Rise/Fall</th>
</tr>
</thead>
<tbody>
<tr>
<td>Size</td>
<td>$W_n=W_p=W_{min}$</td>
<td>$W_n=W_{min}$</td>
<td>$W_n=W_{min}$</td>
</tr>
<tr>
<td></td>
<td>$L_p=L_n=L_{min}$</td>
<td>$W_p=3W_{min}$</td>
<td>$W_p=3W_{min}$</td>
</tr>
<tr>
<td>$t_{HL}$</td>
<td>$R_{pd}C_L$</td>
<td>$R_{pd}C_L$</td>
<td>$R_{pd}C_L$</td>
</tr>
<tr>
<td>$t_{LH}$</td>
<td>$3R_{pd}C_L$</td>
<td>$R_{pd}C_L$</td>
<td>$R_{pd}C_L$</td>
</tr>
<tr>
<td>$t_{PROP}$</td>
<td>$4R_{pd}C_L$</td>
<td>$2R_{pd}C_L$</td>
<td>$2R_{pd}C_L$</td>
</tr>
<tr>
<td>$V_{trip}$</td>
<td>$V_{TRIP}=0.42V_{DD}$</td>
<td>$V_{TRIP}=0.5V_{DD}$</td>
<td>$V_{TRIP}=0.5V_{DD}$</td>
</tr>
</tbody>
</table>

- For a fixed load $C_L$, the minimum-sized structure has a higher $t_{PROP}$ but if the load is another inverter, $C_L$ will also increase so the speed improvements become less apparent
- This will be investigated later
The reference inverter

Assume \( \mu_n/\mu_p = 3 \)

\( L_n = L_p = L_{MIN} \)

\( W_n = W_{MIN}, \quad W_p = 3W_n \)

\[
C_{REF} = C_{INREF} = 4C_{OX}W_{MIN}L_{MIN}
\]

\[
R_{PDREF} = \frac{L_{MIN}}{\mu_n C_{OX} W_{MIN} (V_{DD} - V_{Tn})} \quad V_{Tn} = \frac{2V_{DD}}{} \quad = \frac{L_{MIN}}{\mu_n C_{OX} W_{MIN} (0.8V_{DD})}
\]

- Have sized the reference inverter with \( W_p/W_n = \mu_n/\mu_p \)
- In standard processes, provides \( V_{TRIP} \approx V_{DD}/2 \) and \( t_{HL} \approx t_{LH} \)
- Any other sizing strategy could have been used for the reference inverter but this is most convenient
Reference Inverter

The reference inverter pair

Assume \( \mu_n/\mu_p = 3 \)

\( L_n = L_p = L_{\text{MIN}} \)

\( W_n = W_{\text{MIN}}, \quad W_p = 3W_n \)

\[ C_{L1} = C_{\text{REF}} = 4C_{OX} W_{\text{MIN}} L_{\text{MIN}} \]

\[ t_{\text{REF}} = \begin{cases} \text{def} & \quad t_{\text{PROPREF}} = t_{\text{HLREF}} + t_{\text{LHREF}} = 2R_{PDREF} C_{\text{REF}} \end{cases} \]
Reference Inverter

The reference inverter pair

Assume $\mu_n/\mu_p = 3$

$L_n = L_p = L_{\text{MIN}}$

$W_n = W_{\text{MIN}}, W_p = 3W_n$

Summary: parameters defined from reference inverter:

$C_{\text{REF}} = 4C_{\text{OX}} W_{\text{MIN}} L_{\text{MIN}}$

$R_{\text{PDREF}} = \frac{\mu_n C_{\text{OX}} W_{\text{MIN}} (V_{\text{DD}} - V_{T_n})}{L_{\text{MIN}}}$

$t_{\text{REF}} = 2R_{\text{PDREF}} C_{\text{REF}}$

$C_{\text{REF}} = 4C_{\text{OX}} W_{\text{MIN}} L_{\text{MIN}}$
The Reference Inverter

C_{\text{REF}} = C_{\text{IN}} = 4C_{\text{OX}} W_{\text{MIN}} L_{\text{MIN}}

R_{\text{PDREF}} = \frac{L_{\text{MIN}}}{\mu_n C_{\text{OX}} W_{\text{MIN}} (V_{\text{DD}} - V_{Tn})}

V_{Tn} = \frac{L_{\text{MIN}}}{\mu_n C_{\text{OX}} W_{\text{MIN}} (0.8V_{\text{DD}})}

t_{\text{HLREF}} = t_{\text{LHREF}} = R_{\text{PDREF}} C_{\text{REF}}

V_{\text{IN}} \rightarrow V_{\text{OUT}}

W_n = W_{\text{MIN}}, \quad W_p = 3W_{\text{MIN}}

L_n = L_p = L_{\text{MIN}}

Assume \frac{\mu_n}{\mu_p} = 3

\text{In 0.5u proc } t_{\text{REF}} = 20\, \text{ps},

C_{\text{REF}} = 4fF, R_{\text{PDREF}} = 2.5K
How does the propagation delay compare for a minimum-sized strategy to that of an equal rise/fall sizing strategy?

Minimum Sized
\[
W_2 = W_1 = W_{\text{MIN}}
\]

Reference Inverter
\[
W_2 = (\mu_n/\mu_p)W_1, \quad W_1 = W_{\text{MIN}}
\]
\[
t_{\text{PROP}} = t_{\text{REF}}
\]
Device Sizing

The minimum-sized inverter pair

\[ C_{\text{REF}} = 4C_{\text{OX}} W_{\text{MIN}} L_{\text{MIN}} \]

\[ C_{L1} = 2C_{\text{OX}} W_{\text{MIN}} L_{\text{MIN}} = 0.5C_{\text{REF}} \]

\[ R_{\text{PDn}} = \frac{L_{\text{MIN}}}{\mu_n C_{\text{OX}} W_{\text{MIN}} (V_{\text{DD}} - V_{\text{Tn}})} = R_{\text{PDREF}} \]

\[ R_{\text{PUp}} = \frac{L_{\text{MIN}}}{\mu_p C_{\text{OX}} W_{\text{MIN}} (V_{\text{DD}} + V_{\text{Tp}})} = 3R_{\text{PDREF}} \]

\[ t_{\text{PROP}} = t_{\text{HLREF}} + t_{\text{LHREF}} = R_{\text{PDREF}} (0.5C_{\text{REF}}) + 3R_{\text{PDREF}} (0.5C_{\text{REF}}) = 2R_{\text{PDREF}} C_{\text{REF}} \]

thus \[ t_{\text{PROP}} = t_{\text{REFF}} \]
Device Sizing

The minimum-sized inverter pair

Assume $\mu_n/\mu_p=3$

$L_n=L_p=L_{MIN}$

$W_n=W_{MIN}$, $W_p=W_n$

$C_{REF} = 4C_{OX}W_{MIN}L_{MIN}$

$C_{L1} = 0.5C_{REF} = 2C_{OX}W_{MIN}L_{MIN}$

$R_{PDREF} = \frac{L_{MIN}}{\mu_n C_{OX} W_{MIN} (V_{DD} - V_{Tn})}$

$v_{Tn} = 2V_{DD}$

$= \frac{L_{MIN}}{\mu_n C_{OX} W_{MIN} (0.8V_{DD})}$

$t_{PROP} = t_{HLREF} + t_{LHREF} = R_{PDREF}(0.5C_{REF}) + 3R_{PDREF}(0.5C_{REF}) = 2R_{PDREF}C_{REF}$

$t_{PROP} = t_{REFF}$
By how much did $t_{lh}$ improve?

Why was there no net change in $t_{PROP}$?

How does the propagation delay compare for a minimum-sized strategy to that of an equal rise/fall sizing strategy?

Even though the $t_{lh}$ rise time has been reduced with the equal rise/fall sizing strategy, this was done at the expense of an increase in the total load capacitance that resulted in no net change in propagation delay!

They are the same!
End of Lecture 39