Digital Circuits

Propagation Delay – basic characterization
Device Sizing (Inverter and multiple-input gates)
Other MOS Logic Families

Review from last lecture

Enhancement Load NMOS

Enhancement Load Pseudo-NMOS

Depletion Load NMOS
When $V_{OUT}$ is Low, $I_{D1}=0$

When $V_{OUT}$ is High, $I_{D2}=0$

Thus, $P_{STATIC}=0$

This is a key property of the static CMOS Logic Family and is the major reason Static CMOS Logic is so dominant.

It can be shown that this zero static power dissipation property can be preserved if the PUN is comprised of p-channel devices, the PDN is comprised of n-channel devices and they are never both driven into the conducting states at the same time.
Defn: The Propagation Delay of a gate is defined to be the sum of \( t_{HL} \) and \( t_{LH} \), that is, \( t_{PROP} = t_{HL} + t_{LH} \)

\[
t_{PROP} = t_{HL} + t_{LH} \approx C_L (R_{PU} + R_{PD})
\]

Propagation delay represents a fundamental limit on the speed a gate can be clocked

For basic two-inverter cascade in static CMOS logic

\[
t_{PROP} = t_{HL} + t_{LH} \approx 20 \mu \text{sec}
\]

In typical process with minimum-sized \( M_1 \) and \( M_2 \):
Propagation Delay in Static CMOS Family

Propagation through k levels of logic

\[ t_{HL} \approx t_{HLk} + t_{LH(k-1)} + t_{HL(k-2)} + \cdots + t_{XY1} \]

\[ t_{LH} \approx t_{LHk} + t_{HL(k-1)} + t_{LH(k-2)} + \cdots + t_{YX1} \]

where \( x=H \) and \( Y=L \) if \( k \) odd and \( X=L \) and \( Y=h \) if \( k \) even

\[ t_{PROP} = \sum_{i=1}^{k} t_{PROP}^k \]

Will return to propagation delay after we discuss device sizing
Digital Circuit Design

- Hierarchical Design
- Basic Logic Gates
- Properties of Logic Families
- Characterization of CMOS Inverter
- Static CMOS Logic Gates
  - Ratio Logic
- Propagation Delay
  - Simple analytical models
  - Elmore Delay
- Sizing of Gates

- Propagation Delay with Multiple Levels of Logic
- Optimal driving of Large Capacitive Loads
- Power Dissipation in Logic Circuits
- Other Logic Styles
- Array Logic
- Ring Oscillators
Question:

Why is $|V_{Tp}| \approx V_{Tn} \approx V_{DD}/5$ in many processes?
Device Sizing

Will consider the inverter first
Device Sizing

Degrees of Freedom?

Strategies?
Device Sizing

- Since not ratio logic, $V_H$ and $V_L$ are independent of device sizes for this inverter
- With $L_1=L_2=L_{\text{min}}$, there are 2 degrees of freedom ($W_1$ and $W_2$)

Sizing Strategies

- Minimum Size
- Fixed $V_{TRIP}$
- Equal rise-fall times (equal worst-case rise and fall times)
- Minimum power dissipation
- Minimum time required to drive a given load
- Minimum input capacitance
Device Sizing

Assume \( V_{Tn}=0.2V_{DD}, \ V_{Tp}=-0.2V_{DD}, \ \mu_n/\mu_p=3, \ L_1=L_2=L_{min} \)

Sizing Strategy: minimum sized

\( W_n=?, \ W_p=?, \ V_{\text{trip}}=?, \ t_{HL}=? , t_{LH}=? \)

\[
R_{PD} = \frac{L_1}{\mu_n C_{OX} W_1 (V_{DD} - V_{Tn})}
\]

\[
R_{PU} = \frac{L_2}{\mu_p C_{OX} W_2 (V_{DD} + V_{Tp})}
\]

\[
C_{IN} = C_{OX} (W_1 L_1 + W_2 L_2)
\]
Device Sizing

Assume \( V_{Tn} = 0.2V_{DD} \), \( V_{Tp} = -0.2V_{DD} \), \( \mu_n/\mu_p = 3 \), \( L_1 = L_2 = L_{\text{min}} \)

Sizing Strategy: minimum sized

\[ W_n = ?, \ W_p = ?, \ V_{\text{trip}} = ?, \ t_{HL} = ?, \ t_{LH} = ? \]

\[ W_1 = W_2 = W_{\text{MIN}} \]

also provides minimum input capacitance

\[ t_{HL} = R_{PD} C_L \]
\[ t_{LH} = 3 R_{PD} C_L \]

\( t_{LH} \) is longer than \( t_{HL} \)

\[ t_{\text{PROP}} = 4R_{PD} C_L \]

\[ V_{\text{TRIP}} = \frac{(0.2V_{DD}) + (V_{DD} - 0.2V_{DD})}{1 + \sqrt{\frac{1}{3}}} = .42V_{DD} \]
Device Sizing

Assume $V_{Tn}=0.2V_{DD}$, $V_{Tp}=-0.2V_{DD}$, $\mu_n/\mu_p=3$, $L_1=L_2=L_{\min}$

Sizing strategy: Equal (worst case) rise and fall times

$W_n=\?$, $W_p=\?$, $V_{trip}=\?$, $t_{HL}=\?$, $t_{LH}=\?$

$$R_{PD} = \frac{L_{\min}}{\mu_n C_{OX} W_1 (0.8V_{DD})}$$

$$R_{PU} = \frac{L_{\min}}{3\mu_n C_{OX} W_2 (0.8V_{DD})}$$
Device Sizing

Assume \( V_{Tn}=0.2V_{DD}, \ V_{Tp}=-0.2V_{DD}, \ \mu_n/\mu_p=3, \ L_1=L_2=L_{\text{min}} \)

**Sizing strategy:** Equal (worst case) rise and fall times

\[
\frac{t_{LH}}{t_{HL}} = \frac{R_{PU}C_{IN}}{R_{PD}C_{IN}} \Rightarrow R_{PU}=R_{PD}
\]

Thus

\[
\frac{L_1}{u_nC_{OX}W_1(V_{DD}-V_{Tn})} = \frac{L_2}{u_pC_{OX}W_2(V_{DD}+V_{Tp})}
\]

with \( L_1=L_2 \) and \( V_{Tp}=-V_{Tn} \) we must have

\[
\frac{W_2}{W_1} = \frac{\mu_n}{\mu_p} \approx 3
\]

What about the second degree of freedom?

\( W_1=W_{\text{MIN}} \)

\( V_{TRIP}=? \)
Device Sizing

Assume $V_{Tn}=0.2V_{DD}$, $V_{Tp}=-0.2V_{DD}$, $\mu_n/\mu_p=3$, $L_1=L_2=L_{\text{min}}$

Sizing strategy: Equal (worst-case) rise and fall times

$W_n=W_{\text{MIN}}, W_p=3W_{\text{MIN}}, V_{\text{trip}}=?, t_{HL}=?, t_{LH}=?$

$$V_{\text{TRIP}} = \frac{(V_{Tn}) + (V_{DD} + V_{Tp}) \sqrt{\frac{\mu_p W_2 L_1}{\mu_n W_1 L_2}}}{1 + \sqrt{\frac{\mu_p W_2 L_1}{\mu_n W_1 L_2}}} = \frac{0.2V_{DD} + 0.8V_{DD}}{2} = \frac{V_{DD}}{2}$$

$$t_{HL} = t_{LH} = R_{pd} C_L = \frac{L_{\text{min}}}{\mu_n C_{OX} W_{\text{min}} (0.8V_{DD})} C_L$$

$$t_{\text{PROP}} = 2 R_{pd} C_L$$

For a fixed $C_L$, how does $t_{\text{PROP}}$ compare for the minimum-sizing compared to equal rise/fall sizing?
Device Sizing

Assume $V_{Tn}=0.2V_{DD}$, $V_{Tp}=-0.2V_{DD}$, $\mu_n/\mu_p=3$, $L_1=L_2=L_{\text{min}}$

Sizing strategy: Fixed $V_{\text{TRIP}}=V_{DD}/2$

$W_n=?$, $W_p=?$, $V_{\text{trip}}=?$, $t_{HL}=?$, $t_{LH}=?$
Device Sizing

Assume $V_{Tn}=0.2V_{DD}$, $V_{Tp}=-0.2V_{DD}$, $\mu_n/\mu_p=3$, $L_1=L_2=L_{min}$

Sizing strategy: Fixed $V_{TRIP}=V_{DD}/2$

$W_n=?$, $W_p=?$, $V_{trip}=?$, $t_{HL}=?$, $t_{LH}=?$

Set

$V_{TRIP}=V_{DD}/2$

$$V_{TRIP} = \frac{0.2V_{dd} + (V_{DD} - 0.2V_{DD}) \sqrt{\frac{\mu_p W_2 L_1}{\mu_n W_1 L_2}}}{1 + \sqrt{\frac{\mu_p W_2 L_1}{\mu_n W_1 L_2}}} = \frac{V_{DD}}{2}$$

Solving, obtain

$$\frac{W_2}{W_1} = \frac{\mu_n}{\mu_p}$$

$W_n=W_{MIN}$, $W_p=3W_{MIN}$

- This is the same sizing as was obtained for equal worst-case rise and fall times so $t_{HL}=t_{LH}=R_{pd}C_L$
- This is no coincidence !!! Why?
- These properties guide the definition of the process parameters provided by the foundry
Device Sizing

Assume $V_{Tn} = 0.2V_{DD}$, $V_{Tp} = -0.2V_{DD}$, $\mu_n/\mu_p = 3$, $L_1 = L_2 = L_{\text{min}}$

Sizing Strategies

- Minimum Size
- Fixed $V_{\text{TRIP}}$
- Equal rise-fall times
  (equal worst-case rise and fall times)
- Minimum power dissipation
- Minimum time required to drive a given load
- Minimum input capacitance
Device Sizing

Assume \( V_{Tn} = 0.2V_{DD} \), \( V_{Tp} = -0.2V_{DD} \), \( \mu_n/\mu_p = 3 \), \( L_1 = L_2 = L_{\text{min}} \)

### Sizing Strategy Summary

<table>
<thead>
<tr>
<th>Size</th>
<th>Minimum Size</th>
<th>( V_{TRIP} = V_{DD}/2 )</th>
<th>Equal Rise/Fall</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>( W_n = W_p = W_{\text{min}} )</td>
<td>( W_n = W_{\text{min}} )</td>
<td>( W_n = W_{\text{min}} )</td>
</tr>
<tr>
<td></td>
<td>( L_p = L_n = L_{\text{min}} )</td>
<td>( W_p = 3W_{\text{min}} )</td>
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</tr>
<tr>
<td>( t_{HL} )</td>
<td>( R_{\text{pd}}C_L )</td>
<td>( R_{\text{pd}}C_L )</td>
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</tr>
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<td>( R_{\text{pd}}C_L )</td>
</tr>
<tr>
<td>( t_{PROP} )</td>
<td>( 4R_{\text{pd}}C_L )</td>
<td>( 2R_{\text{pd}}C_L )</td>
<td>( 2R_{\text{pd}}C_L )</td>
</tr>
<tr>
<td>( V_{\text{trip}} )</td>
<td>( V_{TRIP} = 0.42V_{DD} )</td>
<td>( V_{TRIP} = 0.5V_{DD} )</td>
<td>( V_{TRIP} = 0.5V_{DD} )</td>
</tr>
</tbody>
</table>

- For a fixed load \( C_L \), the minimum-sized structure has a higher \( t_{PROP} \) but if the load is another inverter, \( C_L \) will also change so the speed improvements become less apparent.
- This will be investigated later.
**Reference Inverter**

The reference inverter

Assume \( \mu_n/\mu_p = 3 \)

\( L_n = L_p = L_{\text{MIN}} \)

\( W_n = W_{\text{MIN}}, \quad W_p = 3W_n \)

\[ C_{\text{REF}} \quad \text{def} \quad C_{\text{INREF}} = 4C_{\text{OX}} W_{\text{MIN}} L_{\text{MIN}} \]

\[ R_{\text{PDREF}} = \frac{L_{\text{MIN}}}{\mu_n C_{\text{OX}} W_{\text{MIN}} (V_{\text{DD}} - V_{Tn})} = \frac{L_{\text{MIN}}}{\mu_n C_{\text{OX}} W_{\text{MIN}} (0.8V_{\text{DD}})} \]

\[ R_{\text{PUREF}} = \frac{L_{\text{MIN}}}{\mu_p C_{\text{OX}} 3W_{\text{MIN}} (V_{\text{DD}} + V_{Tp})} = R_{\text{PDREF}} \]

- Have sized the reference inverter with \( W_p/W_n = \mu_n/\mu_p \)
- In standard processes, provides \( V_{\text{TRIP}} \approx V_{\text{DD}}/2 \) and \( t_{\text{HL}} \approx t_{\text{LH}} \)
- Any other sizing strategy could have been used for the reference inverter but this is most convenient
Reference Inverter

The reference inverter pair

Assume $\mu_n/\mu_p=3$

$L_n = L_p = L_{MIN}$

$W_n = W_{MIN}$, $W_p = 3W_n$

$C_{L1} = C_{REF} = 4C_{OX} W_{MIN} L_{MIN}$

$t_{REF} = t_{PROPREF} = t_{HLREF} + t_{LHREF} = 2R_{PDREF} C_{REF}$
Reference Inverter

The reference inverter pair

Assume $\frac{\mu_n}{\mu_p} = 3$

$L_n = L_p = L_{\text{MIN}}$

$W_n = W_{\text{MIN}}, \quad W_p = 3W_n$

Summary: parameters defined from reference inverter:

$C_{\text{REF}} = 4C_{\text{OX}} W_{\text{MIN}} L_{\text{MIN}}$

$R_{\text{PDREF}} = \frac{L_{\text{MIN}}}{\mu_n C_{\text{OX}} W_{\text{MIN}} (V_{\text{DD}} - V_{Tn})}$

$t_{\text{REF}} = 2R_{\text{PDREF}} C_{\text{REF}}$

$C_{\text{REF}} = 4C_{\text{OX}} W_{\text{MIN}} L_{\text{MIN}}$
The Reference Inverter

Reference Inverter

Reference Inverter

\[ R_{PDREF} = R_{PUREF} \]

\[ C_{REF} = C_{IN} = 4C_{OX} W_{MIN} L_{MIN} \]

\[ R_{PDREF} = \frac{L_{MIN}}{\mu_n C_{OX} W_{MIN} (V_{DD} - V_{Tn})} = \frac{L_{MIN}}{\mu_n C_{OX} W_{MIN} (0.8V_{DD})} \]

\[ t_{HLREF} = t_{LHREF} = R_{PDREF} C_{REF} \]

\[ t_{REF} = t_{HLREF} + t_{LHREF} = 2R_{PDREF} C_{REF} \]

Assume \( \mu_n/\mu_p = 3 \)

\( W_n = W_{MIN}, \quad W_p = 3W_{MIN} \)

\( L_n = L_p = L_{MIN} \)

In 0.5u proc, \( t_{REF} = 20ps, \quad C_{REF} = 4fF, \quad R_{PDREF} = R_{PUREF} = 2.5K \)

(Note: This \( C_{OX} \) is somewhat larger than that in the 0.5u ON process)
How does the propagation delay compare for a minimum-sized strategy to that of an equal rise/fall sizing strategy?

**Minimum Sized**

\[ W_2 = W_1 = W_{\text{MIN}} \]

**Reference Inverter**

\[ W_2 = (\mu_n/\mu_p)W_1, \quad W_1 = W_{\text{MIN}} \]

\[ t_{\text{PROP}} = t_{\text{REF}} \]
Device Sizing

The minimum-sized inverter pair

Assume $\mu_n/\mu_p = 3$

$L_n = L_p = L_{\text{MIN}}$

$W_n = W_{\text{MIN}}, W_p = W_n$

$C_{\text{REF}} = 4C_{\text{OX}} W_{\text{MIN}} L_{\text{MIN}}$

$C_{L1} = 0.5C_{\text{REF}} = 2C_{\text{OX}} W_{\text{MIN}} L_{\text{MIN}}$

$R_{\text{PDREF}} = \frac{L_{\text{MIN}}}{\mu_n C_{\text{OX}} W_{\text{MIN}} (V_{\text{DD}} - V_{Tn})}$

$v_{Tn} = 2V_{\text{DD}}$

$= \frac{L_{\text{MIN}}}{\mu_n C_{\text{OX}} W_{\text{MIN}} (0.8V_{\text{DD}})}$

$t_{\text{PROP}} = t_{\text{HLREF}} + t_{\text{LHREF}} = R_{\text{PDREF}} (0.5C_{\text{REF}}) + 3R_{\text{PDREF}} (0.5C_{\text{REF}}) = 2R_{\text{PDREF}} C_{\text{REF}}$

$t_{\text{PROP}} = t_{\text{REFF}}$
Propagation Delay

How does the propagation delay compare for a minimum-sized strategy to that of an equal rise/fall sizing strategy?

Minimum Sized

\[ W_2 = W_1 = W_{MIN} \]

\[ t_{PROP} = t_{REF} \]

Reference Inverter

\[ W_2 = (\mu_n/\mu_p)W_1, \quad W_1 = W_{MIN} \]

\[ t_{PROP} = t_{REF} \]

They are the same!

Even though the \( t_{LH} \) rise time has been reduced with the equal rise/fall sizing strategy, this was done at the expense of an increase in the total load capacitance that resulted in no net change in propagation delay!
Will consider now the multiple-input gates

Will consider both minimum sizing and equal worst-case rise/fall

Will initially size so gate drive capability is same as that of ref inverter

Note: worst-case has been added since fall time in NOR gates or rise time in NAND gates depends upon how many transistors are conducting
Fan In

- The Fan In (FI) to an input of a gate device, circuit or interconnect that is capacitive is the input capacitance.
- Often this is normalized to some capacitance (typically $C_{REF}$ of ref inverter).

$$FI = C_{IN} \text{ alternately } FI = \frac{C_{IN}}{C_{REF}}$$
Sizing of Multiple-Input Gates

Analysis strategy: Express delays in terms of those of reference inverter

Reference Inverter

\[ \text{Assume } \mu_n / \mu_p = 3 \]

\[ W_n = W_{\text{MIN}}, \quad W_p = 3W_{\text{MIN}} \]

\[ L_n = L_p = L_{\text{MIN}} \]

In 0.5u proc, \( t_{\text{REF}} = 20 \text{ps}, \quad C_{\text{REF}} = 4 \text{fF}, \quad R_{\text{PDREF}} = 2.5 \text{K} \]

\[ C_{\text{IN}} = C_{\text{REF}} = 4C_{\text{OX}} W_{\text{MIN}} L_{\text{MIN}} \]

\[ F_{I_{\text{REF}}} = C_{\text{REF}} \quad \text{alternately} \quad F_{I_{\text{REF}}} = \frac{C_{\text{IN}}}{C_{\text{REF}}} = 1 \]

\[ R_{\text{PDREF}} = R_{\text{PURREF}} = \frac{L_{\text{MIN}}}{\mu_n C_{\text{OX}} W_{\text{MIN}} (0.8 V_{\text{DD}})} \]

\[ t_{\text{HLREF}} = t_{\text{LHREF}} = R_{\text{PDREF}} C_{\text{REF}} \]

\[ t_{\text{REF}} = t_{\text{HLREF}} + t_{\text{LHREF}} = 2R_{\text{PDREF}} C_{\text{REF}} \]
Device Sizing

Multiple Input Gates:

2-input NOR  2-input NAND  k-input NOR  k-input NAND

Equal Worst Case Rise/Fall (and equal to that of ref inverter when driving $C_{REF}$)

$W_n = ?$
$W_p = ?$

Fastest response ($t_{HL}$ or $t_{LH}$) = ?
Worst case response ($t_{PROP}$, usually of most interest)?

Input capacitance ($F_I$) = ?

Minimum Sized (assume driving a load of $C_{REF}$)

$W_n = W_{min}$
$W_p = W_{min}$

Fastest response ($t_{HL}$ or $t_{LH}$) = ?
Slowest response ($t_{HL}$ or $t_{LH}$) = ?
Worst case response ($t_{PROP}$, usually of most interest)?
Input capacitance ($F_I$) = ?
Device Sizing

Equal Worst Case Rise/Fall (and equal to that of ref inverter when driving $C_{REF}$)

Multiple Input Gates: **2-input NOR**

(n-channel devices sized same, p-channel devices sized the same)

Assume $L_n=L_p=L_{min}$ and driving a load of $C_{REF}$

$W_n=?$

$W_p=?$

Input capacitance = ?

$F\ell=?$

$t_{PROP}=?$  (worst case)

$W_n=W_{MIN}$

$W_p=6W_{MIN}$

$C_{INA}=C_{INB}=C_{OX}W_{MIN}L_{MIN}+6C_{OX}W_{MIN}L_{MIN}=7C_{OX}W_{MIN}L_{MIN}=\left(\frac{7}{4}\right)4C_{OX}W_{MIN}L_{MIN}=\left(\frac{7}{4}\right)C_{REF}$

$F\ell=\left(\frac{7}{4}\right)C_{REF}$  or  $F\ell=\frac{7}{4}$

$t_{PROP} = t_{REF}$  (worst case)
Device Sizing

Equal Worst Case Rise/Fall

Multiple Input Gates: 2-input NOR

(n-channel devices sized same, p-channel devices sized the same)

Assume \( L_n = L_p = L_{\text{min}} \) and driving a load of \( C_{\text{REF}} \)

\( W_n = ? \)

\( W_p = ? \)

Input capacitance = ?

\( f_i = ? \)

\( t_{\text{PROP}} = ? \) (worst case)

\( W_n = W_{\text{MIN}} \)

\( W_p = 6W_{\text{MIN}} \)

One degree of freedom was used to satisfy the constraint indicated

Other degree of freedom was used to achieve equal rise and fall times

\[
C_{\text{INA}} = C_{\text{INB}} = C_{\text{OX}} W_{\text{MIN}} L_{\text{MIN}} + 6 C_{\text{OX}} W_{\text{MIN}} L_{\text{MIN}} = 7 C_{\text{OX}} W_{\text{MIN}} L_{\text{MIN}} = \left( \frac{7}{4} \right) 4 C_{\text{OX}} W_{\text{MIN}} L_{\text{MIN}} = \left( \frac{7}{4} \right) C_{\text{REF}}
\]

\[
f_{i} = \left( \frac{7}{4} \right) C_{\text{REF}} \quad \text{or} \quad f_{i} = \frac{7}{4}
\]

\( t_{\text{PROP}} = t_{\text{REF}} \) (worst case)
Device Sizing

Equal Worst Case Rise/Fall (and equal to that of ref inverter when driving $C_{\text{REF}}$)

Multiple Input Gates: $k$-input NOR

$W_n=\text{?}$

$W_p=\text{?}$

Input capacitance = ?

$F_I=\text{?}$

$t_{\text{PROP}}=\text{?}$

$W_n=W_{\text{MIN}}$

$W_p=3kW_{\text{MIN}}$

$C_{\text{INX}}=C_{\text{OX}}W_{\text{MIN}}L_{\text{MIN}}+3kC_{\text{OX}}W_{\text{MIN}}L_{\text{MIN}}=(3k+1)C_{\text{OX}}W_{\text{MIN}}L_{\text{MIN}}=\left(\frac{3k+1}{4}\right)4C_{\text{OX}}W_{\text{MIN}}L_{\text{MIN}}=\left(\frac{3k+1}{4}\right)C_{\text{REF}}$

$F_I=\left(\frac{3k+1}{4}\right)C_{\text{REF}} \quad \text{or} \quad F_I=\frac{3k+1}{4}$

$t_{\text{PROP}}=t_{\text{REF}}$
Device Sizing

Multiple Input Gates: 2-input NAND

\( W_n = ? \)

\( W_p = ? \)

Input capacitance = ?

\( F_I = ? \)

\( t_{PROP} = ? \)

\( W_n = 2W_{MIN} \)

\( W_p = 3W_{MIN} \)

\( C_{INA} = C_{INB} = 2C_{OX}W_{MIN}L_{MIN} + 3C_{OX}W_{MIN}L_{MIN} = (5)C_{OX}W_{MIN}L_{MIN} = \left( \frac{5}{4} \right)4C_{OX}W_{MIN}L_{MIN} = \left( \frac{5}{4} \right)C_{REF} \)

\( F_I = \left( \frac{5}{4} \right)C_{REF} \quad or \quad F_I = \frac{5}{4} \)

\( t_{PROP} = t_{REF} \)
Device Sizing

Equal Worst Case Rise/Fall (and equal to that of ref inverter when driving $C_{\text{REF}}$)

Multiple Input Gates: $k$-input NAND

$W_n =$?

$W_p =$?

Input capacitance = ?

$F_I =$?

$t_{\text{PROP}} =$?

$W_n = kW_{\text{MIN}}$

$W_p = 3W_{\text{MIN}}$

$C_{\text{INx}} = kC_{\text{OX}}W_{\text{MIN}}L_{\text{MIN}} + 3C_{\text{OX}}W_{\text{MIN}}L_{\text{MIN}} = (3+k)C_{\text{OX}}W_{\text{MIN}}L_{\text{MIN}} = \left(\frac{3+k}{4}\right)4C_{\text{OX}}W_{\text{MIN}}L_{\text{MIN}} = \left(\frac{3+k}{4}\right)C_{\text{REF}}$

$F_I = \left(\frac{3+k}{4}\right)C_{\text{REF}} \quad \text{or} \quad F_I = \frac{3+k}{4}$

$t_{\text{PROP}} = t_{\text{REF}}$
**Device Sizing**

**Comparison of NAND and NOR Gates**

\[ W_n = kW_{\text{MIN}} \]

\[ W_p = 3kW_{\text{MIN}} \]

\[ C_{\text{INx}} = \left( \frac{3k+1}{4} \right) C_{\text{REF}} \]

\[ F_I = \left( \frac{3k+1}{4} \right) C_{\text{REF}} \quad \text{or} \quad F_I = \frac{3k+1}{4} \]

\[ t_{\text{PROP}} = t_{\text{REF}} \]
Device Sizing

Equal Worse-Case Rise/Fall Device Sizing Strategy
-- (same as $V_{\text{TRIP}} = V_{\text{DD}}/2$ for worst case delay in typical process considered in example)

Assume $\mu_n/\mu_p = 3$
$L_n = L_p = L_{\text{MIN}}$

$k$-input NAND

$W_n = kW_{\text{MIN}}$, $W_p = 3W_{\text{MIN}}$
$C_{\text{IN}} = \left( \frac{3+k}{4} \right) C_{\text{REF}}$
$F_l = \left( \frac{3+k}{4} \right)$

$k$-input NOR

$W_n = W_{\text{MIN}}$, $W_p = 3kW_{\text{MIN}}$
$C_{\text{IN}} = \left( \frac{3k+1}{4} \right) C_{\text{REF}}$
$F_l = \left( \frac{3k+1}{4} \right)$

INV

$W_n = W_{\text{MIN}}$, $W_p = 3W_{\text{MIN}}$
$C_{\text{IN}} = C_{\text{REF}}$
$F_l = 1$
Device Sizing

Multiple Input Gates:

- 2-input NOR
- 2-input NAND
- k-input NOR
- k-input NAND

Equal Worst Case Rise/Fall (and equal to that of ref inverter when driving $C_{REF}$)

- $W_n =$ ?
- $W_p =$ ?
- Fastest response ($t_{HL}$ or $t_{LH}$) = ?
- Worst case response ($t_{PROP}$, usually of most interest)?
- Input capacitance ($F_I$) = ?

Minimum Sized (assume driving a load of $C_{REF}$)

- $W_n = W_{min}$
- $W_p = W_{min}$
- Fastest response ($t_{HL}$ or $t_{LH}$) = ?
- Slowest response ($t_{HL}$ or $t_{LH}$) = ?
- Worst case response ($t_{PROP}$, usually of most interest)?
- Input capacitance ($F_I$) = ?
Device Sizing

Minimum Sized (assume driving a load of $C_{\text{REF}}$)

$W_n = W_{\text{min}}$  $W_p = W_{\text{min}}$

Input capacitance ($F I$) = ?

$$C_{\text{IN}} = C_{\text{OX}}W_nL_n + C_{\text{OX}}W_pL_p = C_{\text{OX}}W_{\text{min}}L_{\text{min}} + C_{\text{OX}}W_{\text{min}}L_{\text{min}} = 2C_{\text{OX}}W_{\text{min}}L_{\text{min}} = \frac{C_{\text{REF}}}{2}$$

$$F I = \frac{1}{2}$$

Fastest response ($t_{\text{HL}}$ or $t_{\text{HL}}$) = ?

Slowest response ($t_{\text{HL}}$ or $t_{\text{HL}}$) = ?

Worst case response ($t_{\text{PROP}}$, usually of most interest)?
Device Sizing – minimum size driving $C_{REF}$

**INV**

$$t_{\text{PROP}} = ?$$

$$t_{\text{PROP}} = 0.5t_{REF} + \frac{3}{2}t_{REF}$$

$$t_{\text{PROP}} = 2t_{REF}$$

$$Fl = \frac{C_{\text{REF}}}{2}$$

$$R_{PU} = R_{PD} = R_{PDREF}$$

**k-input NOR**

$$t_{\text{PROP}} = ?$$

$$t_{\text{PROP}} = 0.5t_{REF} + \frac{3k}{2}t_{REF}$$

$$t_{\text{PROP}} = \left(\frac{3k+1}{2}\right)t_{REF}$$

$$Fl = \frac{C_{\text{REF}}}{2}$$

$$R_{PD} = R_{PDREF}$$

$$R_{PU} = 3kR_{PDREF}$$

**k-input NAND**

$$t_{\text{PROP}} = ?$$

$$t_{\text{PROP}} = \frac{3}{2}t_{REF} + \frac{k}{2}t_{REF}$$

$$t_{\text{PROP}} = \frac{3+k}{2}t_{REF}$$

$$Fl = \frac{C_{\text{REF}}}{2}$$

$$R_{PD} = 3R_{PDREF}$$

$$R_{PU} = 3R_{PDREF}$$