Digital Circuit Design

Propagation Delay
  basic characterization

Device Sizing
  Inverter and multiple-input gates
MOS Logic Families

Inverters

Review from last lecture
Logic Levels

• CMOS logic
  – \( VH=VDD \), \( VL=VSS \)
  – Independent of transistor sizes

• Other MOS logic
  – \( VH \) and \( VL \) range reduced
  – \( VH \) and \( VL \) levels depends on sizes
  – \( VL \) may not exist if not sized properly
Review from last lecture

VH/VL Trip Voltage Levels

• CMOS logic
  – Dependent on transistor sizes
  – \( V_{TRIP} \approx \frac{V_{DD}}{2} \) when \( \frac{W_p}{W_n} = \frac{\mu_n}{\mu_p} \)

• Other MOS logic
  – Dependent on transistor sizes
  – \( V_{TRIP} \) to \{VH, VL\} distance reduced
  – \( V_{TRIP} \) may not exist if not sized properly
Review from last lecture

Static Power Consumption

• CMOS logic
  – Static ID = 0 for either VH or VL
  – Zero static power, under MOS square-law models

• Other MOS logic
  – ID=0 when VIN = VL
  – Significant ID when VIN = VH
  – Large static power consumption when number of transistors is large
Propagation Delay in Static CMOS Family

\[ t_{\text{PROP}} = t_{\text{HL}} + t_{\text{LH}} \approx C_L (R_{\text{PU}} + R_{\text{PD}}) \]

\[
R_{\text{PD}} = \frac{L_1}{\mu_n C_{\text{OX}} W_1 (V_{\text{DD}} - V_{\text{Tn}})} \\
R_{\text{PU}} = \frac{L_2}{\mu_p C_{\text{OX}} W_2 (V_{\text{DD}} + V_{\text{TP}})} \\
C_{\text{IN}} = C_{\text{OX}} (W_1 L_1 + W_2 L_2)
\]

\[ t_{\text{PROP}} = C_{\text{OX}} (W L_1 + W W L_2) \left( \frac{L_1}{C_{\text{OX}} W_1 (V_{\text{DD}} - V_T)} + \frac{L_2}{C_{\text{OX}} W_2 (V_{\text{DD}} + V_T)} \right) \]

If \( L_2 = L = L_{\text{min}} \) \( n = 3 \) \( p \),

\[ t_{\text{PROP}} = \frac{L_{\text{min}}^2}{n (V_{\text{DD}} / V_T)} (W_1 + W_2) \left( \frac{1}{W_1} + \frac{3}{W_2} \right) = \frac{L_{\text{min}}^2}{n (V_{\text{DD}} / V_T)} (4 + \frac{W_2}{W_1} + 3 \frac{W_1}{W_2}) \]

For min size: \( W_2 = W_1 = W_{\text{min}} \)

For equal rise/fall: \( W_2 = 3 W_1 \)

For min delay: \( W_2 = \sqrt{3} W_1 \)

\[ t_{\text{PROP}} = \frac{8 L_{\text{min}}^2}{n (V_{\text{DD}} / V_T)} \]

\[ t_{\text{PROP}} = \frac{8 L_{\text{min}}^2}{n (V_{\text{DD}} / V_T)} \]

\[ t_{\text{PROP}} = \frac{(4 + 2 \sqrt{3}) L_{\text{min}}^2}{n (V_{\text{DD}} / V_T)} \]
### Approximate BSIM values

<table>
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<th>process</th>
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<th>u</th>
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<th>VDD</th>
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<td>45</td>
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</table>

For min L transistors, mobility will saturate as field strength reaches a certain level.
The propagation delay through $k$ levels of logic is approximately the sum of the individual delays in the same path.
Propagation Delay in Static CMOS Family

Example:

\[ t_{HL} = t_{HL4} + t_{LH3} + t_{HL2} + t_{LH1} \]

\[ t_{LH} = t_{LH4} + t_{HL3} + t_{LH2} + t_{HL1} \]

\[ t_{PROP} = t_{LH} + t_{HL} = (t_{LH4} + t_{HL3} + t_{LH2} + t_{HL1}) + (t_{HL4} + t_{LH3} + t_{HL2} + t_{LH1}) \]

\[ t_{PROP} = t_{LH} + t_{HL} = (t_{LH4} + t_{HL4}) + (t_{LH3} + t_{HL3}) + (t_{LH2} + t_{HL2}) + (t_{LH1} + t_{HL1}) \]

\[ t_{PROP} = t_{PROP4} + t_{PROP3} + t_{PROP2} + t_{PROP1} \]
Propagation Delay in Static CMOS Family

Propagation through k levels of logic

\[ t_{HL} \approx t_{HLk} + t_{LH(k-1)} + t_{HL(k-2)} + \cdots + t_{XY1} \]
\[ t_{LH} \approx t_{LHk} + t_{HL(k-1)} + t_{LH(k-2)} + \cdots + t_{YX1} \]

where \( x=H \) and \( Y=L \) if \( k \) odd and \( X=L \) and \( Y=h \) if \( k \) even

\[ t_{PROP} = \sum_{i=1}^{k} t_{PROP_i} \]

Will return to propagation delay after we discuss device sizing
Digital Circuit Design

- Hierarchical Design
- Basic Logic Gates
- Properties of Logic Families
- Characterization of CMOS Inverter
- Static CMOS Logic Gates
  - Ratio Logic
- Propagation Delay
  - Simple analytical models
  - Elmore Delay
- Sizing of Gates

- Propagation Delay with Multiple Levels of Logic
- Optimal driving of Large Capacitive Loads
- Power Dissipation in Logic Circuits
- Other Logic Styles
- Array Logic
- Ring Oscillators
Device Sizing

Will consider the inverter first

Strategies?

Degrees of Freedom?
Device Sizing

Degrees of Freedom?

Strategies?
Device Sizing

• \( V_H \) and \( V_L \) are independent of device sizes
• With \( L_1=L_2=L_{\text{min}} \), 2 degrees of freedom: \( W_1, W_2 \)

Sizing Strategies:

• Minimum die area
• Minimum Propagation delay
• Fixing \( V_{\text{TRIP}} \) to maximize distance to \{VH, VL\}
• Equal rise-fall times
  (equal worst-case rise and fall times)
• Minimum power dissipation
• Minimum time required to drive a given load
• Minimum input capacitance
Device Sizing

Assume $V_{Tn} = 0.2V_{DD}$, $V_{Tp} = -0.2V_{DD}$, $\mu_n/\mu_p = 3$, $L_1 = L_2 = L_{min}$

Sizing Strategy: minimum sized

$W_n = ?, \quad W_p = ?, \quad V_{trip} = ?, \quad t_{HL} = ?, \quad t_{LH} = ?$

$R_{PD} = \frac{L_1}{\mu_n C_{OX} W_1 (V_{DD} - V_{Tn})}$

$R_{PU} = \frac{L_2}{\mu_p C_{OX} W_2 (V_{DD} + V_{Tp})}$

$C_{IN} = C_{OX} (W_1 L_1 + W_2 L_2)$
Device Sizing

Assume $V_{Tn}=0.2V_{DD}$, $V_{Tp}=-0.2V_{DD}$, $\mu_n/\mu_p=3$, $L_1=L_2=L_{min}$

Sizing Strategy: minimum sized

$W_n=?$, $W_p=?$, $V_{trip}=?$, $t_{HL}=?$, $t_{LH}=?$

$W_1=W_2=W_{MIN}$

also provides minimum input capacitance

$t_{HL}=R_{PD}C_L$

$t_{LH}=3R_{PD}C_L$

$t_{LH}$ is longer than $t_{HL}$

$t_{PROP}=4R_{PD}C_L$

$v_{trip} = \frac{(0.2V_{DD}) + (V_{DD} - 0.2V_{DD})}{\sqrt{\frac{1}{3}}} = .42V_{DD}$
Device Sizing

Assume \( V_{Tn} = 0.2V_{DD} \), \( V_{Tp} = -0.2V_{DD} \), \( \mu_n/\mu_p = 3 \), \( L_1 = L_2 = L_{\text{min}} \)

Sizing strategy: Equal (worst case) rise and fall times

\( W_n = ?, \ W_p = ?, \ V_{\text{trip}} = ?, \ t_{\text{HL}} = ?, \ t_{\text{LH}} = ? \)

\[ R_{PD} = \frac{L_{\text{min}}}{\mu_n C_{OX} W_1 (0.8V_{DD})} \]

\[ R_{ PU} = \frac{L_{\text{min}}}{3\mu_n C_{OX} W_2 (0.8V_{DD})} \]
Device Sizing

Assume $V_{Tn} = 0.2V_{DD}$, $V_{Tp} = -0.2V_{DD}$, $\mu_n/\mu_p = 3$, $L_1 = L_2 = L_{\text{min}}$

Sizing strategy: Equal (worst case) rise and fall times

Thus

$$\frac{t_{LH}}{t_{HL}} = \frac{R_{PU}C_{IN}}{R_{PD}C_{IN}} \Rightarrow R_{PU} = R_{PD}$$

Thus

$$\frac{L_1}{u_n C_{OX} W_1 (V_{DD} - V_{Tn})} = \frac{L_2}{u_p C_{OX} W_2 (V_{DD} + V_{Tp})}$$

with $L_1 = L_2$ and $V_{Tp} = -V_{Tn}$ we must have

$$\frac{W_2}{W_1} = \frac{\mu_n}{\mu_p} \approx 3$$

What about the second degree of freedom?

$W_1 = W_{\text{MIN}}$

$V_{\text{TRIP}} =$?
Device Sizing

Assume $V_{Tn}=0.2V_{DD}$, $V_{Tp}=-0.2V_{DD}$, $\mu_n/\mu_p=3$, $L_1=L_2=L_{min}$

Sizing strategy: Equal (worst-case) rise and fall times

$W_n=W_{MIN}, W_p=3W_{MIN}, V_{trip}=?, t_{HL}=?, t_{LH}=?$

$$
V_{TRIP} = \frac{(V_{Tn})+(V_{DD}+V_{Tp})}{1+\sqrt{\frac{\mu_p}{\mu_n} \frac{W_2}{W_1} \frac{L_1}{L_2}}} = \frac{0.2V_{DD}+0.8V_{DD}}{2} = \frac{V_{DD}}{2}
$$

$$
t_{HL} = t_{LH} = R_{pd}C_L = \frac{L_{min}}{\mu_n C_{OX} W_{MIN} (0.8V_{DD})} C_L
$$

$$
t_{PROP} = 2 R_{pd}C_L
$$

For a fixed $C_L$, how does $t_{PROP}$ compare for the minimum-sizing compared to equal rise/fall sizing?
Device Sizing

Assume $V_{Tn}=0.2V_{DD}$, $V_{Tp}=-0.2V_{DD}$, $\mu_n/\mu_p=3$, $L_1=L_2=L_{\text{min}}$

Sizing strategy: Fixed $V_{\text{TRIP}}=V_{DD}/2$

$W_n=?$, $W_p=?$, $V_{\text{trip}}=?$, $t_{\text{HL}}=?$, $t_{\text{LH}}=?$
Device Sizing

Assume $V_{Tn}=0.2V_{DD}$, $V_{Tp}=-0.2V_{DD}$, $\mu_n/\mu_p=3$, $L_1=L_2=L_{\text{min}}$

Sizing strategy: Fixed $V_{\text{TRIP}}=V_{DD}/2$

$W_n=\ ?, \ W_p=\ ?, \ V_{\text{trip}}=\ ?, t_{HL}=\ ?, t_{LH}=\ ?$

Set $V_{\text{TRIP}}=V_{DD}/2$

$$V_{\text{TRIP}} = \frac{(0.2V_{DD}) + (V_{DD} - 0.2V_{DD}) \sqrt{\frac{\mu_p W_2 L_1}{\mu_n W_1 L_2}}}{1 + \sqrt{\frac{\mu_p W_2 L_1}{\mu_n W_1 L_2}}} = \frac{V_{DD}}{2}$$

Solving, obtain

$$\frac{W_2}{W_1} = \frac{\mu_n}{\mu_p}$$

$W_n=W_{\text{MIN}}$, $W_p=3W_{\text{MIN}}$

- This is the same sizing as was obtained for equal worst-case rise and fall times so $t_{HL}=t_{LH}=R_{pd}C_L$
- This is no coincidence !!! Why?
- These properties guide the definition of the process parameters provided by the foundry
Device Sizing

- $V_H$ and $V_L$ are independent of device sizes
- With $L_1 = L_2 = L_{\text{min}}$, 2 degrees of freedom: $W_1$, $W_2$

Sizing Strategies:

- Minimum die area
- Minimum Propagation delay
- Fixing $V_{\text{TRIP}}$ to maximize distance to \{VH, VL\}
- Equal rise-fall times
  (equal worst-case rise and fall times)
- Minimum power dissipation
- Minimum time required to drive a given load
- Minimum input capacitance
**Device Sizing**

Assume $V_{Tn}=0.2V_{DD}$, $V_{Tp}=-0.2V_{DD}$, $\mu_n/\mu_p=3$, $L_1=L_2=L_{\text{min}}$

### Sizing Strategy Summary

<table>
<thead>
<tr>
<th></th>
<th>Minimum Size</th>
<th>$V_{TRIP}=V_{DD}/2$</th>
<th>Equal Rise/Fall</th>
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<td><strong>Size</strong></td>
<td>$W_n=W_p=W_{\text{min}}$</td>
<td>$W_n=W_{\text{min}}$</td>
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<tr>
<td></td>
<td>$L_p=L_n=L_{\text{min}}$</td>
<td>$W_p=3W_{\text{min}}$</td>
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<tr>
<td>$t_{HL}$</td>
<td>$R_{pd}C_L$</td>
<td>$R_{pd}C_L$</td>
<td>$R_{pd}C_L$</td>
</tr>
<tr>
<td>$t_{LH}$</td>
<td>$3R_{pd}C_L$</td>
<td>$R_{pd}C_L$</td>
<td>$R_{pd}C_L$</td>
</tr>
<tr>
<td>$t_{PROP}$</td>
<td>$4R_{pd}C_L$</td>
<td>$2R_{pd}C_L$</td>
<td>$2R_{pd}C_L$</td>
</tr>
<tr>
<td>$V_{trip}$</td>
<td>$V_{TRIP}=0.42V_{DD}$</td>
<td>$V_{TRIP}=0.5V_{DD}$</td>
<td>$V_{TRIP}=0.5V_{DD}$</td>
</tr>
</tbody>
</table>

- For a fixed load $C_L$, the minimum-sized structure has a higher $t_{PROP}$
- If the load is another inverter, $C_L$ is half, so $t_{PROP}$ remain the same
- This will be investigated later
The reference inverter

Assume $\frac{\mu_n}{\mu_p} = 3$
$L_n = L_p = L_{\text{MIN}}$

$W_n = W_{\text{MIN}}, \ W_p = 3W_n$

$C_{\text{REF}} = C_{\text{INREF}} = 4C_{\text{OX}} W_{\text{MIN}} L_{\text{MIN}}$

$R_{\text{PDREF}} = \frac{L_{\text{MIN}}}{\mu_n C_{\text{OX}} W_{\text{MIN}} (V_{DD} - V_{Tn})}$
$\quad = \frac{L_{\text{MIN}}}{\mu_n C_{\text{OX}} W_{\text{MIN}} (0.8V_{DD})}$

$R_{\text{PUREF}} = \frac{L_{\text{MIN}}}{\mu_p C_{\text{OX}} 3W_{\text{MIN}} (V_{DD} + V_{Tp})}$
$\quad = R_{\text{PDREF}}$

- Have sized the reference inverter with $W_p/W_n = \mu_n/\mu_p$
- In standard processes, provides $V_{\text{TRIP}} \approx V_{DD}/2$ and $t_{HL} \approx t_{LH}$
- Any other sizing strategy could have been used for the reference inverter but this is most convenient
Reference Inverter

The reference inverter pair

Assume $\mu_n/\mu_p = 3$

$L_n = L_p = L_{MIN}$

$W_n = W_{MIN}$, $W_p = 3W_n$

\[ C_{L1} = C_{REF} = 4C_{OX} \cdot W_{MIN} \cdot L_{MIN} \]

\[ t_{\text{REF}} = t_{\text{PROPREF}} = t_{\text{HLREF}} + t_{\text{LHREF}} = 2R_{PDREF} \cdot C_{REF} \]
Reference Inverter

The reference inverter pair

Assume $\mu_n/\mu_p = 3$

$L_n = L_p = L_{MIN}$

$W_n = W_{MIN}, W_p = 3W_n$

Summary: parameters defined from reference inverter:

$$C_{REF} = 4C_{OX} W_{MIN} L_{MIN}$$

$$R_{PDREF} = \frac{L_{MIN}}{\mu_n C_{OX} W_{MIN} (V_{DD} - V_{Tn})}$$

$$t_{REF} = 2R_{PDREF} C_{REF}$$

$$C_{REF} = 4C_{OX} W_{MIN} L_{MIN}$$
The Reference Inverter

\[ R_{PDREF} = R_{PUREF} \]

\[ C_{REF} = C_{IN} = 4C_{OX} W_{MIN} L_{MIN} \]

\[ R_{PDREF} = \frac{L_{MIN}}{\mu_n C_{OX} W_{MIN} (V_{DD} - V_{Tn})} = \frac{L_{MIN}}{\mu_n C_{OX} W_{MIN} (0.8V_{DD})} \]

\[ t_{HLREF} = t_{LHREF} = R_{PDREF} C_{REF} \]

\[ t_{REF} = t_{HLREF} + t_{LHREF} = 2R_{PDREF} C_{REF} \]

Assume \( \mu_n / \mu_p = 3 \)

\( W_n = W_{MIN}, \quad W_p = 3W_{MIN} \)

\( L_n = L_p = L_{MIN} \)

In 0.5u proc \( t_{REF} = 20ps, \quad C_{REF} = 4fF, \quad R_{PDREF} = R_{PUREF} = 2.5K \)

(Note: This \( C_{OX} \) is somewhat larger than that in the 0.5u ON process)
How does the propagation delay compare for a minimum-sized strategy to that of an equal rise/fall sizing strategy?

Minimum Sized
\[ W_2 = W_1 = W_{\text{MIN}} \]

Reference Inverter
\[ W_2 = (\mu_n/\mu_p)W_1, \quad W_1 = W_{\text{MIN}} \]

\[ t_{\text{PROP}} = t_{\text{REF}} \]
Device Sizing

The minimum-sized inverter pair

Assume $\frac{\mu_n}{\mu_p} = 3$

$L_n = L_p = L_{\text{MIN}}$

$W_n = W_{\text{MIN}}, W_p = W_n$

$C_{\text{REF}} = 4C_{\text{OX}} W_{\text{MIN}} L_{\text{MIN}}$

$C_{L1} = 0.5C_{\text{REF}} = 2C_{\text{OX}} W_{\text{MIN}} L_{\text{MIN}}$

$R_{\text{PDREF}} = \frac{L_{\text{MIN}}}{\mu_n C_{\text{OX}} W_{\text{MIN}} (V_{\text{DD}} - V_{Tn})}$

$v_{Tn} = 2V_{\text{DD}}$

$= \frac{L_{\text{MIN}}}{\mu_n C_{\text{OX}} W_{\text{MIN}} (0.8V_{\text{DD}})}$

$t_{\text{PROP}} = t_{\text{HLREF}} + t_{\text{LHREF}} = R_{\text{PDREF}} (0.5C_{\text{REF}}) + 3R_{\text{PDREF}} (0.5C_{\text{REF}}) = 2R_{\text{PDREF}} C_{\text{REF}}$

$t_{\text{PROP}} = t_{\text{REF}}$
Propagation Delay

How does the propagation delay compare for a minimum-sized strategy to that of an equal rise/fall sizing strategy?

Minimum Sized

\[ W_2 = W_1 = W_{\text{MIN}} \]

\[ t_{\text{PROP}} = t_{\text{REF}} \]

They are the same!

Reference Inverter

\[ W_2 = \left( \frac{\mu_n}{\mu_p} \right) W_1, \quad W_1 = W_{\text{MIN}} \]

\[ t_{\text{PROP}} = t_{\text{REF}} \]

Even though the \( t_{\text{LH}} \) rise time has been reduced with the equal rise/fall sizing strategy, this was done at the expense of an increase in the total load capacitance that resulted in no net change in propagation delay!
Will consider now the multiple-input gates

Will consider both minimum sizing and equal worst-case rise/fall

Will assume $C_L$ (not shown)=$C_{REF}$

Will initially size so gate drive capability is same as that of ref inverter

Note: worst-case has been added since fall time in NOR gates or rise time in NAND gates depends upon how many transistors are conducting
Fan In

- The Fan In (FI) to an input of a gate device, circuit or interconnect that is capacitive is the input capacitance.

- Often this is normalized to some capacitance (typically $C_{\text{REF}}$ of ref inverter).

\[ \text{FI} = C_{\text{IN}} \quad \text{alternatively} \quad \text{FI} = \frac{C_{\text{IN}}}{C_{\text{REF}}} \]
Sizing of Multiple-Input Gates

Analysis strategy: Express delays in terms of those of reference inverter

Reference Inverter

\[ V_{DD} \]

\[ V_{IN} \rightarrow M_1 \rightarrow V_{OUT} \rightarrow M_2 \]

Assume \( \mu_n/\mu_p = 3 \)

\[ W_n = W_{MIN}, \quad W_p = 3W_{MIN} \]

\[ L_n = L_p = L_{MIN} \]

In 0.5u proc \( t_{REF} = 20\text{ps}, \quad C_{REF} = 4\text{fF}, R_{PDREF} = 2.5\text{K} \)

\[ t_{HLREF} = t_{LHREF} = R_{PDREF} C_{REF} \]

\[ t_{REF} = t_{HLREF} + t_{LHREF} = 2R_{PDREF} C_{REF} \]
Device Sizing

Multiple Input Gates:
- 2-input NOR
- 2-input NAND
- k-input NOR
- k-input NAND

Equal Worst Case Rise/Fall (and equal to that of ref inverter when driving $C_{REF}$)
- $W_n = ?$
- $W_p = ?$

Fastest response ($t_{HL}$ or $t_{LH}$) = ?

Worst case response ($t_{PROP}$, usually of most interest)?

Input capacitance ($F_I$) = ?

Minimum Sized (assume driving a load of $C_{REF}$)
- $W_n = W_{min}$
- $W_p = W_{min}$

Fastest response ($t_{HL}$ or $t_{LH}$) = ?

Slowest response ($t_{HL}$ or $t_{LH}$) = ?

Worst case response ($t_{PROP}$, usually of most interest)?

Input capacitance ($F_I$) = ?
Device Sizing

Equal Worst Case Rise/Fall (and equal to that of ref inverter when driving $C_{REF}$)

Multiple Input Gates: 2-input NOR

(n-channel devices sized same, p-channel devices sized the same)

Assume $L_n=L_p=L_{\text{min}}$ and driving a load of $C_{REF}$

$W_n = ?$

$W_p = ?$

Input capacitance = ?

$FI = ?$

$t_{PROP} = ?$ (worst case)

$W_n = W_{\text{MIN}}$

$W_p = 6W_{\text{MIN}}$

$C_{INA} = C_{INB} = COX W_{\text{MIN}} L_{\text{MIN}} + 6COX W_{\text{MIN}} L_{\text{MIN}} = 7COX W_{\text{MIN}} L_{\text{MIN}} = \left( \frac{7}{4} \right) 4COX W_{\text{MIN}} L_{\text{MIN}} = \left( \frac{7}{4} \right) C_{REF}$

$FI = \left( \frac{7}{4} \right) C_{REF}$ or $FI = \frac{7}{4}$

$t_{PROP} = t_{REF}$ (worst case)
Device Sizing

Equal Worst Case Rise/Fall

Multiple Input Gates: 2-input NOR

(n-channel devices sized same, p-channel devices sized the same)

Assume \( L_n = L_p = L_{\text{min}} \) and driving a load of \( C_{\text{REF}} \)

\[ W_n = ? \]

\[ W_p = ? \]

Input capacitance = ?

\[ F_I = ? \]

\[ t_{\text{PROP}} = ? \] (worst case)

\[ W_n = W_{\text{MIN}} \]

\[ W_p = 6W_{\text{MIN}} \]

One degree of freedom was used to satisfy the constraint indicated

Other degree of freedom was used to achieve equal rise and fall times

\[ C_{\text{INA}} = C_{\text{INB}} = C_{\text{OX}}W_{\text{MIN}}L_{\text{MIN}} + 6C_{\text{OX}}W_{\text{MIN}}L_{\text{MIN}} = 7C_{\text{OX}}W_{\text{MIN}}L_{\text{MIN}} = \frac{7}{4}C_{\text{OX}}W_{\text{MIN}}L_{\text{MIN}} = \frac{7}{4}C_{\text{REF}} \]

\[ F_I = \left( \frac{7}{4} \right)C_{\text{REF}} \quad \text{or} \quad F_I = \frac{7}{4} \]

\[ t_{\text{PROP}} = t_{\text{REF}} \] (worst case)
Device Sizing

Equal Worst Case Rise/Fall (and equal to that of ref inverter when driving \( C_{\text{REF}} \))

Multiple Input Gates: \( k \)-input NOR

\[ W_n = W_{\text{MIN}} \]

\[ W_p = 3k W_{\text{MIN}} \]

\[ C_{\text{INx}} = C_{\text{OX}} W_{\text{MIN}} l_{\text{MIN}} + 3k C_{\text{OX}} W_{\text{MIN}} l_{\text{MIN}} = (3k+1) C_{\text{OX}} W_{\text{MIN}} l_{\text{MIN}} = \left( \frac{3k+1}{4} \right) 4 C_{\text{OX}} W_{\text{MIN}} l_{\text{MIN}} = \left( \frac{3k+1}{4} \right) C_{\text{REF}} \]

\[ \text{FI} = \left( \frac{3k+1}{4} \right) C_{\text{REF}} \quad \text{or} \quad \text{FI} = \frac{3k+1}{4} \]

\[ t_{\text{PROP}} = t_{\text{REF}} \]
Device Sizing

Equal Worst Case Rise/Fall (and equal to that of ref inverter when driving $C_{REF}$)

Multiple Input Gates: 2-input NAND

$W_n = ?$

$W_p = ?$

Input capacitance = ?

$F_l = ?$

$t_{PROP} = ?$

$W_n = 2W_{MIN}$

$W_p = 3W_{MIN}$

$C_{INA} = C_{INB} = 2C_{OX}W_{MIN}L_{MIN} + 3C_{OX}W_{MIN}L_{MIN} = (5)C_{OX}W_{MIN}L_{MIN} = \left(\frac{5}{4}\right)C_{REF}$

$F_l = \left(\frac{5}{4}\right)C_{REF}$ or $F_l = \frac{5}{4}$

$t_{PROP} = t_{REF}$
Device Sizing

Equal Worst Case Rise/Fall (and equal to that of ref inverter when driving $C_{REF}$)

Multiple Input Gates: k-input NAND

$W_n = ?$

$W_p = ?$

Input capacitance = ?

$F_I = ?$

$t_{PROP} = ?$

$W_n = kW_{MIN}$

$W_p = 3W_{MIN}$

$C_{INx} = kC_{OX}W_{MIN}L_{MIN} + 3C_{OX}W_{MIN}L_{MIN} = (3+k)C_{OX}W_{MIN}L_{MIN} = \left( \frac{3+k}{4} \right) 4C_{OX}W_{MIN}L_{MIN} = \left( \frac{3+k}{4} \right) C_{REF}$

$F_I = \left( \frac{3+k}{4} \right) C_{REF}$ or $F_I = \frac{3+k}{4}$

$t_{PROP} = t_{REF}$
Device Sizing

Comparison of NAND and NOR Gates

\[ W_n = W_{MIN} \]

\[ W_p = 3kW_{MIN} \]

\[ C_{INx} = \left( \frac{3k+1}{4} \right) C_{REF} \]

\[ FL = \left( \frac{3k+1}{4} \right) C_{REF} \quad \text{or} \quad FL = \frac{3k+1}{4} \]

\[ t_{PROP} = t_{REF} \]
Device Sizing

Equal Worse-Case Rise/Fall Device Sizing Strategy
-- (same as $V_{TRIP}=V_{DD}/2$ for worst case delay in typical process considered in example)

Assume $\mu_n/\mu_p=3$
$L_n=L_p=L_{MIN}$

**INV**

$W_n=W_{MIN}, \quad W_p=3W_{MIN}$
$C_{IN}=C_{REF}$
$FI=1$

**k-input NOR**

$W_n=W_{MIN}, \quad W_p=3kW_{MIN}$

$C_{IN} = \left(\frac{3k+1}{4}\right)C_{REF}$
$FI=\left(\frac{3k+1}{4}\right)$

**k-input NAND**

$W_n=kW_{MIN}, \quad W_p=3W_{MIN}$

$C_{IN} = \left(\frac{3+k}{4}\right)C_{REF}$
$FI=\left(\frac{3+k}{4}\right)$
Multiple Input Gates:

2-input NOR

2-input NAND

k-input NOR

k-input NAND

Equal Worst Case Rise/Fall (and equal to that of ref inverter when driving $C_{REF}$)

$W_n =$?

$W_p =$?

Fastest response ($t_{HL}$ or $t_{LH}$) = ?

Worst case response ($t_{PROP}$, usually of most interest)?

Input capacitance ($F_I$) = ?

Minimum Sized  (assume driving a load of $C_{REF}$)

$W_n = W_{min}$

$W_p = W_{min}$

Fastest response ($t_{HL}$ or $t_{LH}$) = ?

Slowest response ($t_{HL}$ or $t_{LH}$) = ?

Worst case response ($t_{PROP}$, usually of most interest)?

Input capacitance ($F_I$) = ?
Minimum Sized (assume driving a load of \( C_{\text{REF}} \))

\[
W_n = W_{\text{min}} \quad W_p = W_{\text{min}}
\]

Input capacitance (\( F_I \)) = ?

\[
C_{\text{IN}} = C_{\text{OX}}W_nL_n + C_{\text{OX}}W_pL_p = C_{\text{OX}}W_{\text{min}}L_{\text{min}} + C_{\text{OX}}W_{\text{min}}L_{\text{min}} = 2C_{\text{OX}}W_{\text{min}}L_{\text{min}} = \frac{C_{\text{REF}}}{2}
\]

\[
F_I = \frac{1}{2}
\]

Fastest response (\( t_{\text{HL}} \) or \( t_{\text{LH}} \)) = ?

Slowest response (\( t_{\text{HL}} \) or \( t_{\text{LH}} \)) = ?

Worst case response (\( t_{\text{PROP}} \), usually of most interest)?
Device Sizing – minimum size driving $C_{\text{REF}}$

**INV**

$t_{\text{PROP}} = \ ?$

$t_{\text{PROP}} = 0.5t_{\text{REF}} + \frac{3}{2}t_{\text{REF}}$

$t_{\text{PROP}} = 2t_{\text{REF}}$

$F_I = \frac{C_{\text{REF}}}{2}$

$R_{\text{PU}} = 3R_{\text{PDREF}}$

$R_{\text{PD}} = R_{\text{PDREF}}$

**k-input NOR**

$t_{\text{PROP}} = \ ?$

$t_{\text{PROP}} = 0.5t_{\text{REF}} + \frac{3k}{2}t_{\text{REF}}$

$t_{\text{PROP}} = \left(\frac{3k+1}{2}\right)t_{\text{REF}}$

$F_I = \frac{C_{\text{REF}}}{2}$

$R_{\text{PD}} = R_{\text{PDREF}}$

$R_{\text{PU}} = 3kR_{\text{PDREF}}$

**k-input NAND**

$t_{\text{PROP}} = \ ?$

$t_{\text{PROP}} = \frac{3}{2}t_{\text{REF}} + \frac{k}{2}t_{\text{REF}}$

$t_{\text{PROP}} = \frac{3+k}{2}t_{\text{REF}}$

$F_I = \frac{C_{\text{REF}}}{2}$

$R_{\text{PD}} = kR_{\text{PDREF}}$

$R_{\text{PU}} = 3R_{\text{PDREF}}$
End of Lecture 39