EE 330
Lecture 4

Digital Systems – A preview
Quiz 3

The defect density is often considered as proprietary information. Assume, however, that a process engineer had a lapse of thought and disclosed that they were obtaining a 95% hard yield on a circuit. The competitor bought the circuit and measured the die and found the area to be 0.2cm$^2$. What was the defect density in the process?

\[ A = 0.2\text{cm}^2 \]
And the number is ....
And the number is ....
Quiz 3

The defect density is often considered as proprietary information. Assume, however, that a process engineer had a lapse of thought and disclosed that they were obtaining a 95% hard yield on a circuit. The competitor bought the circuit and measured the die and found the area to be 0.2cm². What was the defect density in the process?

Solution:

\[ Y = e^{-Ad} \]

\[ d = - \frac{\ln Y}{A} = - \frac{\ln 0.95}{0.2} = 0.26/\text{cm}^2 \]
Defects in a Wafer

- Dust particles and other undesirable processes cause defects
- Defects in manufacturing cause yield loss
Hard Fault Model

\[ Y_H = e^{-Ad} \]

\( Y_H \) is the probability that the die does not have a hard fault

\( A \) is the die area

\( d \) is the defect density (typically \( 1 \text{cm}^{-2} < d < 2 \text{cm}^{-2} \))

Industry often closely guards the value of \( d \) for their process

Other models, which may be better, have the same general functional form
Soft Fault Model

\[ P_{SOFT} = \int_{X_{MIN}}^{X_{MAX}} f(x) \, dx \]

- \( P_{SOFT} \) is the soft fault yield
- \( f(x) \) is the probability density function of the parameter of interest
- \( X_{MIN} \) and \( X_{MAX} \) define the acceptable range of the parameter of interest

Some circuits may have several parameters that must meet performance requirements.
Soft Fault Model

If there are $k$ parameters that must meet parametric performance requirements and if the random variables characterizing these parameters are uncorrelated, then the soft yield is given by

$$Y_S = \prod_{j=1}^{k} P_{SOFT_j}$$
Overall Yield

If both hard and soft faults affect the yield of a circuit, the overall yield is given by the expression

\[ Y = Y_H Y_S \]
Basic Logic Circuits
Basic Logic Circuits

• Will present a brief description of logic circuits based upon simple models and qualitative description of processes
• Will discuss process technology needed to develop better models
• Will provide more in-depth discussion of logic circuits based upon better device models
Models of Devices

• Several models of the electronic devices will be introduced
  – Complexity
  – Accuracy
  – Insight
  – Application

• Will use the simplest model that can provide acceptable results for any given application
MOS Transistor
Qualitative Discussion of n-channel Operation

- **Source**
- **Gate**
- **Drain**
- **Bulk**

Diagram of an n-channel MOSFET with color codes:
- n-type
- n+ type
- p-type
- p+ type
- SiO₂ (insulator)
- POLY (conductor)
MOS Transistor
Qualitative Discussion of n-channel Operation

Behavioral Description of Basic Operation

If $V_{GS}$ is large, short circuit exists between drain and source

If $V_{GS}$ is small, open circuit exists between drain and source
MOS Transistor
Qualitative Discussion of n-channel Operation

Equivalent Circuit for n-channel MOSFET

This is the first model we have for the n-channel MOSFET!
MOS Transistor MODEL

Equivalent Circuit for n-channel MOSFET

Mathematically:

\[ I_D = 0 \quad \text{if} \quad V_G \quad \text{is high} \]
\[ V_D = 0 \quad \text{if} \quad V_G \quad \text{is low} \]
MOS Transistor
Qualitative Discussion of p-channel Operation

Bulk

Source

Gate

Drain

p-channel MOSFET

Source

Drain

Gate

n-type

n+ type

p-type

p+ type

SiO2 (insulator)

POLY (conductor)
MOS Transistor
Qualitative Discussion of p-channel Operation

p-channel MOSFET

Behavioral Description of Basic Operation

If \( V_{GS} \) is small (negative), short circuit exists between drain and source

If \( V_{GS} \) is large (near 0), open circuit exists between drain and source
MOS Transistor
Qualitative Discussion of p-channel Operation

This is the first model we have for the p-channel MOSFET!
MOS Transistor MODEL

Equivalent Circuit for p-channel MOSFET

Mathematically:

\[ I_D = 0 \quad \text{if } V_G \text{ is low} \]
\[ V_D = 0 \quad \text{if } V_G \text{ is high} \]
MOS Transistor
Comparison of Operation

D
- G = 0
- G = 1

S

D
- G = 0
- G = 1

S
Logic Circuits

Circuit Behaves as a Boolean Inverter
Logic Circuits

Truth Table

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Logic Circuits

A = 0
B = 0

C = 1

V_{DD}
Logic Circuits

A = 1
B = 0
C = 0
Logic Circuits

A = 1
B = 1
C = 0
Logic Circuits

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Logic Circuits

NAND Gate

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Other logic circuits

- Other methods for designing logic circuits exist
- Insight will be provided on how other logic circuits evolve
- Several different types of logic circuits are often used simultaneously in any circuit design
Pull-up and Pull-down Networks

PU network comprised of p-channel device
PD network comprised of n-channel device
One and only one of these networks is conducting at the same time
Pull-up and Pull-down Networks

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Pull-up and Pull-down Networks

1. PU network comprised of p-channel devices
2. PD network comprised of n-channel devices
3. One and only one of these networks is conducting at the same time

What are $V_H$ and $V_L$?
What is the power dissipation?
How fast are these logic circuits?
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What is the power dissipation?
How fast are these logic circuits?

Consider the inverter
Use switch-level model for MOS devices
What are $V_H$ and $V_L$?
What is the power dissipation?
How fast are these logic circuits?

Consider the inverter

Use switch-level model for MOS devices

$V_H = V_{DD}$

$V_L = 0$

$I_D = 0$ thus $P_H = P_L = 0$

$t_{HL} = t_{LH} = 0$ (too good to be true?)
Pull-up and Pull-down Networks

1. PU network comprised of p-channel devices
2. PD network comprised of n-channel devices
3. One and only one of these networks is conducting at the same time

What are $V_H$ and $V_L$?
$V_H = V_{DD}$, $V_L = 0$

What is the power dissipation?
$P_H = P_L = 0$

How fast are these logic circuits?
$t_{HL} = t_{LH} = 0$ (too good to be true?)

These characteristics are inherent in Boolean circuits with these 3 properties
Pull-up and Pull-down Networks

Concept can be extended to arbitrary number of inputs

n-input NOR gate

VDD

X1
X2
... 
Xn

Y

n-input NAND gate

VDD

X1
X2
... 
Xn

Y

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Pull-up and Pull-down Networks

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Pull-up and Pull-down Networks

1. PU network comprised of p-channel devices
2. PD network comprised of n-channel devices
3. One and only one of these networks is conducting at the same time

\[ V_H = V_{DD}, \quad V_L = 0 \]
\[ P_H = P_L = 0 \]
\[ t_{HL} = t_{LH} = 0 \]
In this class, logic circuits that are implemented by interconnecting multiple-input NAND and NOR gates will be referred to as “Static CMOS Logic”.

Since the set of NAND gates is complete, any combinational logic function can be realized with the NAND circuit structures considered thus far.

Since the set NOR gates is complete, any combinational logic function can be realized with the NOR circuit structures considered thus far.

Many logic functions are realized with “Static CMOS Logic” and this is probably the dominant design style used today!
Example:

How many transistors are required to realize the function

\[ F = A \cdot \overline{B} + \overline{A} \cdot C \]

in a basic CMOS process if static NAND and NOR gates are used? Assume A, B and C are available.
Example 1:

How many transistors are required to realize the function

\[ F = \overline{A \cdot B} + \overline{A \cdot C} \]

in a basic CMOS process if static NAND and NOR gates are used? Assume A, B and C are available.

Solution:

20 transistors and 5 levels of logic
Example 1:

How many transistors are required to realize the function

$$F = A \cdot B + \overline{A} \cdot C$$

in a basic CMOS process if static NAND and NOR gates are used? Assume A, B and C are available.

Solution (alternative):

From basic Boolean Manipulations

$$F = \overline{A} + \overline{B} + \overline{A} \cdot C = \overline{A} + B + \overline{A} \cdot C$$

$$F = \overline{A} \cdot (1+C) + B = \overline{A} + B$$

8 transistors and 3 levels of logic
Example 1:

How many transistors are required to realize the function

\[ F = \overline{A} \cdot B + \overline{A} \cdot C \]

in a basic CMOS process if static NAND and NOR gates are used? Assume A, B and C are available.

Solution (alternative):

From basic Boolean Manipulations

\[ F = \overline{A} \cdot (1 + C) + B = \overline{A} + B \]

\[ F = A + B = A \cdot \overline{B} \]

6 transistors and 2 levels of logic
Example 2

\[ Y = (A \cdot B) + (C \cdot D) \]

Standard Static CMOS Implementation

3 levels of Logic

16 Transistors if Basic CMOS Gates are Used