EE 330
Lecture 4

Statistical Concepts
Historical Background, Feature Sizes and Yield
Digital Systems – A preview
The defect density is often considered as proprietary information. Assume, however, that a process engineer had a lapse of thought and disclosed that they were obtaining a 95% hard yield on a circuit. The competitor bought the circuit and measured the die and found the area to be $0.2\text{cm}^2$. What was the defect density in the process?
And the number is ....
And the number is ....
Quiz 3

The defect density is often considered as proprietary information. Assume, however, that a process engineer had a lapse of thought and disclosed that they were obtaining a 95% hard yield on a circuit. The competitor bought the circuit and measured the die and found the area to be 0.2cm$^2$. What was the defect density in the process?

Solution:

\[
Y = e^{-Ad}
\]

\[
d = -\frac{\ln Y}{A} = -\frac{\ln 0.95}{0.2} = 0.26/\text{cm}^2
\]
Review from Last Time

- Sophisticated Integrated CAD Toolsets are extensively used in the industry to design integrated circuits
  - Minimize the chances of an error
  - Real asset to (and not a competitor of) the engineer
  - Critical to pay attention to what tools tell you
- Feature size good metric for characterizing capabilities of a process
  - State of the art at about 65nm
  - Pitch sometimes used instead of feature size
  - Drawn and actual features may differ
  - Bragging rights focus on actual rather than drawn features
- Yield often determined by statistically independent events

\[ Y = P^n \]

- Cost of Wafers in $800 to $3000 range depending on size and process

\[ C_{per \text{ unit area}} \approx \$2.5/cm^2 \]
Review from Last Time

MOS Transistor

Effective Width and Length Generally Smaller than Drawn Width and Length
Physical size of atoms and molecules place fundamental limit on conventional scaling approaches
Defects in a Wafer

- Dust particles and other undesirable processes cause defects
- Defects in manufacturing cause yield loss
Hard Fault Model

\[ Y_H = e^{-Ad} \]

\( Y_H \) is the probability that the die does not have a hard fault
A is the die area
d is the defect density (typically \( 1 \text{cm}^{-2} < d < 2 \text{cm}^{-2} \))

Industry often closely guards the value of d for their process

Other models, which may be better, have the same general functional form
Soft Fault Model

Soft fault models often dependent upon design and application

Often the standard deviation of a parameter is dependent upon the reciprocal of the square root of the parameter sensitive area

\[ \sigma = \frac{\rho}{\sqrt{A_k}} \]

\( \rho \) is a constant dependent upon the architecture and the process

\( A_k \) is the area of the parameter sensitive area
Soft Fault Model

\[ P_{SOFT} = \int_{X_{MIN}}^{X_{MAX}} f(x) \, dx \]

- \( P_{SOFT} \) is the soft fault yield
- \( f(x) \) is the probability density function of the parameter of interest
- \( X_{MIN} \) and \( X_{MAX} \) define the acceptable range of the parameter of interest

Some circuits may have several parameters that must meet performance requirements.
Overall Yield

If both hard and soft faults affect the yield of a circuit, the overall yield is given by the expression

\[ Y = Y_H Y_S \]
Cost Per Good Die

The manufacturing costs per good die is given by

\[ C_{\text{Good}} = \frac{C_{\text{FabDie}}}{Y} \]

where \( C_{\text{FabDie}} \) is the manufacturing costs of a fab die and \( Y \) is the yield.

There are other costs that must ultimately be included such as testing costs, engineering costs, etc.
Review from Last Time

Statistics are Real!

Statistics govern what really happens throughout much of the engineering field!

Statistics are your Friend  !!!!

You might as well know what will happen since statistics characterize what WILL happen in many processes!
Statistics can be abused!

Many that are not knowledgeable incorrectly use statistics

Many use statistics to intentionally mislead the public

Some openly abuse statistics for financial gain or for manipulation purposes

Keep an open mind to separate “good” statistics from “abused” statistics
Meeting the Real Six-Sigma Challenge

Six-Sigma or Else !!

Highly Statistical Concept !
So you've heard of Six Sigma training and always wondered what all the fuss was about. Bottom line... it is a business process that allows companies to drastically improve their profitability. How does it manage to achieve this? Well the concept is simple.

Your Company + Better Processes = $$$$
<table>
<thead>
<tr>
<th>Sigma Level</th>
<th>Defects Per Million Opportunities (DPMO)</th>
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</thead>
<tbody>
<tr>
<td>1</td>
<td>690,000</td>
</tr>
<tr>
<td>2</td>
<td>308,537</td>
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<tr>
<td>3</td>
<td>66,807</td>
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<td>4</td>
<td>6,210</td>
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<td>5</td>
<td>233</td>
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<tr>
<td>6</td>
<td>3.4</td>
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</tbody>
</table>

What Would This Look Like In The Real World?

It's one thing to see the numbers and it's a whole other thing to see how it would apply to your daily life.

<table>
<thead>
<tr>
<th>Real-world Performance Levels</th>
<th>In 1 Sigma World</th>
<th>In 3 Sigma World</th>
<th>In 6 Sigma World</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pieces of your mail lost per year [1,600 opportunities per year]</td>
<td>1,106</td>
<td>107</td>
<td>Less than 1</td>
</tr>
<tr>
<td>Number of empty coffee pots at work (who didn't fill the coffee pot again?) [680 opportunities per year]</td>
<td>470</td>
<td>45</td>
<td>Less than 1</td>
</tr>
<tr>
<td>Number of telephone disconnections [7,000 talk minutes]</td>
<td>4,839</td>
<td>467</td>
<td>0.02</td>
</tr>
<tr>
<td>Erroneous business orders [250,000 opportunities per year]</td>
<td>172,924</td>
<td>16,694</td>
<td>0.9</td>
</tr>
</tbody>
</table>
Assume $x$ is a random variable of interest

$f(x) = \text{Probability Density Function for } x$

$$\int_{-\infty}^{\infty} f(x) \, dx = 1$$

$F(x) = \text{Cumulative Density Function for } x$

$$F(X_1) = \int_{-\infty}^{X_1} f(x) \, dx$$

$0 \leq F(x) \leq 1$  \quad \frac{\partial F(x)}{\partial x} \geq 0$
Statistics Review

$f(x) = \text{Probability Density Function for } x$

$F(x) = \text{Cumulative Density Function for } x$

$$P\{x \leq X_1\} = \int_{-\infty}^{X_1} f(x) \, dx$$

$$P\{x \leq X_1\} = F(X_1)$$
Statistics Review

\[ f(x) = \text{Probability Density Function for } x \]

\[ F(x) = \text{Cumulative Density Function for } x \]

\[ P\{X_1 \leq x \leq X_2\} = \int_{X_1}^{X_2} f(x) \, dx \]

\[ P\{X_1 \leq x \leq X_2\} = F(X_2) - F(X_1) \]
If the random variable $x$ in Normally distributed with mean $\mu$ and standard deviation $\sigma$, then $y = \frac{x - \mu}{\sigma}$ is also a random variable that is Normally distributed with mean 0 and standard deviation of 1.
The random part of many parameters of microelectronic circuits is often assumed to be Normally distributed and experimental observations confirm that this assumption provides close agreement between theoretical and experimental results.

The mapping \[ y = \frac{x - \mu}{\sigma} \] is often used to simplify the statistical characterization of the random parameters in microelectronic circuits.
One-Sided or Two-Sided Capabilities

Single-Sided Capabilities

Two-Sided Capabilities
One-Sided or Two-Sided Capabilities

Single-Sided Capability Example

Clock speed of a microprocessor exceeding a specification of 3.5GHz

Two-Sided Capability Example

Offset voltage magnitude is less than a specified value of 3 mV
The Six-Sigma Challenge

Assumption (empirical) : The long-term capability of a process will degrade by 1.5 sigma from the short-term capability of the process

Assumption : Processes of interest are Gaussian (Normal)

Observation: Any Normally distributed random variable can be mapped to a $N(0,1)$ random variable by subtracting the mean and dividing by the variance
The Six-Sigma Challenge

Single-sided capability:

Long-term Capability

Tail is 3.4 parts in a million

Short-term Capability

Tail is 1 part in a billion
The Six-Sigma Challenge

Two-sided capability:

Long-term Capability
Tails are 6.8 parts in a million

Short-term Capability
Tail is 2 parts in a billion

Six Sigma Performance is Very Good !!!
Example: Determine the maximum die area if the circuit yield is to meet the short-term “six sigma” challenge (Assume a defect density of 1 cm$^{-2}$ and only hard yield loss). Is it realistic to set six-sigma die yield expectations on the design and process engineers?

Solution:

The short-term “six-sigma” challenge requires meeting a 6 standard deviation yield with a Normal (0,1) distribution. The expression for the yield is given by:

$$Y_{6\text{sigma}} = 2F_N(6) - 1$$
<table>
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<tr>
<th>No Sigma</th>
<th>Yield</th>
<th>Defect Rate</th>
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<tr>
<td>1</td>
<td>0.682689492</td>
<td>0.317311</td>
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<td>0.954499736</td>
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<td>3</td>
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</tr>
<tr>
<td>6</td>
<td><strong>0.999999980</strong></td>
<td><strong>1.97E-09</strong></td>
</tr>
<tr>
<td>7</td>
<td>0.9999999974</td>
<td>2.56E-12</td>
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Solution cont:

Six-sigma performance is approximately 2 defects in a billion!
Solution cont:

\[ Y_H = e^{-Ad} \]

\[ A = \frac{-\ln(Y_H)}{d} \]

\[ A = \frac{-\ln(0.9999999980)}{1 \text{cm}^{-2}} = 2.0 \times 10^{-9} \text{cm}^2 = 2.5 \times 10^5 (\text{Å})^2 \]

This is orders of magnitude less than the area needed to fabricate even a single transistor.
Solution cont:

Is it realistic to set six-sigma die yield expectations on the design and process engineers?

The best technologies in the world have orders of magnitude too many defects to build any useful integrated circuits with die yields that meet six-sigma performance requirements!!
Is it realistic to set six-sigma feature yield expectations on individual features in a process?
Is it realistic to set six-sigma feature yield expectations on individual features in a process?

Assume an overall yield for 400 Million transistors of 90%

Assume 10 features for each transistor

Total number of features is 4E9

Let $p$ be the probability that a feature is good and assume the random part of each feature is uncorrelated from that of other features

$$Y = p^n$$

$$p = e^{\left(\frac{\ln Y}{n}\right)}$$
Is it realistic to set six-sigma feature yield expectations on individual features in a process?

\[ p = e^{\frac{\ln Y}{n}} \]

\[ Y = 0.9 \]
\[ N = 4 \times 10^9 \]

Solving, obtain \( p = 0.999999999974 \)

Defect rate of \( 1 - p = 2.6 \times 10^{-11} \)

0.026 in a billion

Note this is much more stringent than the 1.97 parts in a billion corresponding to 6 sigma performance!
Is it realistic to set six-sigma feature yield expectations on individual features in a process?

Six-sigma feature yield is too low to expect acceptable die yield!

- Six-sigma yield expectations can be way too stringent or way too lax depending upon what step is being considered in the manufacturing process!!

- Arbitrarily establishing six-sigma expectations on all steps in a process will guarantee financial disaster!!

- Yield expectations should be established based upon solid mathematical formulations relating the overall manufacturing costs to the market potential of a product
Six-sigma capability has almost nothing to do with optimizing profits and, if taken seriously, will likely guarantee a financial fiasco in most manufacturing processes.
Meeting the Real Six-Sigma Challenge

Six-Sigma or Else !!

YOU’RE FIRED!
Meeting the real Six-Sigma Challenge

Six-Sigma or Else !!
Meeting the real Six-Sigma Challenge

The concept of improving reliability (really profitability) is good – its just the statistics that are abused!
Meeting the real Six-Sigma Challenge

I got the message

Six-Sigma or Else!!
Key Historical Developments

• 1925, 1935  Concept of MOS Transistor Proposed (Lilienfield and Heil)

• 1947  BJT Conceived and Experimentally Verified (Bardeen, Bratin and Shockley of Bell Labs)

• 1959  Jack Kilby (TI) and Bob Noyce (Fairchild) invent IC

• 1963  Wanless (Fairchild) Experimentally verifies MOS Gate
1926 - Field Effect Semiconductor Device Concepts Patented

Julius Lilienfeld files a patent describing a three-electrode amplifying device based on the semiconducting properties of copper sulfide. Attempts to build such a device continue through the 1930s.

Polish-American physicist and inventor Julius E. Lilienfeld filed a patent in 1926, "Method and Apparatus for Controlling Electric Currents," in which he proposed a three-electrode structure using copper-sulfide semiconductor material. Today this device would be called a field-effect transistor. While working at Cambridge University in 1934, German electrical engineer and inventor Oskar Heil filed a patent on controlling current flow in a semiconductor via capacitive coupling at an electrode – essentially a field-effect transistor. Although both patents were granted, no records exist to prove that Heil or Lilienfeld actually constructed functioning devices.

Heil, O. "Improvements in or relating to electrical amplifiers and other control arrangements and devices," British Patent No. 439, 457 (Filed March 5, 1935. Issued December 6, 1935).

http://www.computerhistory.org/semiconductor/timeline/1926-field.html
JULIUS EDGAR LILIENTHAL, OF BROOKLYN, NEW YORK

METHOD AND APPARATUS FOR CONTROLLING ELECTRIC CURRENTS

Application filed October 8, 1926, Serial No. 140,963, and in Canada October 22, 1925.

J. E. LILIENTHAL

METHOD AND APPARATUS FOR CONTROLLING ELECTRIC CURRENTS

Filed Oct. 8, 1926
J. E. LILIENFELD

DEVICE FOR CONTROLLING ELECTRIC CURRENT

Filed March 28, 1928

1,900,018

3 Sheets-Sheet 1
Naming the Transistor

From the group at Bell Labs

“We have called it the transistor, T-R-A-N-S-I-S-T-O-R, because it is resistor or semiconductor device which can amplify electrical signals as they are transferred through it from input to output terminals. It is, if you will, the electrical equivalent of a vacuum tube amplifier. But there the similarity ceases. It has no vacuum, no filament, no glass tube. It is composed entirely of cold, solid substances.”
William Shockley

http://www.time.com/time/time100/scientist/profile/shockley03.html
William Shockley
He fathered the transistor and brought the silicon to Silicon Valley but is remembered by many only for his noxious racial views
By GORDON MOORE

The transistor was born just before Christmas 1947 when John Bardeen and Walter Brattain, two scientists working for William Shockley at Bell Telephone Laboratories in Murray Hill, N.J., observed that when electrical signals were applied to contacts on a crystal of germanium, the output power was larger than the input. Shockley was not present at that first observation. And though he fathered the discovery in the same way Einstein fathered the atom bomb, by advancing the idea and pointing the way, he felt left out of the momentous occasion.

Shockley, a very competitive and sometimes infuriating man, was determined to make his imprint on the discovery. He searched for an explanation of the effect from what was then known of the quantum physics of semiconductors. In a remarkable series of insights made over a few short weeks, he greatly extended the understanding of semiconductor materials and developed the underlying theory of another, much more robust amplifying device — a kind of sandwich made of a crystal with varying impurities added, which came to be known as the junction transistor. By 1951 Shockley's co-workers made his semiconductor sandwich and demonstrated that it behaved much as his theory had predicted.
Not content with his lot at Bell Labs, Shockley set out to capitalize on his invention. In doing so, he played a key role in the industrial development of the region at the base of the San Francisco Peninsula. It was Shockley who brought the silicon to Silicon Valley.

In February 1956, with financing from Beckman Instruments Inc., he founded Shockley Semiconductor Laboratory with the goal of developing and producing a silicon transistor. He chose to establish this start-up near Palo Alto, where he had grown up and where his mother still lived. He set up operations in a storefront — little more than a Quonset hut — and hired a group of young scientists (I was one of them) to develop the necessary technology. By the spring of 1956 he had a small staff in place and was beginning to undertake research and development.

This new company, financed by Fairchild Camera & Instrument Corp., became the mother organization for several dozen new companies in Silicon Valley. Nearly all the scores of companies that are or have been active in semiconductor technology can trace the technical lineage of their founders back through Fairchild to the Shockley Semiconductor Laboratory. Unintentionally, Shockley contributed to one of the most spectacular and successful industry expansions in history.

*Editor's note:*

In 1963 Shockley left the electronics industry and accepted an appointment at Stanford. There he became interested in the origins of human intelligence. Although he had no formal training in genetics or psychology, he began to formulate a theory of what he called dysgenics. Using data from the U.S. Army's crude pre-induction IQ tests, he concluded that African Americans were inherently less intelligent than Caucasians — an analysis that stirred wide controversy among laymen and experts in the field alike.
SEMICONDUCTOR DEVICE

Peterson and Stevenson, Davis, Miller and Mosher

EXEMPLARY CLAIM

1. A semiconductor device comprising:
a. a wafer of semiconductor material having two major faces;
b. said wafer being so shaped as to define a plurality of regions within said wafer and adjacent to one of said major faces;
c. at least some of said regions being electrically insulated within said wafer from others of said regions;
d. said regions having at least one portion thereof extending to said one major face;
e. at least some of said portions having selected locations on said one major face for electrical contact to said region;
f. an insulating material on said one major face of the wafer excluding at least said selected locations;
g. at least one electrically conductive area in contact with said insulating material and spaced from said wafer thereby;
h. said electrically conductive area being disposed in cooperative relationship with respect to a selected one of said isolated regions so as to provide the electrical function of a discrete electrical circuit component and
   i. a plurality of metallic interconnections providing electrically conductive paths between said selected locations on different ones of said regions and between another selected one of said locations and said electrically conductive area.

4 Claims, 33 Drawing Figures
There are few men whose insights and professional accomplishments have changed the world. Jack Kilby is one of these men. His invention of the monolithic integrated circuit - the microchip - some 45 years ago at Texas Instruments (TI) laid the conceptual and technical foundation for the entire field of modern microelectronics. It was this breakthrough that made possible the sophisticated high-speed computers and large-capacity semiconductor memories of today's information age.

Mr. Kilby grew up in Great Bend, Kansas. With B.S. and M.S. degrees in electrical engineering from the Universities of Illinois and Wisconsin respectively, he began his career in 1947 with the Centralab Division of Globe Union Inc. in Milwaukee, developing ceramic-base, silk-screen circuits for consumer electronic products.

In 1958, he joined TI in Dallas. During the summer of that year working with borrowed and improvised equipment, he conceived and built the first electronic circuit in which all of the components, both active and passive, were fabricated in a single piece of semiconductor material half the size of a paper clip. The successful laboratory demonstration of that first simple microchip on September 12, 1958, made history.

Jack Kilby went on to pioneer military, industrial, and commercial applications of microchip technology. He headed teams that built both the first military system and the first computer incorporating integrated circuits. He later co-invented both the hand-held calculator and the thermal printer that was used in portable data terminals.
Robert Norton Noyce was born December 12, 1927 in Burlington, Iowa. A noted visionary and natural leader, Robert Noyce helped to create a new industry when he developed the technology that would eventually become the microchip. Noted as one of the original computer entrepreneurs, he founded two companies that would largely shape today's computer industry—Fairchild Semiconductor and Intel.

Bob Noyce's nickname was the "Mayor of Silicon Valley." He was one of the very first scientists to work in the area -- long before the stretch of California had earned the Silicon name -- and he ran two of the companies that had the greatest impact on the silicon industry: Fairchild Semiconductor and Intel. He also invented the integrated chip, one of the stepping stones along the way to the microprocessors in today's computers.

Noyce, the son of a preacher, grew up in Grinnell, Iowa. He was a physics major at Grinnell College, and exhibited while there an almost baffling amount of confidence. He was always the leader of the crowd. This could turn against him occasionally -- the local farmers didn't approve of him and weren't likely to forgive quickly when he did something like steal a pig for a college luau. The prank nearly got Noyce expelled, even though the only reason the farmer knew about it was because Noyce had confessed and offered to pay for it.
While in college, Noyce's physics professor Grant Gale got hold of two of the very first transistors ever to come out of Bell Labs. Gale showed them off to his class and Noyce was hooked. The field was young, though, so when Noyce went to MIT in 1948 for his Ph.D., he found he knew more about transistors than many of his professors.

After a brief stint making transistors for the electronics firm Philco, Noyce decided he wanted to work at Shockley Semiconductor. In a single day, he flew with his wife and two kids to California, bought a house, and went to visit Shockley to ask for a job -- in that order.

As it was, Shockley and Noyce's scientific vision -- and egos -- clashed. When seven of the young researchers at Shockley semiconductor got together to consider leaving the company, they realized they needed a leader. All seven thought Noyce, aged 29 but full of confidence, was the natural choice. So Noyce became the eighth in the group that left Shockley in 1957 and founded Fairchild Semiconductor.

Noyce was the general manager of the company and while there invented the integrated chip -- a chip of silicon with many transistors all etched into it at once. Fairchild Semiconductor filed a patent for a semiconductor integrated circuit based on the planar process on July 30, 1959. That was the first time he revolutionized the semiconductor industry. He stayed with Fairchild until 1968, when he left with Gordon Moore to found Intel.
At Intel he oversaw Ted Hoff's invention of the microprocessor -- that was his second revolution.

At both companies, Noyce introduced a very casual working atmosphere, the kind of atmosphere that has become a cultural stereotype of how California companies work. But along with that open atmosphere came responsibility. Noyce learned from Shockley's mistakes and he gave his young, bright employees phenomenal room to accomplish what they wished, in many ways defining the Silicon Valley working style was his third revolution.
Key Historical Developments

• 1971 Intel Introduces 4004 microprocessor (2300 transistors, 10u process)
Silicon Gate MOS 4004

SINGLE CHIP 4-BIT P-CHANNEL MICROPROCESSOR

- 10.8 Microsecond Instruction Cycle
- CPU Directly Compatible With MCS-4 ROMs and RAMs
- Easy Expansion—One CPU can Directly Drive up to 32,768 Bits of ROM and up to 5120 Bits of RAM
- 4-Bit Parallel CPU With 46 Instructions
- Instruction Set Includes Conditional Branching, Jump to Subroutine and Indirect Fetching
- Binary and Decimal Arithmetic Modes

The Intel 4004 is a complete 4-bit parallel central processing unit (CPU). It is designed to be used in test systems, terminals, billing machines, process control and random logic replacement applications. The 4004 easily interfaces with keyboards, switches, displays, A/D converters, printers and other peripheral equipment.

The CPU can directly address 4K 8-bit instruction words of program memory and 5120 bits of data storage RAM. Sixteen index registers are provided for temporary data storage. Up to 16 4-bit input ports and 16 4-bit output ports may also be directly addressed.

The 4004 is fabricated with P-channel silicon gate MOS technology.
Basic Logic Circuits
Basic Logic Circuits

- Will present a brief description of logic circuits based upon simple models and qualitative description of processes
- Will discuss process technology needed to develop better models
- Will provide more in-depth discussion of logic circuits based upon better device models
Models of Devices

• Several models of the electronic devices will be introduced
  – Complexity
  – Accuracy
  – Insight
  – Application

• Will use the simplest model that can provide acceptable results for any given application
MOS Transistor
Qualitative Discussion of n-channel Operation

Designer always works with top view
Complete Symmetry in construction between Drain and Source
MOS Transistor
Qualitative Discussion of n-channel Operation

Behavioral Description of Basic Operation

If $V_{GS}$ is large, short circuit exists between drain and source

If $V_{GS}$ is small, open circuit exists between drain and source
MOS Transistor
Qualitative Discussion of n-channel Operation

Equivalent Circuit for n-channel MOSFET

This is the first model we have for the n-channel MOSFET!
MOS Transistor MODEL

Equivalent Circuit for n-channel MOSFET

Mathematically:

\[ I_D = 0 \quad \text{if} \quad V_{GS} \quad \text{is low} \]
\[ V_{DS} = 0 \quad \text{if} \quad V_{GS} \quad \text{is high} \]
MOS Transistor
Qualitative Discussion of p-channel Operation

Complete Symmetry in construction between Drain and Source
MOS Transistor
Qualitative Discussion of p-channel Operation

Behavioral Description of Basic Operation

If $V_{GS}$ is small (negative), short circuit exists between drain and source

If $V_{GS}$ is large (near 0), open circuit exists between drain and source
MOS Transistor
Qualitative Discussion of p-channel Operation

This is the first model we have for the p-channel MOSFET!
MOS Transistor MODEL

Mathematically:

\[ I_D = 0 \quad \text{if } V_{GS} \text{ is high} \]
\[ V_{DS} = 0 \quad \text{if } V_{GS} \text{ is low} \]
MOS Transistor
Comparison of Operation
A model for the n-channel and p-channel transistor has been developed

- *Termed the ideal switch-level model*
- *Several other models will be developed later*
- *Invariably use simplest model that is justifiable*
- *Will introduce better models only when needed*

Symbols have been introduced for the two basic transistors

- *Other symbols will be introduced later*
Logic Circuits

Circuit Behaves as a Boolean Inverter
Logic Circuits

Inverter

Truth Table

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Logic Circuits

\[ A = 0 \]
\[ B = 0 \]

\[ V_{DD} = 1 \]

\[ A = 0 \]
\[ B = 0 \]

\[ C = 1 \]
Logic Circuits

A = 1
B = 0
C = 0

A
B
C
V_{DD}
Logic Circuits

A = 0
B = 1
C = 0
Logic Circuits

A = 1
B = 1

A = 1
B = 1
C = 0
Logic Circuits

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Logic Circuits

Truth Table

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End of Lecture 4