Historical Background
Digital Systems – A preview
Review from Last Time

Defects in a Wafer

- Dust particles and other undesirable processes cause defects
- Defects in manufacturing cause yield loss
Review from Last Time

Hard Fault Model

\[ Y_H = e^{-Ad} \]

\( Y_H \) is the probability that the die does not have a hard fault
\( A \) is the die area
\( d \) is the defect density (typically \( 1 \text{cm}^{-2} < d < 2 \text{cm}^{-2} \))

Industry often closely guards the value of \( d \) for their process

Other models, which may be better, have the same general functional form
Soft Fault Model

Soft fault models often dependent upon design and application

Often the standard deviation of a parameter is dependent upon the reciprocal of the square root of the parameter sensitive area.

\[ \sigma = \frac{\rho}{\sqrt{A_k}} \]

\( \rho \) is a constant dependent upon the architecture and the process.

\( A_k \) is the area of the parameter sensitive area.
Soft Fault Model

\[ P_{\text{SOFT}} = \int_{X_{\text{MIN}}}^{X_{\text{MAX}}} f(x) \, dx \]

- \( P_{\text{SOFT}} \) is the soft fault yield
- \( f(x) \) is the probability density function of the parameter of interest
- \( X_{\text{MIN}} \) and \( X_{\text{MAX}} \) define the acceptable range of the parameter of interest

Some circuits may have several parameters that must meet performance requirements.
Overall Yield

If both hard and soft faults affect the yield of a circuit, the overall yield is given by the expression

\[ Y = Y_H Y_S \]
Cost Per Good Die

The manufacturing costs per good die is given by

\[
C_{\text{Good}} = \frac{C_{\text{FabDie}}}{Y}
\]

where \(C_{\text{FabDie}}\) is the manufacturing costs of a fab die and \(Y\) is the yield.

There are other costs that must ultimately be included such as testing costs, engineering costs, etc.
Theorem 1: If the random variable $x$ is normally distributed with mean $\mu$ and standard deviation $\sigma$, then $y = \frac{x - \mu}{\sigma}$ is also a random variable that is normally distributed with mean 0 and standard deviation of 1.

(Normal Distribution and Gaussian Distribution are the same)
Background Information

Tables of the CDF of the $N(0,1)$ random variable are readily available. It is also available in Matlab, Excel, and a host of other sources.

Review from Last Time

![Probability Content from $-\infty$ to $Z$](http://www.math.unb.ca/~knight/utility/NormTble.htm)
Statistics are Real!

Statistics govern what really happens throughout much of the engineering field!

Statistics are your Friend  !!!!

You might as well know what will happen since statistics characterize what WILL happen in many processes !
Meeting the Real Six-Sigma Challenge

Introduced by Bill Smith of Motorola in 1984
2/3 of Fortune 500 Companies adopted/adopting 6-sigma concepts
Review from Last Time

Meeting the Real Six-Sigma Challenge

How has Motorola fared with the 6-sigma approach?

- Sold military activities to General Dynamics 2000/2001
- Sold automotive products in 2006
- Spun off discrete components as ON semiconductor in 1999
- Spun off SPS as Freescale in 2003
- Sold Motorola Mobility to Google in 2011
Statistics can be abused!

Many that are not knowledgeable incorrectly use statistics

Many use statistics to intentionally mislead the public

Some openly abuse statistics for financial gain or for manipulation purposes

Keep an open mind to separate “good” statistics from “abused” statistics
Key Historical Developments

• 1925, 1935 Concept of MOS Transistor Proposed (Lilienfield and Heil)

• 1947 BJT Conceived and Experimentally Verified (Bardeen, Bratin and Shockley of Bell Labs)

• 1959 Jack Kilby (TI) and Bob Noyce (Fairchild) invent IC

• 1963 Wanless (Fairchild) Experimentally verifies MOS Gate
1926 - Field Effect Semiconductor Device Concepts Patented

Julius Lilienfeld files a patent describing a three-electrode amplifying device based on the semiconducting properties of copper sulfide. Attempts to build such a device continue through the 1930s.

Polish-American physicist and inventor Julius E. Lilienfeld filed a patent in 1926, "Method and Apparatus for Controlling Electric Currents," in which he proposed a three-electrode structure using copper-sulfide semiconductor material. Today this device would be called a field-effect transistor. While working at Cambridge University in 1934, German electrical engineer and inventor Oskar Heil filed a patent on controlling current flow in a semiconductor via capacitive coupling at an electrode - essentially a field-effect transistor. Although both patents were granted, no records exist to prove that Heil or Lilienfeld actually constructed functioning devices.

Heil, O. "Improvements in or relating to electrical amplifiers and other control arrangements and devices," British Patent No. 439, 457 (Filed March 5, 1935. Issued December 6, 1935).
JULIUS EDGAR LILIJENFELD, OF BROOKLYN, NEW YORK

METHOD AND APPARATUS FOR CONTROLLING ELECTRIC CURRENTS

Application filed October 8, 1926, Serial No. 140,363, and in Canada October 28, 1925.

Jan. 28, 1930.

J. E. LILIJENFELD

METHOD AND APPARATUS FOR CONTROLLING ELECTRIC CURRENTS

Filed Oct. 8, 1926

Fig. 1.
FIG. 1.

16  14  13  15  17

12 Copper Sulfide
11 Aluminum Oxide
10 Aluminum

20

FIG. 2.

26  25

12 Copper Sulfide
11 Aluminum Oxide
10 Aluminum

March 7, 1933.
J. E. LILIENTHIELD

DEVICE FOR CONTROLLING ELECTRIC CURRENT

Filed March 28, 1928
3 Sheets-Sheet 1
Naming the Transistor

From the group at Bell Labs

“We have called it the transistor, T-R-A-N-S-I-S-T-O-R, because it is resistor or semiconductor device which can amplify electrical signals as they are transferred through it from input to output terminals. It is, if you will, the electrical equivalent of a vacuum tube amplifier. But there the similarity ceases. It has no vacuum, no filament, no glass tube. It is composed entirely of cold, solid substances.”
William Shockley
He fathered the transistor and brought the silicon to Silicon Valley but is remembered by many only for his noxious racial views
By GORDON MOORE

The transistor was born just before Christmas 1947 when John Bardeen and Walter Brattain, two scientists working for William Shockley at Bell Telephone Laboratories in Murray Hill, N.J., observed that when electrical signals were applied to contacts on a crystal of germanium, the output power was larger than the input. Shockley was not present at that first observation. And though he fathered the discovery in the same way Einstein fathered the atom bomb, by advancing the idea and pointing the way, he felt left out of the momentous occasion.

Shockley, a very competitive and sometimes infuriating man, was determined to make his imprint on the discovery. He searched for an explanation of the effect from what was then known of the quantum physics of semiconductors. In a remarkable series of insights made over a few short weeks, he greatly extended the understanding of semiconductor materials and developed the underlying theory of another, much more robust amplifying device — a kind of sandwich made of a crystal with varying impurities added, which came to be known as the junction transistor. By 1951 Shockley's co-workers made his semiconductor sandwich and demonstrated that it behaved much as his theory had predicted.
Not content with his lot at Bell Labs, Shockley set out to capitalize on his invention. In doing so, he played a key role in the industrial development of the region at the base of the San Francisco Peninsula. It was Shockley who brought the silicon to Silicon Valley.

In February 1956, with financing from Beckman Instruments Inc., he founded Shockley Semiconductor Laboratory with the goal of developing and producing a silicon transistor. He chose to establish this start-up near Palo Alto, where he had grown up and where his mother still lived. He set up operations in a storefront — little more than a Quonset hut — and hired a group of young scientists (I was one of them) to develop the necessary technology. By the spring of 1956 he had a small staff in place and was beginning to undertake research and development.

This new company, financed by Fairchild Camera & Instrument Corp., became the mother organization for several dozen new companies in Silicon Valley. Nearly all the scores of companies that are or have been active in semiconductor technology can trace the technical lineage of their founders back through Fairchild to the Shockley Semiconductor Laboratory. Unintentionally, Shockley contributed to one of the most spectacular and successful industry expansions in history.

*Editor's note:*

In 1963 Shockley left the electronics industry and accepted an appointment at Stanford. There he became interested in the origins of human intelligence. Although he had no formal training in genetics or psychology, he began to formulate a theory of what he called dysgenics. Using data from the U.S. Army's crude pre-induction IQ tests, he concluded that African Americans were inherently less intelligent than Caucasians — an analysis that stirred wide controversy among laymen and experts in the field alike.

(Fairchild was formed in 1957 – Moore and Noyce were 2 or 8 co-founders)
SEMICONDUCTOR DEVICE

Inventor: Jack St Clair Kilby, Dallas, Tex.

Assignee: Texas Instruments Incorporated, Dallas, Tex.

Filed: Jun. 29, 1962

Appl. No.: 169,557

Related U.S. Application Data


U.S. Cl. 317/233, 317/234, 317/1101

Int. Cl. H01L 19/00

Field of Search 317/234, 235, 101, 231

References Cited

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2,796,562 6/1957 Elgin et al. 317/234
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2,910,634 10/1959 Bunt 317/235
3,038,085 6/1962 Wallmark et al. 307/88.5

Primary Examiner—James D. Kallam

Attorneys—James O. Dicken, Andrew M. Hassell, Robert C.

EXEMPLARY CLAIM

1. A semiconductor device comprising:
   a. a wafer of semiconductor material having two major faces;
   b. said wafer being so shaped as to define a plurality of regions within said wafer and adjacent to one of said major faces;
   c. at least some of said regions being electrically isolated within said wafer from others of said regions;
   d. said regions having at least one portion thereof extending to said one major face;
   e. at least some of said portions having selected locations on said one major face for electrical contact to said region;
   f. an insulating material on said one major face of the wafer excluding at least said selected locations;
   g. at least one electrically conductive area in contact with said insulating material and spaced from said wafer thereby;
   h. said electrically conductive area being disposed in cooperative relationship with respect to a selected one of said isolated regions so as to provide the electrical function of a discrete electrical circuit component; and
   i. a plurality of metallic interconnections providing electrically conductive paths between said selected locations on different ones of said regions and between another selected one of said locations and said electrically conductive area.

4 Claims, 33 Drawing Figures
There are few men whose insights and professional accomplishments have changed the world. Jack Kilby is one of these men. His invention of the monolithic integrated circuit - the microchip - some 45 years ago at Texas Instruments (TI) laid the conceptual and technical foundation for the entire field of modern microelectronics. It was this breakthrough that made possible the sophisticated high-speed computers and large-capacity semiconductor memories of today's information age.

Mr. Kilby grew up in Great Bend, Kansas. With B.S. and M.S. degrees in electrical engineering from the Universities of Illinois and Wisconsin respectively, he began his career in 1947 with the Centralab Division of Globe Union Inc. in Milwaukee, developing ceramic-base, silk-screen circuits for consumer electronic products.

In 1958, he joined TI in Dallas. During the summer of that year working with borrowed and improvised equipment, he conceived and built the first electronic circuit in which all of the components, both active and passive, were fabricated in a single piece of semiconductor material half the size of a paper clip. The successful laboratory demonstration of that first simple microchip on September 12, 1958, made history.

Jack Kilby went on to pioneer military, industrial, and commercial applications of microchip technology. He headed teams that built both the first military system and the first computer incorporating integrated circuits. He later co-invented both the hand-held calculator and the thermal printer that was used in portable data terminals.
Robert Norton Noyce was born December 12, 1927 in Burlington, Iowa. A noted visionary and natural leader, Robert Noyce helped to create a new industry when he developed the technology that would eventually become the microchip. Noted as one of the original computer entrepreneurs, he founded two companies that would largely shape today’s computer industry—Fairchild Semiconductor and Intel.

Bob Noyce's nickname was the "Mayor of Silicon Valley." He was one of the very first scientists to work in the area -- long before the stretch of California had earned the Silicon name -- and he ran two of the companies that had the greatest impact on the silicon industry: Fairchild Semiconductor and Intel. He also invented the integrated chip, one of the stepping stones along the way to the microprocessors in today's computers.

Noyce, the son of a preacher, grew up in Grinnell, Iowa. He was a physics major at Grinnell College, and exhibited while there an almost baffling amount of confidence. He was always the leader of the crowd. This could turn against him occasionally -- the local farmers didn't approve of him and weren't likely to forgive quickly when he did something like steal a pig for a college luau. The prank nearly got Noyce expelled, even though the only reason the farmer knew about it was because Noyce had confessed and offered to pay for it.
While in college, Noyce's physics professor Grant Gale got hold of two of the very first transistors ever to come out of Bell Labs. Gale showed them off to his class and Noyce was hooked. The field was young, though, so when Noyce went to MIT in 1948 for his Ph.D., he found he knew more about transistors than many of his professors.

After a brief stint making transistors for the electronics firm Philco, Noyce decided he wanted to work at Shockley Semiconductor. In a single day, he flew with his wife and two kids to California, bought a house, and went to visit Shockley to ask for a job -- in that order.

As it was, Shockley and Noyce's scientific vision -- and egos -- clashed. When seven of the young researchers at Shockley semiconductor got together to consider leaving the company, they realized they needed a leader. All seven thought Noyce, aged 29 but full of confidence, was the natural choice. So Noyce became the eighth in the group that left Shockley in 1957 and founded Fairchild Semiconductor.

Noyce was the general manager of the company and while there invented the integrated chip -- a chip of silicon with many transistors all etched into it at once. Fairchild Semiconductor filed a patent for a semiconductor integrated circuit based on the planar process on July 30, 1959. That was the first time he revolutionized the semiconductor industry. He stayed with Fairchild until 1968, when he left with Gordon Moore to found Intel.
At Intel he oversaw Ted Hoff's invention of the microprocessor -- that was his second revolution.

At both companies, Noyce introduced a very casual working atmosphere, the kind of atmosphere that has become a cultural stereotype of how California companies work. But along with that open atmosphere came responsibility. Noyce learned from Shockley's mistakes and he gave his young, bright employees phenomenal room to accomplish what they wished, in many ways defining the Silicon Valley working style was his third revolution.
Key Historical Developments

• 1971  Intel Introduces 4004 microprocessor (2300 transistors, 10u process)
Silicon Gate MOS 4004

SINGLE CHIP 4-BIT P-CHANNEL MICROPROCESSOR

• 10.8 Microsecond Instruction Cycle
• CPU Directly Compatible With MCS-4 ROMs and RAMs
• Easy Expansion—One CPU can Directly Drive up to 32,768 Bits of ROM and up to 5120 Bits of RAM
• 4-Bit Parallel CPU With 46 Instructions
• Instruction Set Includes Conditional Branching, Jump to Subroutine and Indirect Fetching
• Binary and Decimal Arithmetic Modes

The Intel 4004 is a complete 4-bit parallel central processing unit (CPU). It is designed to be used in test systems, terminals, billing machines, process control and random logic replacement applications. The 4004 easily interfaces with keyboards, switches, displays, A-D converters, printers and other peripheral equipment.

The CPU can directly address 4K 8-bit instruction words of program memory and 6120 bits of data storage RAM. Sixteen index registers are provided for temporary data storage. Up to 16 4-bit input ports and 16 4-bit output ports may also be directly addressed.

The 4004 is fabricated with P-channel silicon gate MOS technology.
Basic Logic Circuits
Basic Logic Circuits

• Will present a brief description of logic circuits based upon simple models and qualitative description of processes
• Will discuss process technology needed to develop better models
• Will provide more in-depth discussion of logic circuits based upon better device models
Models of Devices

• Several models of the electronic devices will be introduced
  – Complexity
  – Accuracy
  – Insight
  – Application

• Will use the simplest model that can provide acceptable results for any given application
MOS Transistor
Qualitative Discussion of n-channel Operation

Designer always works with top view
Complete Symmetry in construction between Drain and Source
MOS Transistor
Qualitative Discussion of n-channel Operation

Behavioral Description of Basic Operation

If $V_{GS}$ is large, short circuit exists between drain and source

If $V_{GS}$ is small, open circuit exists between drain and source
Most logic circuits characterized by the relationship between the Boolean input/output variables though these correspond to voltage ranges on the continuous voltage axis.
MOS Transistor
Qualitative Discussion of n-channel Operation

Equivalent Circuit for n-channel MOSFET

Source assumed connected to ground

This is the first model we have for the n-channel MOSFET!
MOS Transistor MODEL

Equivalent Circuit for n-channel MOSFET

Mathematically:

\[ I_D = 0 \quad \text{if } V_{GS} \text{ is low} \]
\[ V_{DS} = 0 \quad \text{if } V_{GS} \text{ is high} \]
MOS Transistor

Qualitative Discussion of p-channel Operation

Complete Symmetry in construction between Drain and Source
Behavioral Description of Basic Operation

If $V_{GS}$ is large (negative), short circuit exists between drain and source.

If $V_{GS}$ is small (near 0), open circuit exists between drain and source.
MOS Transistor
Qualitative Discussion of p-channel Operation

This is the first model we have for the p-channel MOSFET!
MOS Transistor MODEL

Mathematically:

\[ I_D = 0 \quad \text{if } V_G \text{ is high} \quad (\left| V_{GSp} \right| \text{ is small}) \]
\[ V_{DS} = 0 \quad \text{if } V_G \text{ is low} \quad (\left| V_{GSp} \right| \text{ is large}) \]
MOS Transistor
Comparison of Operation

\[ \begin{array}{c}
D \\
S
\end{array} \]
\[ \begin{array}{c}
D \\
G = 0 \\
S
\end{array} \]

\[ \begin{array}{c}
D \\
S
\end{array} \]
\[ \begin{array}{c}
D \\
G = 1 \\
S
\end{array} \]

\[ \begin{array}{c}
D \\
S
\end{array} \]
\[ \begin{array}{c}
D \\
G = 0 \\
S
\end{array} \]

\[ \begin{array}{c}
D \\
S
\end{array} \]
\[ \begin{array}{c}
D \\
G = 1 \\
S
\end{array} \]
A model for the n-channel and p-channel transistor has been developed

- *Termed the ideal switch-level model*
- *Several other models will be developed later*
- *Invariably use simplest model that is justifiable*
- *Will introduce better models only when needed*

Symbols have been introduced for the two basic transistors

- *Other symbols will be introduced later*
Logic Circuits

Circuit Behaves as a Boolean Inverter
Logic Circuits

Inverter

Truth Table

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Logic Circuits

\[ A = 0 \]
\[ B = 0 \]
\[ C = 1 \]

\[ V_{DD} \]
Logic Circuits

A = 1
B = 0

A = 1
B = 0

C = 0
Logic Circuits

A = 0
B = 1

A = 0
B = 1

C = 0
Logic Circuits

A = 1
B = 1
C

A = 1
B = 1
C = 0

A
B
C
V_{DD}

V_{DD}

C = 0
Logic Circuits

A NOR Gate

Truth Table

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Logic Circuits

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NAND Gate
Other logic circuits

- Other methods for designing logic circuits exist.
- Insight will be provided on how other logic circuits evolve.
- Several different types of logic circuits are often used simultaneously in any circuit design.
Pull-up and Pull-down Networks

PU network comprised of p-channel device
PD network comprised of n-channel device
One and only one of these networks is conducting at the same time
Pull-up and Pull-down Networks

PU network comprised of p-channel devices
PD network comprised of n-channel devices
One and only one of these networks is conducting at the same time
Pull-up and Pull-down Networks

PU network comprised of p-channel device
PD network comprised of n-channel device
One and only one of these networks is conducting at the same time
Pull-up and Pull-down Networks

In these circuits, the PUN and PDN have the 3 interesting characteristics

1. PU network comprised of p-channel devices
2. PD network comprised of n-channel devices
3. One and only one of these networks is conducting at the same time

What are $V_H$ and $V_L$? What is the power dissipation? How fast are these logic circuits?
What are $V_H$ and $V_L$?
What is the power dissipation?
How fast are these logic circuits?

Consider the inverter

Use switch-level model for MOS devices
What are $V_H$ and $V_L$?
What is the power dissipation?
How fast are these logic circuits?

Consider the inverter

Use switch-level model for MOS devices

\[ V_H = V_{DD} \]
\[ V_L = 0 \]
\[ I_D = 0 \text{ thus } P_H = P_L = 0 \]
\[ t_{HL} = t_{LH} = 0 \] (too good to be true?)
Pull-up and Pull-down Networks

For these circuits, the PUN and PDN have 3 interesting characteristics:

Three key characteristics of Static CMOS Gates
1. PU network comprised of p-channel devices
2. PD network comprised of n-channel devices
3. One and only one of these networks is conducting at the same time

What are $V_H$ and $V_L$?
$V_H = V_{DD}, V_L = 0$ (too good to be true?)

What is the power dissipation?
$P_H = P_L = 0$ (too good to be true?)

How fast are these logic circuits?
$t_{HL} = t_{LH} = 0$ (too good to be true?)

These 3 properties are inherent in Boolean circuits with these 3 characteristics.
Pull-up and Pull-down Networks

Three key characteristics of Static CMOS Gates
1. PU network comprised of p-channel devices
2. PD network comprised of n-channel devices
3. One and only one of these networks is conducting at the same time

Three properties of Static CMOS Gates (based upon simple switch-level model)

1. $V_H = V_{DD}$, $V_L = 0$ (too good to be true?)
2. $P_H = P_L = 0$ (too good to be true?)
3. $t_{HL} = t_{LH} = 0$ (too good to be true?)

These 3 properties are inherent in Boolean circuits with these 3 characteristics
Pull-up and Pull-down Networks

Concept can be extended to arbitrary number of inputs

n-input NOR gate

n-input NAND gate
Pull-up and Pull-down Networks

1. PU network comprised of p-channel devices
2. PD network comprised of n-channel devices
3. One and only one of these networks is conducting at the same time

Concept can be extended to arbitrary number of inputs

n-input NOR gate

n-input NAND gate
Pull-up and Pull-down Networks

1. PU network comprised of p-channel devices
2. PD network comprised of n-channel devices
3. One and only one of these networks is conducting at the same time

\[ V_H = V_{DD}, \quad V_L = 0 \]
\[ P_H = P_L = 0 \]
\[ t_{HL} = t_{LH} = 0 \]
In this class, logic circuits that are implemented by interconnecting multiple-input NAND and NOR gates will be referred to as “Static CMOS Logic”

Since the set of NAND gates is complete, any combinational logic function can be realized with the NAND circuit structures considered thus far

Since the set NOR gates is complete, any combinational logic function can be realized with the NOR circuit structures considered thus far

Many logic functions are realized with “Static CMOS Logic” and this is probably the dominant design style used today!
End of Lecture 4