EE 330
Lecture 40
Digital Circuits

Optimal driving of Large Capacitive Loads
Elmore Delay
Power Dissipation in Logic Circuits
Digital Circuit Design

Review from last time

- Hierarchical Design
- Basic Logic Gates
- Properties of Logic Families
- Characterization of CMOS Inverter
- Static CMOS Logic Gates
  - Ratio Logic
- Propagation Delay
  - Simple analytical models
- Sizing of Gates

- Propagation Delay with Multiple Levels of Logic
  - Elmore Delay

- Optimal driving of Large Capacitive Loads

- Power Dissipation in Logic Circuits
- Other Logic Styles
- Array Logic
- Ring Oscillators
# Digital Circuit Design

- Hierarchical Design
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Review from last time

Minimum-sized gates

\[ F_{i2} = \frac{13}{2} \]
\[ F_{i3} = 1 \]
\[ F_{i4} = 1 \]
\[ F_{i5} = \frac{1}{2} \]
\[ F_{i6} = 12.5 \]

\[ t_{\text{PROP}} = t_{\text{REF}} \cdot \left( \frac{1}{2} \sum_{k=1}^{5} F_{i(k+1)} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right) \]

\[ t_{\text{PROP}} = t_{\text{REF}} \cdot \left( \frac{1}{2} \left( \frac{13}{2} + 1 + 1 \right) + 1 \right) \]

\[ t_{\text{PROP}} = 63.25 \cdot t_{\text{REF}} \]
Review from last time

Propagation Delay in Multiple-Levels of Logic with Stage Loading

*Mixture of Minimum-sized gates, equal rise/fall gates and OD*

\[
t_{\text{PROP}} = t_{\text{REF}} \cdot \left( \frac{1}{2} \sum_{k=1}^{5} F_{l(k+1)} \left( \frac{1}{OD_{\text{HL}k}} + \frac{1}{OD_{\text{LH}k}} \right) \right)
\]
Summary

Propagation Delay in Multiple-Levels of Logic with Stage Loading

Review from last time
Summary

Propagation Delay in Multiple-Levels of Logic with Stage Loading

Review from last time
Summary

Propagation Delay in Multiple-Levels of Logic with Stage Loading

- Equal rise/fall (no overdrive)
- Equal rise/fall with overdrive
- Minimum Sized
- Asymmetric overdrive
- Combination of equal rise/fall, minimum size and overdrive

\[ t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^{n} F_{I(k+1)} \]

\[ t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^{n} \frac{F_{I(k+1)}}{OD_k} \]

\[ t_{\text{PROP}} = t_{\text{REF}} \cdot \left( \frac{1}{2} \sum_{k=1}^{5} F_{I(k+1)} \left( \frac{1}{OD_{HLK}} + \frac{1}{OD_{LHK}} \right) \right) \]

\[ t_{\text{PROP}} = t_{\text{REF}} \cdot \left( \frac{1}{2} \sum_{k=1}^{5} F_{I(k+1)} \left( \frac{1}{OD_{HLK}} + \frac{1}{OD_{LHK}} \right) \right) \]
Summary

Propagation Delay in Multiple-Levels of Logic with Stage Loading

Review from last time

<table>
<thead>
<tr>
<th>C_{IN}/C_{REF}</th>
<th>Equal Rise/Fall</th>
<th>Equal Rise/Fall (with OD)</th>
<th>Minimum Sized</th>
<th>Asymmetric OD (OD_{HL}, OD_{LH})</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inverter</td>
<td>1</td>
<td>OD</td>
<td>1/2</td>
<td>OD_{HL} + 3 \cdot OD_{LH}</td>
</tr>
<tr>
<td>NOR</td>
<td>\frac{3k+1}{4}</td>
<td>\frac{3k+1}{4} \cdot OD</td>
<td>1/2</td>
<td>\frac{OD_{HL} + 3k \cdot OD_{LH}}{4}</td>
</tr>
<tr>
<td>NAND</td>
<td>\frac{3+k}{4}</td>
<td>\frac{3+k}{4} \cdot OD</td>
<td>1/2</td>
<td>k \cdot OD_{HL} + 3 \cdot OD_{LH}</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Overdrive</th>
<th>Equal Rise/Fall</th>
<th>Minimum Sized</th>
<th>Asymmetric OD (OD_{HL}, OD_{LH})</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inverter</td>
<td>1</td>
<td>1</td>
<td>OD_{HL}</td>
</tr>
<tr>
<td>HL</td>
<td>OD</td>
<td>1/3</td>
<td>OD_{LH}</td>
</tr>
<tr>
<td>LH</td>
<td>1</td>
<td>1</td>
<td>OD_{HL}</td>
</tr>
<tr>
<td>NOR</td>
<td>1</td>
<td>1/3</td>
<td>OD_{LH}</td>
</tr>
<tr>
<td>HL</td>
<td>OD</td>
<td>1</td>
<td>OD_{HL}</td>
</tr>
<tr>
<td>LH</td>
<td>OD</td>
<td>1/(3k)</td>
<td>OD_{LH}</td>
</tr>
<tr>
<td>NAND</td>
<td>1</td>
<td>1/4k</td>
<td>OD_{HL}</td>
</tr>
<tr>
<td>HL</td>
<td>OD</td>
<td>1/3</td>
<td>OD_{LH}</td>
</tr>
<tr>
<td>LH</td>
<td>OD</td>
<td>1/3</td>
<td>OD_{LH}</td>
</tr>
</tbody>
</table>

\[ t_{PROP}/t_{REF} = \sum_{k=1}^{n} \frac{F_{k(k+1)}}{OD_k} \]
Optimal Driving of Capacitive Loads

Assume first stage is a reference inverter

Need to determine the number of stages, n, and the OD factors for each stage to minimize $t_{\text{PROP}}$.

$$t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^{n} \frac{F_{l(k+1)}}{OD_k}$$

where $\theta_0 = 1$, $\theta_n = C_L / C_{\text{REF}}$

This becomes an n-parameter optimization (minimization) problem!

Unknown parameters: $\{\theta_1, \theta_2, \ldots, \theta_{n-1}, n\}$
Optimal Driving of Capacitive Loads

Assume first stage is a reference inverter

Order reduction strategy: Assume overdrive of stages increases by the same factor clear until the load

This becomes a 2-parameter optimization (minimization) problem!

Unknown parameters: \( \{\theta, n\} \)
Optimal Driving of Capacitive Loads

\[ t_{PROP} = t_{REF} \sum_{k=1}^{n} \frac{\theta_k}{\theta_{k-1}} \]

Unknown parameters: \( \{\theta, n\} \)

Thus obtain an expression for \( t_{PROP} \) in terms of only \( \theta \)

\[ t_{PROP} = t_{REF} n \theta \]

\[ \theta^n C_{REF} = C_L \]

\[ n = \frac{1}{\ln(\theta)} \ln \left( \frac{C_L}{C_{REF}} \right) \]

\[ t_{PROP} = t_{REF} \frac{\theta}{\ln(\theta)} \left[ \ln \frac{C_L}{C_{REF}} \right] \]
Optimal Driving of Capacitive Loads

\[ t_{\text{PROP}} = t_{\text{REF}} \frac{\theta}{\ln(\theta)} \left[ \ln \frac{C_L}{C_{\text{REF}}} \right] \]

It suffices to minimize the function

\[ f(\theta) = \frac{\theta}{\ln(\theta)} \]

\[ \frac{df}{d\theta} = \frac{\ln(\theta) - \theta \cdot \left( \frac{1}{\theta} \right)}{(\ln(\theta))^2} = 0 \]

\[ \ln(\theta) - 1 = 0 \quad \rightarrow \quad \theta = e \]

\[ n = \frac{1}{\ln(\theta)} \ln \left( \frac{C_L}{C_{\text{REF}}} \right) \quad \rightarrow \quad n = \ln \left( \frac{C_L}{C_{\text{REF}}} \right) \]
Optimal Driving of Capacitive Loads

\[ \theta_{\text{OPT}} = e \]

\[ n_{\text{OPT}} = \ln \left( \frac{C_L}{C_{\text{REF}}} \right) \]

\[ t_{\text{PROP}} = t_{\text{REF}} \frac{\theta}{\ln(\theta)} \left[ \ln \frac{C_L}{C_{\text{REF}}} \right] \]

\[ t_{\text{PROP}} = t_{\text{REF}} e \left[ \ln \frac{C_L}{C_{\text{REF}}} \right] = n\theta t_{\text{REF}} \]
Optimal Driving of Capacitive Loads

$$f = \frac{\theta}{\ln(\theta)}$$

minimum at \(\theta = e\) but shallow inflection point for \(2 < \theta < 3\)

practically pick \(\theta = 2, \theta = 2.5, \text{ or } \theta = 3\)

since optimization may provide non-integer for \(n\), must pick close integer
Optimal Driving of Capacitive Loads

- Often termed a pad driver
- Often used to drive large internal busses as well
- Generally included in standard cells or in cell library
- Device sizes can become very large
- Odd number of stages will cause signal inversion but usually not a problem
Example: Design a pad driver for driving a load capacitance of 10pF, determine $t_{\text{PROP}}$ for the pad driver, and compare this with the propagation delay for driving the pad with a minimum-sized reference inverter.

In 0.5μm process $t_{\text{REF}}=20\text{ps}$, $C_{\text{REF}}=4\text{fF}, R_{\text{PDREF}}=2.5\text{K}$

$$n_{\text{OPT}} = \ln\left(\frac{C_L}{C_{\text{REF}}}\right) = \ln\left(\frac{10\text{pF}}{4\text{fF}}\right) = 7.8$$

Select $n=8$, $\theta=2.5$

$$W_{nk} = 2.5^{k-1}, \quad W_{pk} = 3 \cdot 2.5^{k-1}$$
Optimal Driving of Capacitive Loads

Example: Design a pad driver for driving a load capacitance of 10pF, determine $t_{\text{PROP}}$ for the pad driver, and compare this with the propagation delay for driving the pad with a minimum-sized reference inverter.

In 0.5u proc $t_{\text{REF}}=20\text{ps}$, $C_{\text{REF}}=4\text{fF}$, $R_{\text{PREF}}=2.5\text{K}$

$W_{nk}=2.5^{k-1}$, $W_{pk}=3\cdot2.5^{k-1}$

<table>
<thead>
<tr>
<th>$k$</th>
<th>n-channel</th>
<th>p-channel</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1 $W_{\text{MIN}}$</td>
<td>3 $W_{\text{MIN}}$</td>
</tr>
<tr>
<td>2</td>
<td>2.5 $W_{\text{MIN}}$</td>
<td>7.5 $W_{\text{MIN}}$</td>
</tr>
<tr>
<td>3</td>
<td>6.25 $W_{\text{MIN}}$</td>
<td>18.75 $W_{\text{MIN}}$</td>
</tr>
<tr>
<td>4</td>
<td>15.6 $W_{\text{MIN}}$</td>
<td>46.9 $W_{\text{MIN}}$</td>
</tr>
<tr>
<td>5</td>
<td>39.1 $W_{\text{MIN}}$</td>
<td>117.2 $W_{\text{MIN}}$</td>
</tr>
<tr>
<td>6</td>
<td>97.7 $W_{\text{MIN}}$</td>
<td>293.0 $W_{\text{MIN}}$</td>
</tr>
<tr>
<td>7</td>
<td>244.1 $W_{\text{MIN}}$</td>
<td>732.4 $W_{\text{MIN}}$</td>
</tr>
<tr>
<td>8</td>
<td>610.4 $W_{\text{MIN}}$</td>
<td>1831.1 $W_{\text{MIN}}$</td>
</tr>
</tbody>
</table>

Note devices in last stage are very large!
Optimal Driving of Capacitive Loads

Example: Design a pad driver for driving a load capacitance of 10pF, determine $t_{PROP}$ for the pad driver, and compare this with the propagation delay for driving the pad with a minimum-sized reference inverter.

In 0.5μm process $t_{REF} = 20\text{ps}$, $C_{REF} = 4\text{fF}, R_{PDREF} = 2.5\text{K}$

$W_{nk} = 2.5^{k-1}$, $W_{pk} = 3 \cdot 2.5^{k-1}$

$t_{PROP} \approx n\theta t_{REF} = 8 \cdot 2.5 \cdot t_{REF} = 20 t_{REF}$

More accurately:

$t_{PROP} = t_{REF} \left( \sum_{k=1}^{7} \theta + \frac{1}{\theta^{7}} \frac{C_{L}}{C_{REF}} \right) = t_{REF} \left( 17.5 + \frac{1}{610} \frac{2500}{2} \right) = 21.6 t_{REF}$
Optimal Driving of Capacitive Loads

Example: Design a pad driver for driving a load capacitance of 10pF, determine $t_{PROP}$ for the pad driver, and compare this with the propagation delay for driving the pad with a minimum-sized reference inverter.

In 0.5μm proc, $t_{REF}=20\,\text{ps}$, $C_{REF}=4\,\text{fF}$, $R_{PDREF}=2.5\,\text{K}$

If driven directly with the minimum-sized reference inverter

$$t_{PROP} = t_{REF} \frac{C_L}{C_{REF}} = 2500 t_{REF}$$

Note an improvement in speed by a factor of

$$r = \frac{2500}{20} = 125$$

$W_{ nk } = 2.5^{k-1}$, $W_{ pk } = 3 \cdot 2.5^{k-1}$
Pad Driver Size Implications

\[ W_{nk} = 2.5^{k-1}, \quad W_{pk} = 3 \cdot 2.5^{k-1} \]
Area of Last Stage Larger than that of all previous stages combined!
Propagation Delay in “Logic Effort” approach

Propagation delay for equal rise/fall gates was derived to be

\[ t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^{3} \frac{F_{i(k+1)}}{OD_k} \]

Delay calculations with “logical effort” approach

Author’s definition:

\[ t_{\text{PROP}} = \sum_{k=1}^{n} f_k \]

where \( f_k \) is the “effort delay” of stage \( k \)

\[ f_k = g_k h_k \]

\( g_k \) = logical effort

\( h_k \) = electrical effort
Propagation Delay in “Logic Effort” approach

\[ t_{\text{PROP}} = \sum_{k=1}^{n} f_k \]

\[ f_k = g_k h_k \]

\[ f_k = \text{“effort delay” of stage } k \]

\[ g_k = \text{logical effort} \]

\[ h_k = \text{electrical effort} \]

Logic Effort is the ratio of the input capacitance of a gate to the input capacitance of an inverter that can deliver the same output current.

Electrical Effort is the ratio of the gate load capacitance to the input capacitance of a gate.
Propagation Delay in “Logic Effort” approach

\[ t_{\text{PROP}} = \sum_{k=1}^{n} f_k \quad f_k = g_k h_k \]

Logic Effort \((g)\) is the ratio of the input capacitance of a gate to the input capacitance of an inverter that can deliver the same output current.

Electrical Effort \((h)\) is the ratio of the gate load capacitance to the input capacitance of a gate.

\[ g_k = \frac{C_{I\text{N}_k}}{C_{\text{REF}} \cdot \text{OD}_k} \quad h_k = \frac{C_{\text{REF}} \cdot F_{I_k+1}}{C_{I\text{N}_k}} \]
Propagation Delay in “Logic Effort” approach

\[ t_{\text{PROP}} = \sum_{k=1}^{n} f_k \]

\[ f_k = g_k h_k \]

\[ g_k = \frac{C_{\text{IN}_k}}{C_{\text{REF} \cdot \text{OD}_k}} \]

\[ h_k = \frac{C_{\text{REF} \cdot F_{I(k+1)}}}{C_{\text{IN}_k}} \]

\[ f_k = \frac{F_{I(k+1)}}{\text{OD}_k} \]

\[ t_{\text{PROP}} = \sum_{k=1}^{n} f_k = \sum_{k=1}^{n} g_k h_k = \sum_{k=1}^{n} \frac{F_{I(k+1)}}{\text{OD}_k} \]
Propagation Delay in “Logic Effort” approach

\[ t_{\text{PROP}} = \sum_{k=1}^{n} f_k = \sum_{k=1}^{n} g_k h_k = \sum_{k=1}^{n} \frac{F_{l(k+1)}}{OD_k} \]

- Note with the exception of the \( t_{\text{REF}} \) that was omitted in the text, this expression is identical to what we have derived previously.
- Probably more tedious to use the “Logical Effort” approach.
- Extensions to asymmetric overdrive factors may not be trivial.
- Extensions to include parasitics may be tedious as well.
- Logical Effort is widely used throughout the industry.
Elmore Delay Calculations

- Interconnects have a distributed resistance and a distributed capacitance
  - Often modeled as resistance/unit length and capacitance per unit length
- These delay the propagation of the signal
- Effectively a transmission line
  - analysis is really complicated
- Can have much more complicated geometries
Elmore Delay Calculations

Can have much more complicated geometries
Elmore Delay Calculations

For $X_1 < X_2 < X_3$
Elmore Delay Calculations

A lumped element model of transmission line

Even this lumped model is 4-th order and a closed-form solution is very tedious!

Need a quick (and reasonably good) approximation to the delay of a delay line!!
Elmore Delay Calculations

Elmore delay: \[ t_{PD} = \sum_{i=1}^{n} \left( C_i \sum_{j=1}^{i} R_j \right) \]

- Numbering is critical (resistors and capacitors numbered from input to output)
- As stated, only applies to this specific structure
Elmore Delay Calculations

Elmore delay:

\[ t_{PD} = \sum_{i=1}^{n} \left( C_i \sum_{j=1}^{i} R_j \right) \]

• Note error in text on Page 161

\[ t_{pd} = \sum_{i} R_{n-i} C_i = \sum_{i=1}^{N} C_i \sum_{j=i}^{i} R_j \]
Elmore Delay Calculations

From Wikipedia:

**Elmore delay**[1] is a simple approximation to the delay through an RC network in an electronic system. It is often used in applications such as logic synthesis, delay calculation, static timing analysis, placement and routing, since it is simple to compute (especially in tree structured networks, which are the vast majority of signal nets within ICs) and is reasonably accurate. Even where it is not accurate, it is usually faithful, in the sense that reducing the Elmore delay will almost always reduce the true delay, so it is still useful in optimization.

Elmore Delay Calculations

Example:

Elmore delay:

\[ t_{PD} = \sum_{i=1}^{4} \left( C_i \sum_{j=1}^{i} R_j \right) \]

\[ t_{PD} = \sum_{i=1}^{4} (t_i) \]

where

\[ t_i = C_i \sum_{j=1}^{i} R_j \quad j = 1, 2, 3, 4 \]

What is really happening?

- Creating 4 first-order circuits
- Delay to \( V_1 \), \( V_2 \), \( V_3 \) and \( V_4 \) calculated separately by considering capacitors one at a time and assuming others are 0
Elmore Delay Calculations

Extensions:

Lumped Network Model:
Elmore Delay Calculations

Extensions:

1. Create a lumped element model

2. Create a path from input to output
Elmore Delay Calculations

Extensions:

3. Renumber elements along path from input to output and neglect off-path elements

4. Use Elmore Delay equation for elements on this RC network

\[
t_{PD} = \sum_{i=1}^{4} \left( C_i \sum_{j=1}^{i} R_j \right)
\]
Elmore Delay Calculations

How is a resistive load handled?
Elmore Delay Calculations

Example with resistive load:

\[ t_1 = \left( R_1 / \left[ R_2 + R_3 + R_4 + R_5 \right] \right) C_1 \]

\[ t_2 = \left( \left[ R_1 + R_2 \right] / \left[ R_3 + R_4 + R_5 \right] \right) C_2 \]

\[ t_3 = \left( \left[ R_1 + R_2 + R_3 \right] / \left[ R_4 + R_5 \right] \right) C_2 \]

\[ t_4 = \left( \left( R_1 + R_2 + R_3 + R_4 \right) / R_5 \right) C_4 \]

where

\[ t_{PD} = \sum_{i=1}^{4} (t_i) \]
Elmore Delay Calculations

With resistive load:

\[ t_{PD} = \sum_{i=1}^{n} C_i \left( \sum_{j=1}^{i} R_j \right) \parallel \left( \sum_{j=i+1}^{n+1} R_j \right) \]

\[ \text{Elmore delay:} \]

\[ t = C \frac{1}{R} \left( \frac{1}{R_1} + \frac{1}{R_2} + \ldots + \frac{1}{R_n} \right) \]
Power Dissipation in Logic Circuits

\[ P_{AVG,T} = \frac{1}{T_{CL}} \int_{t_1}^{t_1+T_{CL}} V_{DD}I_{DD}(t)dt \]
Power Dissipation in Logic Circuits

Types of Power Dissipation

- Static
- Pipe
- Dynamic
- Leakage
  - Gate
  - Diffusion
  - Drain
Static Power Dissipation

If Boolean output averages H and L 50% of the time

\[ P_{STAT, AVG} = \frac{P_H + P_L}{2} \]

\[ P_{STAT, AVG} = \frac{V_{DD}(I_{DDH} + I_{DDL})}{2} \]

Generally decreases with \( V_{DD} \)

\( I_{DDH} = I_{DDL} = 0 \) for static CMOS gates so \( P_{STAT} = 0 \)
Pipe Power Dissipation

Due to conduction of both PUN and PDN during transitions

- Can be made small if transitions are fast
- Usually negligible in Static CMOS circuits
Dynamic Power Dissipation

Due to charging and discharging $C_L$ on logic transitions

$C_L$ dissipates no power but PUN and PDN dissipate power during charge and discharge of $C_L$

$C_L$ includes all gate input capacitances of loads and interconnect capacitances
Dynamic Power Dissipation

Energy supplied by $V_{DD}$ when $C_L$ charges

$$E = \int_{t_1}^{\infty} V_{DD} I_{DD}(t) dt$$

$$I_{DD} = C_L \frac{dV_C}{dt}$$

$$E = \int_{t_1}^{\infty} V_{DD} C_L \frac{dV_C}{dt} dt$$

$$E = \int_{V_C=0}^{V_{DD}} V_{DD} C_L dV_C = V_{DD} C_L \int_{V_C=0}^{V_{DD}} dV_C = V_{DD} C_L V_C \Big|_{V_C=0}^{V_{DD}}$$

$$E = \frac{1}{2} C_L V_{DD}^2$$
Dynamic Power Dissipation

Energy supplied by $V_{DD}$ when $C_L$ charges

$$E_{DIS} = \frac{1}{2} C_L V_{DD}^2$$

Energy stored on $C_L$ after L-H transition

$$E_{STORE} = \frac{1}{2} C_L V_{DD}^2$$

Thus, energy from $V_{DD}$ for one L-H output transition is

$$E = C_L V_{DD}^2$$

When the output transitions from H to L, energy stored on $C_L$ is dissipated in PDN

If $f$ is the average transition rate of the output, determine $P_{AVG}$
Dynamic Power Dissipation

Energy from $V_{DD}$ for one L-H output transition is

$$E = C_L V_{DD}^2$$

If $f$ is the average transition rate of the output, determine $P_{AVG}$

$$P_{AVG} = \frac{E}{T} = Ef$$

$$P_{DYN} = fC_L V_{DD}^2$$

If a gate has a transition duty cycle of 50% with a clock frequency of $f_{CL}$

$$P_{DYN} = \frac{f_{CL}}{2} C_L V_{DD}^2$$

Note dependent on the square of $V_{DD}$! .... Want to make VDD small!!!

Major source of power dissipation in many static CMOS circuits for $L_{min} > 0.1\mu$m.
Leakage Power Dissipation

- **Gate**
  with very thin gate oxides, some gate leakage current flows
  major concern in 60nm and smaller processes
  actually a type of static power dissipation

- **Diffusion**
  Leakage across a reverse-biased pn junction
  Dependent upon total diffusion area
  May actually be dominant power loss on longer-channel devices
  Actually a type of static power dissipation

- **Drain**
  channel current due to small $V_{GS} - V_T$
  of significant concern only with low $V_{DD}$ processes
  actually a type of static power dissipation
Example: Determine the dynamic power dissipation in the last stage of a 6-stage CMOS pad driver if used to drive a 10pF capacitive load if clocked at 500MHz. Assume pad driver with OD of $\theta=2.5$ and $V_{DD}=3.5V$.

Solution:

$$P_{DYN} = \frac{f_{CL}}{2} C_L V_{DD}^2 = 5E8 \cdot 10pF \cdot 3.5^2 = 61mW$$

Note this solution is independent of the OD and the process.
Example: Will the CMOS pad driver actually be able to drive the 10pF load at 500MHz in the previous example in the 0.5u process?

Solution:

\[
\frac{1}{500\text{MHz}} = 2\text{nsec}
\]

\[
t_{PROP} = n\theta \cdot t_{REF} = 6 \cdot 2.5 \cdot 20\text{psec} = 0.3\text{nsec}
\]

Since \( t_{CLK} > t_{PROP} \), this pad driver can drive the 10pF load at 500MHz.
Example: Determine the dynamic power dissipation in the next to the last stage of a 6-stage CMOS pad driver if used to drive a 10pF capacitive load if clocked at 500MHz. Assume pad driver with OD of $\theta=2.5$ and $V_{DD}=3.5V$.

Solution:

$C_{IN} = \theta^5 C_{REF} = 2.5^5 \cdot 4fF = 390fF$

$P_{DYN} = f_{CL} C_L V_{DD}^2 = 5E8 \cdot 390fF \cdot (3.5)^2 = 2.4mW$
Example: Is the 6-stage CMOS pad driver adequate to drive the 10pF capacitive load as fast as possible? Assume pad driver with OD of $\theta=2.5$ and $V_{DD}=3.5\text{V}$

Solution:

$$n_{OPT} = \ln \left( \frac{C_L}{C_{REF}} \right) = \ln \left( \frac{10\text{pF}}{4\text{fF}} \right) = 7.8$$

No – an 8-stage pad driver would drive the load much faster (but is not needed if clocked at only 500MHz)
Example: Determine the power that would be required in the last stage of a CMOS pad driver to drive a 32-bit data bus off-chip if the capacitive load on each line is 2pF. Assume the clock speed is 500MHz and that each bit has an average 50% toggle rate. Assume $V_{DD}=3.5V$.

Solution:

$$P_{DYN}=32 \cdot \frac{f_{CL}}{2} C_L V_{DD}^2 = 32 \cdot \frac{5 \times 10^8}{2} \cdot 2pF \cdot 3.5^2 = 196mW$$

Note: A very large amount of power is required to take a large bus off-chip if bus has a high rate of activity.