EE 330
Lecture 40
Digital Circuits

Logical Effort
Elmore Delay
Power Dissipation in Logic Circuits
Reminder

Exam 2 Next Period

May bring two sheets of paper to exam with notes

Two attachments will also be provided

Basic Amplifier Gain Table

<table>
<thead>
<tr>
<th>$A_V$</th>
<th>$R_{in}$</th>
<th>$R_{out}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>-$g_mR_C$</td>
<td>$r_n + \beta R_E$</td>
<td>$g_m^{-1}$</td>
</tr>
<tr>
<td>$2\beta_0 R_C$</td>
<td>$2\beta_0 R_E$</td>
<td>$\beta_0$</td>
</tr>
<tr>
<td>$V_{EB}$</td>
<td>$I_{CO}$</td>
<td>$V_{EB}$</td>
</tr>
<tr>
<td>$V_{I}$</td>
<td>$V_{I}$</td>
<td>$V_{I}$</td>
</tr>
</tbody>
</table>

Propagation Delay in Multiple-Levels of Logic with Stage Loading

Asymmetric-sized gates

<table>
<thead>
<tr>
<th>Gate</th>
<th>Equal Rise/Fall (ns)</th>
<th>Equal Fall/Fall (ns)</th>
<th>Minimum Sized (ns)</th>
<th>Asymmetric OD (OD_L, OD_H)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inverter</td>
<td>1</td>
<td>0.5</td>
<td>1</td>
<td>OD_L</td>
</tr>
<tr>
<td>NOR</td>
<td>3$\times$1</td>
<td>3$\times$1</td>
<td>1</td>
<td>OD_L, 3$\times$1</td>
</tr>
<tr>
<td>NAND</td>
<td>3$\times$1</td>
<td>3$\times$1</td>
<td>1/2</td>
<td>4$\times$1</td>
</tr>
<tr>
<td>Overdrive Inverter</td>
<td>1</td>
<td>0.5</td>
<td>1</td>
<td>OD_L</td>
</tr>
<tr>
<td>LI</td>
<td>1</td>
<td>0</td>
<td>1/3</td>
<td>OD_H</td>
</tr>
<tr>
<td>LDI</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>OD_H</td>
</tr>
<tr>
<td>LDHI</td>
<td>1</td>
<td>0</td>
<td>1/3</td>
<td>OD_H</td>
</tr>
<tr>
<td>LII</td>
<td>1</td>
<td>0</td>
<td>1/3</td>
<td>OD_H</td>
</tr>
</tbody>
</table>

$t_{D_{on}} = \frac{1}{2} t_{R_{on}}$
Digital Circuit Design

- Hierarchical Design
- Basic Logic Gates
- Properties of Logic Families
- Characterization of CMOS Inverter
- Static CMOS Logic Gates
  - Ratio Logic
- Propagation Delay
  - Simple analytical models
  - Elmore Delay
- Sizing of Gates

- Propagation Delay with Multiple Levels of Logic
- Optimal driving of Large Capacitive Loads
  - Power Dissipation in Logic Circuits
- Other Logic Styles
- Array Logic
- Ring Oscillators
Review from last time

Propagation Delay in Multiple-Levels of Logic with Stage Loading

*Will consider an example with the five cases*

- Equal rise/fall (no overdrive)
- Equal rise/fall with overdrive
- Minimum Sized
- Asymmetric Overdrive
- Combination of equal rise/fall, minimum size and overdrive

*Will develop the analysis methods as needed*
#### Propagation Delay in Multiple-Levels of Logic with Stage Loading

**Asymmetric-sized gates**

<table>
<thead>
<tr>
<th>$C_{IN}/C_{REF}$</th>
<th>Equal Rise/Fall</th>
<th>Equal Rise/Fall (with OD)</th>
<th>Minimum Sized</th>
<th>Asymmetric OD (OD$<em>{HL}$, OD$</em>{LH}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inverter</td>
<td>1</td>
<td>1/p</td>
<td>1/2</td>
<td>$OD_{HL} + 3 \cdot OD_{LH}$</td>
</tr>
<tr>
<td>NOR</td>
<td>$\frac{3k+1}{4}$</td>
<td>$\frac{3k+1}{4}$ \cdot OD</td>
<td>1/2</td>
<td>$\frac{OD_{HL} + 3k \cdot OD_{LH}}{4}$</td>
</tr>
<tr>
<td>NAND</td>
<td>$\frac{3+k}{4}$</td>
<td>$\frac{3+k}{4}$ \cdot OD</td>
<td>1/2</td>
<td>$\frac{k \cdot OD_{HL} + 3 \cdot OD_{LH}}{4}$</td>
</tr>
</tbody>
</table>

**Overdrive**

<table>
<thead>
<tr>
<th>Inverter</th>
<th>HL</th>
<th>LH</th>
<th>NOR</th>
<th>HL</th>
<th>LH</th>
<th>NAND</th>
<th>HL</th>
<th>LH</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>OD</td>
<td>OD</td>
<td>OD</td>
<td>OD</td>
<td>OD</td>
<td>OD</td>
<td>OD</td>
<td>OD</td>
</tr>
<tr>
<td></td>
<td>$1$</td>
<td>$1/3$</td>
<td>$1$</td>
<td>$1/(3k)$</td>
<td>$1/k$</td>
<td>$1/3$</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**$t_{PROP}/t_{REF}$**

| $t_{PROP} = t_{REF} \cdot \left( \sum_{k=1}^{n} \frac{F_{i(k+1)}}{OD_k} \right)$ |

**$t_{PROP} = t_{REF} \cdot \left( \frac{1}{2} \sum_{k=1}^{5} \frac{F_{i(k+1)}}{OD_{HL_k}} + \frac{1}{OD_{LH_k}} \right)$**
Review from last time

Propagation Delay in Multiple-Levels of Logic with Stage Loading

- Equal rise/fall (no overdrive)
- Equal rise/fall with overdrive
- Minimum Sized
- Asymmetric overdrive

Combination of equal rise/fall, minimum size and overdrive
Review from last time

Optimal Driving of Capacitive Loads

\[ \theta_{OPT} = e \]

\[ n_{OPT} = \ln \left( \frac{C_L}{C_{REF}} \right) \]

\[ t_{PROP} = t_{REF} \frac{\theta}{\ln(\theta)} \left[ \ln \left( \frac{C_L}{C_{REF}} \right) \right] \quad \text{or} \quad t_{PROP} = t_{REF} e \left[ \ln \left( \frac{C_L}{C_{REF}} \right) \right] = n\theta \]

\[ \theta^n C_{REF} = C_L \]
Optimal Driving of Capacitive Loads

Review from last time

$f = \frac{\theta}{\ln(\theta)}$

minimum at $\theta = e$ but shallow inflection point for $2 < \theta < 3$

practically pick $\theta = 2$, $\theta = 2.5$, or $\theta = 3$

since optimization may provide non-integer for $n$, must pick close integer
Optimal Driving of Capacitive Loads

Example: Design a pad driver for driving a load capacitance of 10pF, determine $t_{\text{PROP}}$ for the pad driver, and compare this with the propagation delay for driving the pad with a minimum-sized reference inverter.

In 0.5μm proc $t_{\text{REF}}=20\text{ps}$, $C_{\text{REF}}=4\text{fF}$, $R_{\text{PDREF}}=2.5\text{kΩ}$

If driven directly with the minimum-sized reference inverter

$$t_{\text{PROP}} = t_{\text{REF}} \frac{C_L}{C_{\text{REF}}} = 2500t_{\text{REF}}$$

Note an improvement in speed by a factor of

$$r = \frac{2500}{20} = 125$$
End of Lecture 39
Optimal Driving of Capacitive Loads

Example: Design a pad driver for driving a load capacitance of 10pF, determine $t_{\text{PROP}}$ for the pad driver, and compare this with the propagation delay for driving the pad with a minimum-sized reference inverter. In 0.5μm process $t_{\text{REF}} = 20\text{ps}$, $C_{\text{REF}} = 4\text{fF}$, $R_{P\text{DREF}} = 2.5\text{K}$.

$W_{nk} = 2.5^{k-1}$, $W_{pk} = 3 \cdot 2.5^{k-1}$

<table>
<thead>
<tr>
<th>$k$</th>
<th>n-channel $L$</th>
<th>p-channel $L$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1 $W_{\text{MIN}}$</td>
<td>3 $W_{\text{MIN}}$</td>
</tr>
<tr>
<td>2</td>
<td>2.5 $W_{\text{MIN}}$</td>
<td>7.5 $W_{\text{MIN}}$</td>
</tr>
<tr>
<td>3</td>
<td>6.25 $W_{\text{MIN}}$</td>
<td>18.75 $W_{\text{MIN}}$</td>
</tr>
<tr>
<td>4</td>
<td>15.6 $W_{\text{MIN}}$</td>
<td>46.9 $W_{\text{MIN}}$</td>
</tr>
<tr>
<td>5</td>
<td>39.1 $W_{\text{MIN}}$</td>
<td>117.2 $W_{\text{MIN}}$</td>
</tr>
<tr>
<td>6</td>
<td>97.7 $W_{\text{MIN}}$</td>
<td>293.0 $W_{\text{MIN}}$</td>
</tr>
<tr>
<td>7</td>
<td>244.1 $W_{\text{MIN}}$</td>
<td>732.4 $W_{\text{MIN}}$</td>
</tr>
<tr>
<td>8</td>
<td>610.4 $W_{\text{MIN}}$</td>
<td>1831.1 $W_{\text{MIN}}$</td>
</tr>
</tbody>
</table>

Note devices in last stage are very large!
Pad Driver Size Implications

\[ W_{nk} = 2.5^{k-1}, \quad W_{pk} = 3 \cdot 2.5^{k-1} \]
Area of Last Stage Larger than that of all previous stages combined!
Propagation Delay in “Logic Effort” approach

Propagation delay for equal rise/fall gates was derived to be

\[ t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^{3} \frac{F_{I(k+1)}}{OD_k} \]

Delay calculations with “logical effort” approach

Author’s definition:

\[ t_{\text{PROP}} = \sum_{k=1}^{n} f_k \]

where \( f_k \) is the “effort delay” of stage \( k \)

\[ f_k = g_k h_k \]

\( g_k \) = logical effort

\( h_k \) = electrical effort
Propagation Delay in “Logic Effort” approach

\[ t_{PROP} = \sum_{k=1}^{n} f_k \]

\[ f_k = g_k h_k \]

\( f_k \) = “effort delay” of stage \( k \)

\( g_k \) = logical effort

\( h_k \) = electrical effort

Logic Effort is the ratio of the input capacitance of a gate to the input capacitance of an inverter that can deliver the same output current.

Electrical Effort is the ratio of the gate load capacitance to the input capacitance of a gate.
Propagation Delay in “Logic Effort” approach

\[ t_{\text{PROP}} = \sum_{k=1}^{n} f_k \]
\[ f_k = g_k h_k \]

Logic Effort \((g)\) is the ratio of the input capacitance of a gate to the input capacitance of an inverter that can deliver the same output current.

Electrical Effort \((h)\) is the ratio of the gate load capacitance to the input capacitance of a gate.

\[ g_k = \frac{C_{\text{IN}_k}}{C_{\text{REF}} \cdot \text{OD}_k} \]
\[ h_k = \frac{C_{\text{REF}} \cdot \text{FI}_{k+1}}{C_{\text{IN}_k}} \]
Propagation Delay in “Logic Effort” approach

\[ t_{\text{PROP}} = \sum_{k=1}^{n} f_k \]

\[ f_k = g_k h_k \]

\[ g_k = \frac{C_{\text{IN}k}}{C_{\text{REF}} \cdot O D_k} \]

\[ h_k = \frac{C_{\text{REF}} \cdot F_{l(k+1)}}{C_{\text{IN}k}} \]

\[ f_k = \frac{F_{l(k+1)}}{O D_k} \]

\[ t_{\text{PROP}} = \sum_{k=1}^{n} f_k = \sum_{k=1}^{n} g_k h_k = \sum_{k=1}^{n} \frac{F_{l(k+1)}}{O D_k} \]
Propagation Delay in “Logic Effort” approach

\[ t_{\text{PROP}} = \sum_{k=1}^{n} f_k = \sum_{k=1}^{n} g_k h_k = \sum_{k=1}^{n} \frac{F_{i(k+1)}}{\text{OD}_k} \]

- Note with the exception of the \( t_{\text{REF}} \) that was omitted in the text, this expression is identical to what we have derived previously

- Probably more tedious to use the “Logical Effort” approach

- Extensions to asymmetric overdrive factors may not be trivial

- Extensions to include parasitics may be tedious as well

- Logical Effort is widely used throughout the industry
Elmore Delay Calculations

- Interconnects have a distributed resistance and a distributed capacitance
  - Often modeled as resistance/unit length and capacitance per unit length
- These delay the propagation of the signal
- Effectively a transmission line
  - Analysis is really complicated
- Can have much more complicated geometries
Elmore Delay Calculations

Can have much more complicated geometries
Elmore Delay Calculations

For \( X_1 < X_2 < X_3 \)
Elmore Delay Calculations

A lumped element model of transmission line

Even this lumped model is 4-th order and a closed-form solution is very tedious!

Need a quick (and reasonably good) approximation to the delay of a delay line!!
Elmore Delay Calculations

Elmore delay: \[ t_{PD} = \sum_{i=1}^{n} \left( C_i \sum_{j=1}^{i} R_j \right) \]

- Numbering is critical (resistors and capacitors numbered from input to output)
- As stated, only applies to this specific structure
Elmore Delay Calculations

Elmore delay:

\[ t_{pd} = \sum_{i=1}^{n} \left( C_i \sum_{j=1}^{i} R_j \right) \]

• Note error in text on Page 161

\[ t_{pd} = \sum_{i} R_{n-i} C_i = \sum_{i=1}^{N} C_i \sum_{j=i}^{i} R_j \]
Elmore Delay Calculations

\[
 t_{PD} = \sum_{i=1}^{n} \left( C_i \sum_{j=1}^{i} R_j \right)
\]

From Wikipedia:

**Elmore delay**[1] is a simple approximation to the delay through an RC network in an electronic system. It is often used in applications such as logic synthesis, delay calculation, static timing analysis, placement and routing, since it is simple to compute (especially in tree structured networks, which are the vast majority of signal nets within ICs) and is reasonably accurate. Even where it is not accurate, it is usually faithful, in the sense that reducing the Elmore delay will almost always reduce the true delay, so it is still useful in optimization.

Elmore Delay Calculations

Example:

Elmore delay:

\[ t_{PD} = \sum_{i=1}^{4} \left( \sum_{j=1}^{i} R_j \right) C_i \]

\[ t_{PD} = \sum_{i=1}^{4} t_i \]

where \[ t_i = C_i \sum_{j=1}^{i} R_j \quad j = 1, 2, 3, 4 \]

What is really happening?

- Creating 4 first-order circuits
- Delay to \( V_1 \), \( V_2 \), \( V_3 \) and \( V_4 \) calculated separately by considering capacitors one at a time and assuming others are 0
Elmore Delay Calculations

Extensions:

Lumped Network Model:
Elmore Delay Calculations

Extensions:

1. Create a lumped element model

2. Create a path from input to output
Elmore Delay Calculations

Extensions:

3. Renumber elements along path from input to output and neglect off-path elements

4. Use Elmore Delay equation for elements on this RC network

\[
\begin{equation}
\sum_{i=1}^{4} C_i \sum_{j=1}^{i} R_j
\end{equation}
\]
Elmore Delay Calculations

How is a resistive load handled?
Elmore Delay Calculations

Example with resistive load:

\[
R_1 \quad R_2 \quad R_3 \quad R_4 \quad V_{\text{OUT}}
\]
\[
C_1 \quad C_2 \quad C_3 \quad C_4
\]

Elmore delay:

\[
t_{PD} = \sum_{i=1}^{4} \left( C_i \sum_{j=1}^{i} R_j \right)
\]

where

\[
t_{PD} = \sum_{i=1}^{4} (t_i)
\]

\[
t_i = C_i \sum_{j=1}^{i} R_j \quad j = 1, 2, 3
\]

\[
t_4 = C_4 \left( \left[ \sum_{j=1}^{4} R_j \right] / R_5 \right)
\]
Elmore Delay Calculations

With resistive load:

Simple Elmore delay: \[ t_{PD} = \sum_{i=1}^{n-1} \left( C_i \sum_{j=1}^{i} R_j \right) + C_n \left( \sum_{j=1}^{n} R_j \right) // R_L \]

Actually, \( R_L \) affects all of the delays and a modestly better but modestly more complicated delay model is often used.
Elmore Delay Calculations

Example with resistive load:

Elmore delay:

\[ t_1 = \left( \frac{R_1}{R_2 + R_3 + R_4 + R_5} \right) C_1 \]

\[ t_2 = \left( \frac{R_1 + R_2}{R_3 + R_4 + R_5} \right) C_2 \]

\[ t_i = C_i \left( \sum_{j=1}^{i} R_j \right) \left( \sum_{j=i+1}^{5} R_j \right) \]

where

\[ t_{PD} = \sum_{i=1}^{4} (t_i) \]
Elmore Delay Calculations

With resistive load:

\[
\begin{align*}
    t_{PD} &= \sum_{i=1}^{n} C_i \left( \sum_{j=1}^{i} R_j \right) \parallel \left[ \sum_{j=i+1}^{n+1} R_j \right] \\
    &\text{Elmore delay:}
\end{align*}
\]
Power Dissipation in Logic Circuits

\[ P_{AVG,T} = \frac{1}{T_{CL}} \int_{t_1}^{t_1+T_{CL}} V_{DD}I_{DD}(t)dt \]
Power Dissipation in Logic Circuits

Types of Power Dissipation

- Static
- Pipe
- Dynamic
- Leakage
  - Gate
  - Diffusion
  - Drain
Static Power Dissipation

If Boolean output averages H and L 50% of the time

\[
P_{\text{STAT, AVG}} = \frac{P_H + P_L}{2}
\]

\[
P_{\text{STAT, AVG}} = \frac{V_{\text{DD}}(I_{\text{DDH}} + I_{\text{DDL}})}{2}
\]

Generally decreases with \( V_{\text{DD}} \)

\( I_{\text{DDH}} = I_{\text{DDL}} = 0 \) for static CMOS gates so \( P_{\text{STAT}} = 0 \)
Pipe Power Dissipation

Due to conduction of both PUN and PDN during transitions

- Can be made small if transitions are fast
- Usually negligible in Static CMOS circuits
Dynamic Power Dissipation

Due to charging and discharging $C_L$ on logic transitions

$C_L$ dissipates no power but PUN and PDN dissipate power during charge and discharge of $C_L$

$C_L$ includes all gate input capacitances of loads and interconnect capacitances
Dynamic Power Dissipation

Energy supplied by $V_{DD}$ when $C_L$ charges

$$E = \int_{t_1}^{\infty} V_{DD} I_{DD}(t) dt$$

$$I_{DD} = C_L \frac{dV_C}{dt}$$

$$E = \int_{t_1}^{\infty} V_{DD} C_L \frac{dV_C}{dt} dt$$

$$V_{DD} = \int_{V_C=0}^{V_{DD}} V_{DD} C_L dV_C = V_{DD} C_L \int_{V_C=0}^{V_{DD}} dV_C = V_{DD} C_L V_C \bigg|_{V_C=0}^{V_{DD}}$$

$$E = \frac{1}{2} C_L V_{DD}^2$$
Dynamic Power Dissipation

Energy supplied by $V_{DD}$ when $C_L$ charges

$$E_{DIS} = \frac{1}{2} C_L V_{DD}^2$$

Energy stored on $C_L$ after L-H transition

$$E_{STORE} = \frac{1}{2} C_L V_{DD}^2$$

Thus, energy from $V_{DD}$ for one L-H output transition is

$$E = C_L V_{DD}^2$$

When the output transitions from H to L, energy stored on $C_L$ is dissipated in PDN

If $f$ is the average transition rate of the output, determine $P_{AVG}$
Dynamic Power Dissipation

Energy from $V_{DD}$ for one L-H output transition is

$$E = C_L V_{DD}^2$$

If $f$ is the average transition rate of the output, determine $P_{AVG}$

$$P_{AVG} = \frac{E}{T} = Ef$$

$$P_{DYN} = fC_L V_{DD}^2$$

If a gate has a transition duty cycle of 50% with a clock frequency of $f_{CL}$

$$P_{DYN} = \frac{f_{CL}}{2} C_L V_{DD}^2$$

Note dependent on the square of $V_{DD}$! .... Want to make VDD small !!!

Major source of power dissipation in many static CMOS circuits for $L_{min}>0.1u$
Leakage Power Dissipation

- **Gate**
  
  with very thin gate oxides, some gate leakage current flows
  major concern in 60nm and smaller processes
  actually a type of static power dissipation

- **Diffusion**
  
  Leakage across a reverse-biased pn junction
  Dependent upon total diffusion area
  May actually be dominant power loss on longer-channel devices
  Actually a type of static power dissipation

- **Drain**
  
  channel current due to small $V_{GS}-V_T$
  of significant concern only with low $V_{DD}$ processes
  actually a type of static power dissipation
Example: Determine the dynamic power dissipation in the last stage of a 6-stage CMOS pad driver if used to drive a 10pF capacitive load if clocked at 500MHz. Assume pad driver with OD of θ=2.5 and V_{DD}=3.5V.

Solution:

\[
P_{\text{DYN}} = \frac{f_{CL}}{2} C_L V_{DD}^2 = 5 \times 10^8 \cdot 10\text{pF} \cdot 3.5^2 = 61\text{mW}
\]

Note this solution is independent of the OD and the process.
Example: Will the CMOS pad driver actually be able to drive the 10pF load at 500MHz in the previous example in the 0.5u process?

Solution:

\[ t_{\text{CLK}} = \frac{1}{500\text{MHz}} = 2\text{nsec} \]

\[ t_{\text{PROP}} = n\theta \cdot t_{\text{REF}} = 6\cdot 2.5 \cdot 20\text{psec} = 0.3\text{nsec} \]

since \( t_{\text{CLK}} > t_{\text{PROP}} \), this pad driver can drive the 10pF load at 500MHz

In 0.5u proc \( t_{\text{REF}} = 20\text{ps}, C_{\text{REF}} = 4\text{fF}, R_{\text{PDREF}} = 2.5\text{K} \)
Example: Determine the dynamic power dissipation in the next to the last stage of a 6-stage CMOS pad driver if used to drive a 10pF capacitive load if clocked at 500MHz. Assume pad driver with OD of $\theta=2.5$ and $V_{DD}=3.5V$.

Solution:

$$C_{IN}=\theta^5 C_{REF}=2.5^5 \cdot 4fF=390fF$$

$$P_{DYN}=f_{CL} C_{L} V_{DD}^2 = 5E8 \cdot 390fF \cdot 3.5^2 = 2.4mW$$
Example: Is the 6-stage CMOS pad driver adequate to drive the 10pF capacitive load as fast as possible? Assume pad driver with OD of $\theta=2.5$ and $V_{DD}=3.5V$

Solution:

$$n_{OPT} = \ln\left( \frac{C_L}{C_{REF}} \right) = \ln\left( \frac{10\text{pF}}{4\text{fF}} \right) = 7.8$$

No – an 8-stage pad driver would drive the load much faster (but is not needed if clocked at only 500MHz)
Example: Determine the power that would be required in the last stage of a CMOS pad driver to drive a 32-bit data bus off-chip if the capacitive load on each line is 2pF. Assume the clock speed is 500MHz and that each bit has an average 50% toggle rate. Assume $V_{DD} = 3.5V$.

Solution:

$$P_{DYN} = 32 \cdot \frac{f_{CL}}{2} \cdot C_L \cdot \frac{V_{DD}^2}{2} = 32 \cdot \frac{5 \cdot 10^8}{2} \cdot 2pF \cdot 3.5^2 = 196mW$$

Note: A very large amount of power is required to take a large bus off-chip if bus has a high rate of activity.