EE 330
Lecture 40
Digital Circuits

Propagation Delay in Multiple Levels of Logic
Optimally Driving Large Capacitive Loads
Review from last lecture

**Device Sizing** – minimum size driving $C_{REF}$

\[ V_{IN} \rightarrow V_{OUT} \]

- **INV**

- **k-input NOR**
  \[ t_{PROP} = ? \]
  \[ t_{PROP} = 0.5t_{REF} + \frac{3k}{2}t_{REF} \]
  \[ t_{PROP} = \left( \frac{3k+1}{2} \right)t_{REF} \]

\[ F1 = \frac{C_{REF}}{2} \]

\[ V_{DD} \]

\[ A_k \rightarrow M_{2k} \]
\[ \cdots \]
\[ A_2 \rightarrow M_{22} \]
\[ A_1 \rightarrow M_{21} \]
\[ A_1 \rightarrow M_{11} \]
\[ A_2 \rightarrow M_{12} \]
\[ \cdots \]
\[ A_k \rightarrow M_{1k} \]

- **k-input NOR**
  \[ t_{PROP} = ? \]
  \[ t_{PROP} = \frac{3}{2}t_{REF} + \frac{k}{2}t_{REF} \]
  \[ t_{PROP} = \frac{3+k}{2}t_{REF} \]

\[ F1 = \frac{C_{REF}}{2} \]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Analysis strategy: Express delays in terms of those of reference inverter

Reference Inverter

\[ C_{\text{REF}} = C_{\text{IN}} = 4C_{\text{OX}} W_{\text{MIN}} L_{\text{MIN}} \]

\[ R_{\text{PDREF}} = \frac{L_{\text{MIN}}}{\mu_n C_{\text{OX}} W_{\text{MIN}} V_{DD} - V_{Tn}} \]

\[ V_{Tn} = 0.2V_{DD} \]

\[ t_{\text{REF}} = t_{\text{HLREF}} + t_{\text{LHREF}} = 2R_{\text{PDREF}} C_{\text{REF}} \]

Assume \( \mu_n/\mu_p = 3 \)

\( W_n = W_{\text{MIN}}, \ W_p = 3W_{\text{MIN}} \)

\( V_{IN}, V_{OUT}, M_1, M_2, V_{DD} \)

In 0.5u proc \( t_{\text{REF}} = 20\text{ps}, \ C_{\text{REF}} = 4\text{fF}, R_{\text{PDREF}} = 2.5\text{K} \)

\( L_n=L_p=L_{\text{MIN}} \)
Propagation Delay with Stage Loading

$t_{\text{REF}} = 2R_{PD\text{REF}} C_{\text{REF}}$

$C_{\text{REF}} = C_{\text{IN}} = 4C_{\text{OX}} W_{\text{MIN}} L_{\text{MIN}}$

$F_{I_c} = \frac{C}{C_{\text{REF}}}$

$F_{I_G} = \frac{C_{\text{INk}}}{C_{\text{REF}}}$

$F_{I_i} = \frac{C_{\text{INl}}}{C_{\text{REF}}}$

$F_I = \sum_{\text{Gates}} C_{\text{INGi}} + \sum_{\text{Capacitances}} C_{\text{INCi}} + \sum_{\text{Interconnects}} C_{\text{INli}}$

Fl can be expressed either in units of capacitance or normalized to $C_{\text{REF}}$

Most commonly $F_I$ is normalized but must determine from context
Propagation Delay Through Multiple Stages of Logic with Stage Loading

(assuming gate drives are all same as that of reference inverter)

Identify the gate path from A to F

\[ t_{PROP_k} = t_{REF} F_{I(k+1)} \]

Propagation delay from A to F:

\[ t_{PROP} = t_{REF} \sum_{k=1}^{n} F_{I(k+1)} \]
Define the Asymmetric Overdrive Factors of the stage to be the factor by which PU and PD resistors are scaled relative to those of the reference inverter.

\[ R_{PDEFF} = \frac{R_{PDREF}}{OD_{HL}} \]
\[ R_{PUEFF} = \frac{R_{PUREF}}{OD_{LH}} \]

If inverter sized for equal rise/fall, define OD by \( OD_{HL} = OD_{LH} = OD \)

\[ t_{HL} = t_{LH} = \frac{R_{PDREF}}{OD} \]
\[ C_L = R_{PDREF}C_{REF} \]
\[ F_{IL} = \frac{F_{IL}}{OD} \]

\[ t_{PROP} = t_{LH} + t_{HL} = t_{REF} \frac{F_{IL}}{OD} \]

OD may be larger or smaller than 1
Propagation Delay in Multiple-Levels of Logic with Stage Loading

\[ F_{Ik} \text{ denotes the total loading on stage } k \text{ which is the sum of the } F_i \text{ of all loading on stage } k \]

Notation:

\[ t_k = t_{PROP_k} \]

Propagation delay from A to F:

\[ t_{PROP} = t_{REF} \sum_{k=1}^{n} \frac{F_{I(k+1)}}{OD_k} \]
Review from last lecture

Propagation Delay in Multiple-Levels of Logic with Stage Loading

- Equal rise/fall (no overdrive)
- Equal rise/fall with overdrive
- Minimum Sized
- Asymmetric overdrive
- Combination of equal rise/fall, minimum size and overdrive
Review from last lecture

Driving Notation

- Equal rise/fall (no overdrive)
- Equal rise/fall with overdrive
- Minimum Sized
- Asymmetric Overdrive

Notation will be used only if it is not clear from the context what sizing is being used
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Asymmetric Overdrive

\[ t_{\text{PROP}} = t_{\text{HL}} + t_{\text{LH}} = \frac{1}{2} t_{\text{REF}} F_{I} \left( \frac{1}{OD_{\text{HL}}} + \frac{1}{OD_{\text{LH}}} \right) \]

When propagating through \( n \) stages:

\[ F_{i_k} \text{ denotes the total loading on stage } k \text{ which is } \text{the sum of the } F_{i} \text{ of all loading on stage } k \]

\[ t_{\text{PROP}} = t_{\text{REF}} \cdot \left( \sum_{k=1}^{n} F_{i(k+1)} \right) \left( \frac{1}{OD_{\text{HL}k}} + \frac{1}{OD_{\text{LH}k}} \right) \]
Review from last lecture

Propagation Delay in Multiple-Levels of Logic with Stage Loading

Overdrive Notation

Equal Rise/Fall with overdrive OD

Examples

Equal Rise/Fall with overdrive of 8

If \( W_n = W_{\text{MIN}} \), minimum sized inverter
Propagation Delay in Multiple-Levels of Logic with Stage Loading

*Equal rise-fall gates, no overdrive*

\[ t_{\text{REF}} = 2t_{\text{HL-REF}} \]

In 0.5u proc \( t_{\text{REF}} = 20\text{ps} \), \( C_{\text{REF}} = 4\text{fF}, R_{\text{PDREF}} = 2.5\text{K} \)
Propagation Delay in Multiple-Levels of Logic with Stage Loading

*Equal rise-fall gates, no overdrive*

<table>
<thead>
<tr>
<th>$C_{IN}/C_{REF}$</th>
<th>Equal Rise/Fall</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Inverter</strong></td>
<td>1</td>
</tr>
<tr>
<td><strong>NAND</strong></td>
<td>$\frac{3k+1}{4}$</td>
</tr>
<tr>
<td><strong>NOR</strong></td>
<td>$\frac{3+k}{4}$</td>
</tr>
</tbody>
</table>

**Overdrive**

<table>
<thead>
<tr>
<th><strong>Inverter</strong></th>
<th><strong>HL</strong></th>
<th>1</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>LH</strong></td>
<td>1</td>
<td></td>
</tr>
<tr>
<td><strong>NOR</strong></td>
<td>1</td>
<td></td>
</tr>
<tr>
<td><strong>HL</strong></td>
<td>1</td>
<td></td>
</tr>
<tr>
<td><strong>LH</strong></td>
<td>1</td>
<td></td>
</tr>
<tr>
<td><strong>NAND</strong></td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

**$t_{PROP}/t_{REF}$**

\[ t_{PROP} = t_{REF} \sum_{k=1}^{5} F_{i(k+1)} \]
Equal rise-fall gates, no overdrive

In 0.5u proc  \( t_{\text{REF}}=20\text{ps} \), \( C_{\text{REF}}=4\text{fF} \), \( R_{\text{PDREF}}=2.5\text{K} \)

\[
I_2 = 10.25 \\
I_3 = 4.25 \\
I_4 = 4.25 \\
I_5 = 1.25 \\
I_6 = 12.5
\]

\[
t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^{5} F_{k+1}
\]

\[
t_{\text{PROP}} = t_{\text{REF}} \times 10.25 + 4.25 + 4.25 + 1.25 + 12.5
\]

\[
t_{\text{PROP}} = 32.5 t_{\text{REF}}
\]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Equal rise-fall gates, with overdrive

In 0.5u proc \( t_{\text{REF}}=20\text{ps} \), \( C_{\text{REF}}=4\text{fF} \), \( R_{\text{PDREF}}=2.5\text{K} \)

\[ t_{\text{PROP}}=t_{\text{REF}} \sum_{k=1}^{n} \frac{F_{k+1}}{\text{OD}_k} \]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Equal rise-fall gates, with overdrive

<table>
<thead>
<tr>
<th>$C_{IN}/C_{REF}$</th>
<th>Equal Rise/Fall</th>
<th>Equal Rise/Fall (with OD)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inverter</td>
<td>1</td>
<td>$OD$</td>
</tr>
<tr>
<td>NOR</td>
<td>$\frac{3k+1}{4}$</td>
<td>$\frac{3k+1}{4} \cdot OD$</td>
</tr>
<tr>
<td>NAND</td>
<td>$\frac{3+k}{4}$</td>
<td>$\frac{3+k}{4} \cdot OD$</td>
</tr>
<tr>
<td>Overdrive</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Inverter</td>
<td></td>
<td></td>
</tr>
<tr>
<td>HL</td>
<td>1</td>
<td>$OD$</td>
</tr>
<tr>
<td>LH</td>
<td>1</td>
<td>$OD$</td>
</tr>
<tr>
<td>NOR</td>
<td></td>
<td></td>
</tr>
<tr>
<td>HL</td>
<td>1</td>
<td>$OD$</td>
</tr>
<tr>
<td>LH</td>
<td>1</td>
<td>$OD$</td>
</tr>
<tr>
<td>NAND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>HL</td>
<td>1</td>
<td>$OD$</td>
</tr>
<tr>
<td>LH</td>
<td>1</td>
<td>$OD$</td>
</tr>
</tbody>
</table>

$t_{PROP}/t_{REF} = \sum_{k=1}^{n} F_{l(k+1)}$  $t_{PROP} = t_{REF} \sum_{k=1}^{n} \frac{F_{l(k+1)}}{OD_k}$
Equal rise-fall gates, with overdrive

\[
\begin{align*}
F_i2 &= 14.25 \\
F_i3 &= 13 \\
F_i4 &= 4.25 \\
F_i5 &= 5 \\
F_i6 &= 12.5 \\
\end{align*}
\]

\[
t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^{n} \frac{F_{i_{k+1}}}{\text{OD}_k}
\]

\[
t_{\text{PROP}} = t_{\text{REF}} \left( \frac{14.25}{8} + \frac{13}{1} + \frac{4.25}{6} + \frac{5}{1} + \frac{12.5}{4} \right)
\]

\[
t_{\text{PROP}} = 23.6 \, t_{\text{REF}}
\]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Minimum-sized gates

In 0.5u proc \( t_{REF}=20\text{ps} \),
\( C_{REF}=4\text{fF}, R_{PDREF}=2.5\text{K} \)

\[ t_{PROP} = t_{REF} \cdot ? \]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Minimum-sized gates

Minimum-sized gates

$\text{t_{PROP}} = \text{t_{REF}} \cdot \square$
Propagation Delay with Minimum-Sized Gates

But recall

Thus

Now, for k levels of logic

\[ t_{\text{PROP}} = t_{\text{REF}} \cdot \frac{1}{2} \sum_{k=1}^{n} F_{(k+1)} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \]
Propagation Delay with Minimum-Sized Gates

\[ t_{\text{PROP}} = t_{\text{REF}} \cdot \left( \frac{1}{2} \sum_{k=1}^{n} F_{l(k+1)} \left( \frac{1}{OD_{\text{HL}_k}} + \frac{1}{OD_{\text{LH}_k}} \right) \right) \]

Still need OD_{\text{HL}} and OD_{\text{LH}}

Still need F_{l}
Propagation Delay with minimum-sized gates

\[ O_D^{HL} = \frac{1}{3k} \]

\[ O_D^{LH} = \frac{1}{3} \]

\[ F_I = 2C_{OX}W_{MIN}L_{MIN} \]

\[ C_{REF} = 4C_{OX}W_{MIN}L_{MIN} \]

\[ F_I = \frac{C_{REF}}{2} \]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Minimum-sized gates

<table>
<thead>
<tr>
<th></th>
<th>Equal Rise/Fall</th>
<th>Equal Rise/Fall (with OD)</th>
<th>Minimum Sized</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{IN}/C_{REF}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Inverter</td>
<td>1</td>
<td>OD</td>
<td></td>
</tr>
<tr>
<td>NOR</td>
<td>$\frac{3k+1}{4}$</td>
<td>$\frac{3k+1}{4}$·OD</td>
<td></td>
</tr>
<tr>
<td>NAND</td>
<td>$\frac{3+k}{4}$</td>
<td>$\frac{3+k}{4}$·OD</td>
<td></td>
</tr>
<tr>
<td>Overdrive</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Inverter</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HL</td>
<td>1</td>
<td>OD</td>
<td></td>
</tr>
<tr>
<td>LH</td>
<td>1</td>
<td>OD</td>
<td></td>
</tr>
<tr>
<td>NOR</td>
<td>1</td>
<td>OD</td>
<td></td>
</tr>
<tr>
<td>HL</td>
<td>1</td>
<td>OD</td>
<td></td>
</tr>
<tr>
<td>LH</td>
<td>1</td>
<td>OD</td>
<td></td>
</tr>
<tr>
<td>NAND</td>
<td>1</td>
<td>OD</td>
<td></td>
</tr>
<tr>
<td>HL</td>
<td>1</td>
<td>OD</td>
<td></td>
</tr>
<tr>
<td>$t_{PROP}/t_{REF}$</td>
<td>$\sum_{k=1}^{n} F_{I(k+1)}$</td>
<td>$\sum_{k=1}^{n} F_{I(k+1)}/OD_k$</td>
<td></td>
</tr>
</tbody>
</table>

$OD_{HL} = 1$

$OD_{LH} = \frac{1}{3k}$

$OD_{HL} = 1/k$

$OD_{LH} = \frac{1}{3}$

$F_{I} = \frac{C_{REF}}{2}$
### Propagation Delay in Multiple-Levels of Logic with Stage Loading

**Minimum-sized gates**

<table>
<thead>
<tr>
<th></th>
<th>Equal Rise/Fall</th>
<th>Equal Rise/Fall (with OD)</th>
<th>Minimum Sized</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>C&lt;sub&gt;IN&lt;/sub&gt;/C&lt;sub&gt;REF&lt;/sub&gt;</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Inverter</td>
<td>1</td>
<td>OD</td>
<td>1/2</td>
</tr>
<tr>
<td></td>
<td>3k+1/4</td>
<td>3k+1/4 OD</td>
<td></td>
</tr>
<tr>
<td>NOR</td>
<td>3+k/4</td>
<td>3+k/4 OD</td>
<td>1/2</td>
</tr>
<tr>
<td>NAND</td>
<td>3+k/4</td>
<td>3+k/4 OD</td>
<td>1/2</td>
</tr>
<tr>
<td>Overdrive</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Inverter</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HL</td>
<td>1</td>
<td>OD</td>
<td>1</td>
</tr>
<tr>
<td>LH</td>
<td>1</td>
<td>OD</td>
<td>1/3</td>
</tr>
<tr>
<td>NOR</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HL</td>
<td>1</td>
<td>OD</td>
<td>1</td>
</tr>
<tr>
<td>LH</td>
<td>1</td>
<td>OD</td>
<td>1/(3k)</td>
</tr>
<tr>
<td>NAND</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HL</td>
<td>1</td>
<td>OD</td>
<td>1/k</td>
</tr>
<tr>
<td>LH</td>
<td>1</td>
<td>OD</td>
<td>1/3</td>
</tr>
<tr>
<td><strong>t&lt;sub&gt;PROP&lt;/sub&gt;/t&lt;sub&gt;REF&lt;/sub&gt;</strong></td>
<td>(\sum_{k=1}^{n} F_{l(k+1)})</td>
<td>(\sum_{k=1}^{n} F_{l(k+1)} / \text{OD}_k)</td>
<td>(1/2 \sum_{k=1}^{n} F_{l(k+1)} \left( 1 / \text{OD}<em>{HLk} + 1 / \text{OD}</em>{LHk} \right))</td>
</tr>
</tbody>
</table>

**Overdrive Impedance**

- \(\text{OD}_{HL} = 1\)
- \(\text{OD}_{LH} = 1/3k\)
- \(\text{OD}_{HL} = 1/k\)
- \(\text{OD}_{LH} = 1/3k\)

- \(F_1 = \frac{C_{REF}}{2}\)

**Diagrams:**

- Circuit diagram of a minimum-sized gate network with overdrive levels.
- Symbol representation of the overdrive and stage loading conditions.
Minimum-sized gates

- \( \frac{C}{C_{REF}} \rightarrow \frac{20fF}{4fF} = 5 \)
- \( F_{i2} = 13/2 \)
- \( F_{i3} = 1 \)
- \( F_{i4} = 1 \)
- \( F_{i5} = 1/2 \)
- \( F_{i6} = 12.5 \)

\[ t_{PROP} = t_{REF} \cdot \left( \frac{1}{2} \sum_{k=1}^{5} F_{i(k+1)} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right) \]

\[ t_{PROP} = t_{REF} \cdot \frac{1}{2} \left( \frac{13}{2} \cdot 3 + 3 + 1 \cdot 12 + 1 + 1 \cdot 6 + 10 + \frac{1}{2} \cdot 9 + 1 \cdot 12.5 + 2 + 3 \right) \]

\[ t_{PROP} = 63.25 \cdot t_{REF} \]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Asymmetric-sized gates

\[ t_{\text{PROP}} = t_{\text{REF}} \cdot ? \]
## Propagation Delay in Multiple-Levels of Logic with Stage Loading

**Asymmetric-sized gates**

<table>
<thead>
<tr>
<th>C_{in}/C_{ref}</th>
<th>Equal Rise/Fall</th>
<th>Equal Rise/Fall (with OD)</th>
<th>Minimum Sized</th>
<th>Asymmetric OD (OD_{hl}, OD_{lh})</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inverter</td>
<td>1</td>
<td>OD</td>
<td>1/2</td>
<td>(OD_{hl} + 3 \cdot OD_{lh})</td>
</tr>
<tr>
<td>NOR</td>
<td>(\frac{3+k}{4})</td>
<td>(\frac{3+k}{4} \cdot OD)</td>
<td>1/2</td>
<td>(OD_{hl} + 3k \cdot OD_{lh})</td>
</tr>
<tr>
<td>NAND</td>
<td>(\frac{3+k}{4})</td>
<td>(\frac{3+k}{4} \cdot OD)</td>
<td>1/2</td>
<td>(k \cdot OD_{hl} + 3 \cdot OD_{lh})</td>
</tr>
<tr>
<td>Overdrive</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Inverter</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HL</td>
<td>1</td>
<td>OD</td>
<td>1/3</td>
<td>(OD_{hl})</td>
</tr>
<tr>
<td>LH</td>
<td>1</td>
<td>OD</td>
<td>1/3</td>
<td>(OD_{lh})</td>
</tr>
<tr>
<td>NOR</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HL</td>
<td>1</td>
<td>OD</td>
<td>1/3</td>
<td>(OD_{hl})</td>
</tr>
<tr>
<td>LH</td>
<td>1</td>
<td>OD</td>
<td>1/3</td>
<td>(OD_{lh})</td>
</tr>
<tr>
<td>NAND</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HL</td>
<td>1</td>
<td>OD</td>
<td>(1/k)</td>
<td>(OD_{hl})</td>
</tr>
<tr>
<td>LH</td>
<td>1</td>
<td>OD</td>
<td>(1/k)</td>
<td>(OD_{lh})</td>
</tr>
</tbody>
</table>

\[
t_{PROP}/t_{REF} = \sum_{k=1}^{n} F_{(k+1)} / \sum_{k=1}^{n} \frac{F_{(k+1)}}{OD_k} = \frac{1}{2} \sum_{k=1}^{n} F_{(k+1)} \left( \frac{1}{OD_{hl_k}} + \frac{1}{OD_{lh_k}} \right) = \frac{1}{2} \sum_{k=1}^{n} F_{(k+1)} \left( \frac{1}{OD_{hl_k}} \right) + \frac{1}{2} \sum_{k=1}^{n} F_{(k+1)} \left( \frac{1}{OD_{lh_k}} \right)
\]

\[
t_{PROP} = t_{REF} \cdot \left( \sum_{k=1}^{n} F_{(k+1)} \left( \frac{1}{OD_{hl_k}} + \frac{1}{OD_{lh_k}} \right) \right)
\]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Asymmetric-sized gates

Asymmetric-sized gates

\[ t_{\text{PROP}} = t_{\text{REF}} \cdot \left( \frac{1}{2} \sum_{k=1}^{5} f_{(k+1)} \left( \frac{1}{OD_{HL_k}} + \frac{1}{OD_{LH_k}} \right) \right) \]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

*Mixture of Minimum-sized gates, equal rise/fall gates and OD*

\[ t_{PROP} = t_{REF} \cdot ? \]
Driving Notation

- Equal rise/fall (no overdrive)
- Equal rise/fall with overdrive
- Minimum Sized
- Asymmetric Overdrive
Propagation Delay in Multiple-Levels of Logic with Stage Loading

*Mixture of Minimum-sized gates, equal rise/fall gates and OD*

\[ t_{PROP} = t_{REF} \cdot \left( \frac{1}{2} \sum_{k=1}^{5} F_{l(k+1)} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right) \]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

*Mixture of Minimum-sized gates, equal rise/fall gates and OD*

\[ t_{\text{PROP}} = t_{\text{REF}} \cdot \left( \sum_{k=1}^{5} F_{(k+1)} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right) \]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

- Equal rise/fall (no overdrive)
- Equal rise/fall with overdrive
- Minimum Sized
- Asymmetric overdrive
- Combination of equal rise/fall, minimum size and overdrive
Recall

Propagation Delay in Multiple-Levels of Logic with Stage Loading

Overdrive

\[ V_{\text{IN}} \rightarrow V_{\text{OUT}} \]

Define the Overdrive Factor of the stage to be the factor by which PU and PD resistors are scaled relative to those of the reference inverter.

\[ R_{\text{PDEFF}} = \frac{R_{\text{PDREF}}}{\text{OD}_{\text{HL}}} \quad \text{and} \quad R_{\text{PUEFF}} = \frac{R_{\text{PUREF}}}{\text{OD}_{\text{LH}}} \]

If inverter sized for equal rise/fall, \( \text{OD}_{\text{HL}} = \text{OD}_{\text{LH}} = \text{OD} \)

\[ t_{\text{HL}} = t_{\text{LH}} = \frac{R_{\text{PDREF}}}{\text{OD}} \quad C_{\text{L}} = R_{\text{PDREF}} C_{\text{REF}} \frac{F_{\text{IL}}}{\text{OD}} \]

\[ t_{\text{PROP}} = t_{\text{LH}} + t_{\text{HL}} = t_{\text{REF}} \frac{F_{\text{IL}}}{\text{OD}} \]

\( \text{OD} \) may be larger or smaller than 1
Recall

Propagation Delay in Multiple-Levels of Logic with Stage Loading

Overdrive

\[ V_{\text{IN}} \xrightarrow{} V_{\text{OUT}} \]

\[ C_L \]

\[ t_{\text{PROP}} = t_{\text{HL}} + t_{\text{LL}} = t_{\text{REF}} \frac{F_{\text{IL}}}{OD} \]

If inverter is not equal rise/fall

\[ t_{\text{HL}} = \frac{R_{\text{PDREF}}}{OD_{\text{HL}}} C_L = \frac{1}{2} t_{\text{REF}} \frac{F_{\text{IL}}}{OD_{\text{HL}}} \]

\[ t_{\text{LL}} = \frac{R_{\text{PUREF}}}{OD_{\text{LL}}} C_L = \frac{1}{2} t_{\text{REF}} \frac{F_{\text{IL}}}{OD_{\text{LL}}} \]

\[ t_{\text{PROP}} = t_{\text{HL}} + t_{\text{LL}} = \frac{1}{2} t_{\text{REF}} F_{\text{IL}} \left( \frac{1}{OD_{\text{HL}}} + \frac{1}{OD_{\text{LL}}} \right) \]
Driving Large Capacitive Loads

Example

Assume driving by a reference inverter

Assume $C_L = 1000C_{REF}$

$t_{PROP} = ?$

In 0.5u proc $t_{REF} = 20\text{ps}$,
$C_{REF} = 4\text{fF}, R_{PDREF} = 2.5\text{K}$
Driving Large Capacitive Loads

Example

Assume driving by a reference inverter

Assume $C_L = 1000C_{REF}$

$t_{PROP} = 1000 t_{REF}$

t_{PROP} is too long!

In 0.5u proc $t_{REF} = 20ps$, $C_{REF} = 4fF, RPDREF = 2.5K$
Driving Large Capacitive Loads

Example

Assume first stage is a reference inverter

Assume \( C_L = 1000C_{REF} \)

\[
\begin{align*}
t_{PROP} &= \text{?} \\
t_{PROP} &= t_{REF} \sum_{k=1}^{2} \frac{F_{I(k+1)}}{O_{D_k}} \\
t_{PROP} &= t_{REF} \left( \frac{1}{1000} + \frac{1}{1000} \right) = t_{REF} \cdot 1000 + 1 \\
t_{PROP} &= t_{REF} \cdot 1001
\end{align*}
\]

Delay of second inverter is really small but overall delay is even longer than before!
Driving Large Capacitive Loads

Example

Assume first stage is a reference inverter

Assume \( C_L = 1000C_{REF} \)

\[
I(k+1) = PROP REF_{k=1} t_{OD} = t_{OD}
\]

\[
I(k+1) = PROP REF_{k=1} t_{OD} = t_{OD}
\]

\[
t_{PROP} = t_{REF} \sum_{k=1}^{3} \frac{F_{I(k+1)}}{OD_k}
\]

\[
t_{PROP} = t_{REF} \left( \frac{1}{10} + \frac{1}{100} + \frac{1}{1000} \right) = t_{REF} 10 + 10 + 10
\]

\[
t_{PROP} = 30t_{REF}
\]

Dramatic reduction is propagation delay (over a factor of 30!)

What is the fastest way to drive a large capacitive load?
Optimal Driving of Capacitive Loads

Assume first stage is a reference inverter

Need to determine the number of stages, \( n \), and the OD factors for each stage to minimize \( t_{\text{PROP}} \).

\[
t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^{n} \frac{F_{I(k+1)}}{OD_k}
\]

where \( \theta_0 = 1, \theta_n = C_L/C_{\text{REF}} \)

This becomes an \( n \)-parameter optimization (minimization) problem!

Unknown parameters: \( \{\theta_1, \theta_2, \ldots, \theta_{n-1}, n\} \)
Optimal Driving of Capacitive Loads

Assume first stage is a reference inverter

Order reduction strategy: Assume overdrive of stages increases by the same factor clear until the load

This becomes a 2-parameter optimization (minimization) problem!

Unknown parameters: \( \theta, n \)

One constraint: \( \theta^n C_{REF} = C_L \)
Optimal Driving of Capacitive Loads

\[ t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^{n} \frac{\theta_k}{\theta_{k-1}} \]

\[ t_{\text{PROP}} = t_{\text{REF}} n \theta \]

Unknown parameters: \( \theta, n \)

Thus obtain an expression for \( t_{\text{PROP}} \) in terms of only \( \theta \)

\[ t_{\text{PROP}} = t_{\text{REF}} \frac{\theta}{\ln \theta} \left[ \ln \frac{C_L}{C_{\text{REF}}} \right] \]

\[ \theta^n C_{\text{REF}} = C_L \]
Optimal Driving of Capacitive Loads

\[ t_{\text{PROP}} = t_{\text{REF}} \frac{\theta}{\ln \theta} \left[ \ln \frac{C_L}{C_{\text{REF}}} \right] \]

Is suffices to minimize the function

\[ f(\theta) = \frac{\theta}{\ln \theta} \]

\[ \frac{df}{d\theta} = \frac{\ln \theta - \theta \cdot \left( \frac{1}{\theta} \right)}{\ln \theta^2} = 0 \]

\[ \ln \theta - 1 = 0 \quad \rightarrow \quad \theta = e \]

\[ n = \frac{1}{\ln \theta} \ln \left( \frac{C_L}{C_{\text{REF}}} \right) \quad \rightarrow \quad n = \ln \left( \frac{C_L}{C_{\text{REF}}} \right) \]
Optimal Driving of Capacitive Loads

\[ \theta_{\text{OPT}} = e \]

\[ n_{\text{OPT}} = \ln \left( \frac{C_L}{C_{\text{REF}}} \right) \]

\[ t_{\text{PROP}} = t_{\text{REF}} \frac{\theta}{\ln \theta} \left[ \ln \frac{C_L}{C_{\text{REF}}} \right] \]

\[ t_{\text{PROP}} = t_{\text{REF}} e \left[ \ln \frac{C_L}{C_{\text{REF}}} \right] = n\theta t_{\text{REF}} \]

\[ \theta^n C_{\text{REF}} = C_L \]
Optimal Driving of Capacitive Loads

\[ f = \frac{\theta}{\ln \theta} \]

minimum at \( \theta = e \) but shallow inflection point for \( 2 < \theta < 3 \)

practically pick \( \theta = 2, \theta = 2.5, \) or \( \theta = 3 \)

since optimization may provide non-integer for \( n \), must pick close integer
Optimal Driving of Capacitive Loads

- Often termed a pad driver
- Often used to drive large internal busses as well
- Generally included in standard cells or in cell library
- Device sizes can become very large
- Odd number of stages will cause signal inversion but usually not a problem
Optimal Driving of Capacitive Loads

Example: Design a pad driver for driving a load capacitance of 10pF, determine $t_{\text{PROP}}$ for the pad driver, and compare this with the propagation delay for driving the pad with a minimum-sized reference inverter.

In 0.5µm proc, $t_{\text{REF}}=20\text{ps}$, $C_{\text{REF}}=4\text{fF}$, $R_{\text{PDREF}}=2.5\text{K}

$$n_{\text{OPT}} = \ln \left( \frac{C_L}{C_{\text{REF}}} \right) = \ln \left( \frac{10\text{pF}}{4\text{fF}} \right) = 7.8$$

Select $n=8$, $\theta=2.5$

$$W_{nk} = 2.5^{k-1}, \quad W_{pk} = 3 \cdot 2.5^{k-1}$$
Optimal Driving of Capacitive Loads

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In 0.5μm process $t_{\text{REF}}=20\text{ps}$, $C_{\text{REF}}=4\text{fF}, R_{\text{PDREF}}=2.5\text{K}$, $W_{nk}=2.5^{k-1}, \quad W_{pk} = 3 \cdot 2.5^{k-1}$

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Note devices in last stage are very large!
Optimal Driving of Capacitive Loads

Example: Design a pad driver for driving a load capacitance of 10pF, determine $t_{PROP}$ for the pad driver, and compare this with the propagation delay for driving the pad with a minimum-sized reference inverter.

In 0.5u proc $t_{REF}=20\text{ps}$, $C_{REF}=4\text{fF}, R_{PDREF}=2.5\Omega$

$W_{nk}=2.5^{k-1}$, $W_{pk} = 3 \cdot 2.5^{k-1}$

$t_{PROP} \approx n\theta t_{REF} = 8 \cdot 2.5 \cdot t_{REF} = 20t_{REF}$

More accurately:

$$t_{PROP} = t_{REF} \left( \sum_{k=1}^{7} \theta + \frac{1}{\theta^{7}} \frac{C_{L}}{C_{REF}} \right) = t_{REF} \left( 17.5 + \frac{1}{610} \cdot \frac{2500}{2500} \right) = 21.6t_{REF}$$
Optimal Driving of Capacitive Loads

Example: Design a pad driver for driving a load capacitance of 10pF, determine \( t_{\text{PROP}} \) for the pad driver, and compare this with the propagation delay for driving the pad with a minimum-sized reference inverter.

In 0.5\( \mu \)m process, \( t_{\text{REF}} = 20\,\text{ps}, C_{\text{REF}} = 4\,\text{fF}, R_{\text{PDREF}} = 2.5\,\text{K} \)

\[ W_{nk} = 2.5^{k-1}, \quad W_{pk} = 3 \cdot 2.5^{k-1} \]

If driven directly with the minimum-sized reference inverter

\[ t_{\text{PROP}} = t_{\text{REF}} \frac{C_L}{C_{\text{REF}}} = 2500 t_{\text{REF}} \]

Note an improvement in speed by a factor of

\[ r = \frac{2500}{20} = 125 \]
Optimal Driving of Capacitive Loads

Example: Design a pad driver for driving a load capacitance of 10pF, determine $t_{\text{PROP}}$ for the pad driver, and compare this with the propagation delay for driving the pad with a minimum-sized reference inverter.

In 0.5u proc, $t_{\text{REF}}=20\text{ps}$, $C_{\text{REF}}=4\text{fF}, R_{\text{PDREF}}=2.5\text{K}

$W_{nk}=2.5^{k-1}$, $W_{pk} = 3 \cdot 2.5^{k-1}$

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