Digital Circuits

- Device Sizing
- Propagation Delay With Multiple Levels of Logic
- Overdrive
- Driving Large Capacitive Load
## Device Sizing

Assume $V_{Tn} = 0.2V_{DD}$, $V_{Tp} = -0.2V_{DD}$, $\mu_n/\mu_p = 3$, $L_1 = L_2 = L_{\text{min}}$

### Sizing Strategy Summary

<table>
<thead>
<tr>
<th></th>
<th>Minimum Size</th>
<th>$V_{TRIP} = V_{DD}/2$</th>
<th>Equal Rise/Fall</th>
</tr>
</thead>
</table>
| Size | $W_n = W_p = W_{\text{min}}$
$L_p = L_n = L_{\text{min}}$ | $W_n = W_{\text{min}}$
$W_p = 3W_{\text{min}}$
$L_p = L_n = L_{\text{min}}$ | $W_n = W_{\text{min}}$
$W_p = 3W_{\text{min}}$
$L_p = L_n = L_{\text{min}}$ |
| $t_{HL}$ | $R_{pd}C_L$ | $R_{pd}C_L$ | $R_{pd}C_L$ |
| $t_{LH}$ | $3R_{pd}C_L$ | $R_{pd}C_L$ | $R_{pd}C_L$ |
| $t_{PROP}$ | $4R_{pd}C_L$ | $2R_{pd}C_L$ | $2R_{pd}C_L$ |
| $V_{\text{trip}}$ | $V_{TRIP} = 0.42V_{DD}$ | $V_{TRIP} = 0.5V_{DD}$ | $V_{TRIP} = 0.5V_{DD}$ |

- For a fixed load $C_L$, the minimum-sized structure has a higher $t_{PROP}$ but if the load is another inverter, $C_L$ will also change so the speed improvements become less apparent.
- This will be investigated later.

---

Review from Last Time

- [Diagram of circuit with labels: $V_{DD}$, $V_{IN}$, $V_{OUT}$, $C_L$, $M_1$, $M_2$]
The Reference Inverter

Assume $\mu_n/\mu_p=3$

$W_n=W_{\text{MIN}}$, $W_p=3W_{\text{MIN}}$

$L_n=L_p=L_{\text{MIN}}$

In 0.5μ proc $t_{\text{REF}}=20\text{ps}$, $C_{\text{REF}}=4\text{fF}$, $R_{\text{PDREF}}=2.5\text{K}$

(Note: This $C_{\text{OX}}$ is somewhat larger than that in the 0.5μ ON process)
Propagation Delay

How does the propagation delay compare for a minimum-sized strategy to that of an equal rise/fall sizing strategy?

Minimum Sized

\[ W_2 = W_1 = W_{MIN} \]

\[ t_{PROP} = t_{REF} \]

Reference Inverter

\[ W_2 = \left( \frac{\mu_n}{\mu_p} \right) W_1, \quad W_1 = W_{MIN} \]

\[ t_{PROP} = t_{REF} \]

They are the same!

Even though the \( t_{LH} \) rise time has been reduced with the equal rise/fall sizing strategy, this was done at the expense of an increase in the total load capacitance that resulted in no net change in propagation delay!
Device Sizing

Equal Worse-Case Rise/Fall Device Sizing Strategy
-- (same as $V_{TRIP}=V_{DD}/2$ for worst case delay in typical process considered in example)

Assume $\mu_n/\mu_p=3$
$L_n=L_p=L_{MIN}$

$W_n=W_{MIN}$, $W_p=3W_{MIN}$
$C_{IN}=C_{REF}$
$F_{I}=1$

INV

$k$-input NOR
$W_n=W_{MIN}$, $W_p=3kW_{MIN}$
$C_{IN}=\left(\frac{3k+1}{4}\right)C_{REF}$
$F_{I}=\left(\frac{3k+1}{4}\right)$

$k$-input NAND
$W_n=kW_{MIN}$, $W_p=3W_{MIN}$
$C_{IN}=\left(\frac{3+k}{4}\right)C_{REF}$
$F_{I}=\left(\frac{3+k}{4}\right)$
Device Sizing – minimum size driving $C_{REF}$

**INV**

$$ t_{PROP} = \frac{3}{2} t_{REF} $$

$$ t_{PROP} = \frac{3}{2} t_{REF} + \frac{1}{2} t_{REF} $$

$$ t_{PROP} = 2 t_{REF} $$

$$ F_{I} = \frac{C_{REF}}{2} $$

$$ R_{PU} = R_{PD} = R_{PDREF} $$

**$k$-input NOR**

$$ t_{PROP} = \frac{3}{2} t_{REF} + \frac{k}{2} t_{REF} $$

$$ t_{PROP} = \left( \frac{3k + 1}{2} \right) t_{REF} $$

$$ F_{I} = \frac{C_{REF}}{2} $$

$$ R_{PD} = R_{PDREF} $$

$$ R_{PU} = 3k R_{PDREF} $$

**$k$-input NAND**

$$ t_{PROP} = \frac{3}{2} t_{REF} + \frac{k}{2} t_{REF} $$

$$ t_{PROP} = \frac{3 + k}{2} t_{REF} $$

$$ F_{I} = \frac{C_{REF}}{2} $$

$$ R_{PD} = 3 R_{PDREF} $$

$$ R_{PU} = 3 R_{PDREF} $$

**Review from Last Time**
Review from Last Time

Device Sizing – minimum size driving \( C_{\text{REF}} \)

**INV**

\[ t_{\text{PROP}} = \frac{3}{2} t_{\text{REF}} \]

\[ t_{\text{PROP}} = 0.5 t_{\text{REF}} + \frac{3}{2} t_{\text{REF}} \]

\[ t_{\text{PROP}} = 2 t_{\text{REF}} \]

\[ \text{FI} = \frac{C_{\text{REF}}}{2} \]

\[ R_{\text{PU}} = R_{\text{PD}} = R_{\text{PDREF}} \]

**k-input NOR**

\[ t_{\text{PROP}} = \frac{3k + 1}{2} t_{\text{REF}} \]

\[ t_{\text{PROP}} = 0.5 t_{\text{REF}} + \frac{3k}{2} t_{\text{REF}} \]

\[ t_{\text{PROP}} = 2 t_{\text{REF}} \]

\[ \text{FI} = \frac{C_{\text{REF}}}{2} \]

\[ R_{\text{PD}} = R_{\text{PDREF}} \quad R_{\text{PU}} = 3k R_{\text{PDREF}} \]

**k-input NAND**

\[ t_{\text{PROP}} = \frac{3}{2} t_{\text{REF}} + \frac{k}{2} t_{\text{REF}} \]

\[ t_{\text{PROP}} = 0.5 t_{\text{REF}} + \frac{3k}{2} t_{\text{REF}} \]

\[ t_{\text{PROP}} = 2 t_{\text{REF}} \]

\[ \text{FI} = \frac{C_{\text{REF}}}{2} \]

\[ R_{\text{PD}} = 3 R_{\text{PDREF}} \quad R_{\text{PU}} = 3k R_{\text{PDREF}} \]
Review from Last Time

Device Sizing – minimum size driving $C_{REF}$

**INV**

$P_{PROP} = ?$

\[ t_{PROP} = 0.5t_{REF} + \frac{3}{2}t_{REF} \]

\[ t_{PROP} = 2t_{REF} \]

$F_I = \frac{C_{REF}}{2}$

$R_{PU} = R_{PD} = R_{PDREF}$

**k-input NOR**

$P_{PROP} = ?$

\[ t_{PROP} = 0.5t_{REF} + \frac{3k}{2}t_{REF} \]

\[ t_{PROP} = \left(\frac{3k+1}{2}\right)t_{REF} \]

$F_I = \frac{C_{REF}}{2}$

$R_{PD} = R_{PDREF}$  $R_{PU} = 3kR_{PDREF}$

**k-input NAND**

$P_{PROP} = ?$

\[ t_{PROP} = \frac{3}{2}t_{REF} + \frac{k}{2}t_{REF} \]

\[ t_{PROP} = \frac{3 + k}{2}t_{REF} \]

$F_I = \frac{C_{REF}}{2}$

$R_{PD} = 3R_{PDREF}$  $R_{PU} = 3R_{PDREF}$
Review from Last Time

Propagation Delay in Multiple-Levels of Logic with Stage Loading

Assume all gates sized for equal worst-case rise/fall times

For n levels of logic between A and F

\[ t_{PROP} = \sum_{k=1}^{n} t_{PROP}(k) \]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Analysis strategy: Express delays in terms of those of reference inverter

**Reference Inverter**

$C_{REF} = C_{IN} = 4C_{OX} W_{MIN} L_{MIN}$

$F_I = 1$

$R_{PDREF} = \frac{L_{MIN}}{\mu_n C_{OX} W_{MIN} (V_{DD} - V_{Tn})} = \frac{L_{MIN}}{\mu_n C_{OX} W_{MIN} (0.8V_{DD})}$

$t_{REF} = t_{HLREF} + t_{LHREF} = 2R_{PDREF} C_{REF}$

$L_n = L_p = L_{MIN}$

Assume $\mu_n/\mu_p = 3$

$W_n = W_{MIN}, \quad W_p = 3W_{MIN}$

In 0.5u proc $t_{REF} = 20ps, \quad C_{REF} = 4fF, R_{PDREF} = 2.5K$

(Note: This $C_{OX}$ is somewhat larger than that in the 0.5u ON process)
Propagation Delay in Multiple-Levels of Logic with Stage Loading

What loading will a gate see?

- Input capacitance to other gates
- Any load capacitors
- Parasitic interconnect capacitances

Assume:
- all gates sized for equal worst-case rise/fall times
- all gates sized to have rise and fall times equal to that of ref inverter when driving $C_{REF}$

Observe:
- Propagation delay of these gates will be scaled by the ratio of the total load capacitance on each gate to $C_{REF}$
Propagation Delay with Stage Loading

\[ t_{\text{REF}} = 2R_{\text{PDref}} C_{\text{REF}} \]

\[ C_{\text{REF}} = 4C_{\text{OX}} W_{\text{MIN}} L_{\text{MIN}} \]

Fl of a capacitor

Fl of a gate (input k)

Fl of an interconnect

Overall Fl

Fl can be expressed either in units of capacitance or normalized to \( C_{\text{REF}} \)

Most commonly Fl is normalized but must determine from context

If gates sized to have same drive as ref inverter

\[ t_{\text{prop-k}} = t_{\text{REF}} \cdot \text{Fl}_{\text{LOAD}} \]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Example

Assume all gates sized for equal worst-case rise/fall times

Assume all gate drives are the same as that of reference inverter

Neglect interconnect capacitance, assume load of $10C_{\text{REF}}$ on F output

**Determine propagation delay from A to F**
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Assume all gates sized for equal worst-case rise/fall times
Assume all gate drives are the same as that of reference inverter
Neglect interconnect capacitance, assume load of $10C_{\text{REF}}$ on F output

Determine propagation delay from A to F

What loading will a gate see?

Derivation:

\[
F_{I_2} = \frac{6}{4}C_{\text{REF}} \quad F_{I_3} = C_{\text{REF}} + \frac{7}{4}C_{\text{REF}} \quad F_{I_4} = \frac{7}{4}C_{\text{REF}} + \frac{13}{4}C_{\text{REF}} \quad F_{I_{\text{LOAD}}} = F_{I_5} = 10C_{\text{REF}}
\]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Example

Assume all gates sized for equal worst-case rise/fall times
Assume all gate drives are the same as that of reference inverter
Neglect interconnect capacitance, assume load of $10C_{\text{REF}}$ on F output

Determine propagation delay from A to F

DERIVATIONS

$F_{l2} = \frac{6}{4} C_{\text{REF}}$

$t_{\text{PROP1}} = \frac{6}{4} t_{\text{REF}}$

$F_{l3} = C_{\text{REF}} + \frac{7}{4} C_{\text{REF}}$

$t_{\text{PROP2}} = \left(1 + \frac{7}{4}\right) t_{\text{REF}}$

$F_{l4} = \frac{7}{4} C_{\text{REF}} + \frac{13}{4} C_{\text{REF}}$

$t_{\text{PROP3}} = \left(\frac{7}{4} + \frac{13}{4}\right) t_{\text{REF}}$

$F_{l5} = 10C_{\text{REF}}$

$t_{\text{PROP4}} = 10t_{\text{REF}}$

$t_{\text{PROP}} = \sum_{k=1}^{n} t_{\text{PROP}_k} = t_{\text{REF}} \sum_{k=1}^{n} F_{l(k+1)} = t_{\text{REF}} \left(\frac{6}{4} + \frac{11}{4} + \frac{20}{4} + 10\right) = t_{\text{REF}} (19.25)$
Propagation Delay Through Multiple Stages of Logic with Stage Loading
(assuming gate drives are all same as that of reference inverter)

Identify the gate path from A to F

\[ t_{PROP_k} = t_{REF} F_{I(k+1)} \]

Propagation delay from A to F:

\[ t_{PROP} = t_{REF} \sum_{k=1}^{n} F_{I(k+1)} \]

This approach is analytically manageable, provides modest accuracy and is “faithful”
Digital Circuit Design

- Hierarchical Design
- Basic Logic Gates
- Properties of Logic Families
- Characterization of CMOS Inverter
- Static CMOS Logic Gates
  - Ratio Logic
- Propagation Delay
  - Simple analytical models
  - Elmore Delay
- Sizing of Gates
- Propagation Delay with Multiple Levels of Logic
- Optimal driving of Large Capacitive Loads
- Power Dissipation in Logic Circuits
- Other Logic Styles
- Array Logic
- Ring Oscillators

- done
- partial
What if the propagation delay is too long (or too short)?

Propagation delay from A to F:

\[ t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^{n} F_{I(k+1)} \]

\[ t_{\text{PROP}_k} = t_{\text{REF}} F_{I(k+1)} \]
Recall:

Multiple Input Gates:

2-input NOR

2-input NAND

k-input NOR

k-input NAND

Equal Worst Case Rise/Fall

\( W_n = ? \)

\( W_p = ? \)

Fastest response \((t_{HL} \text{ or } t_{LH}) = ?\)

Worst case response \((t_{PROP}, \text{ usually of most interest})?\)

Input capacitance \((F_I) = ?\)

Minimum Sized \((\text{assume driving a load of } C_{REF})\)

\( W_n = W_{\text{min}} \)

\( W_p = W_{\text{min}} \)

Fastest response \((t_{HL} \text{ or } t_{LH}) = ?\)

Slowest response \((t_{HL} \text{ or } t_{LH}) = ?\)

Worst case response \((t_{PROP}, \text{ usually of most interest})?\)

Input capacitance \((F_I) = ?\)

(and equal to that of ref inverter when driving \( C_{REF} \))

consider the fine print!
Device Sizing

Multiple Input Gates: **2-input NOR**

- Equal Worst Case Rise/Fall
  - (and equal to that of ref inverter when driving $C_{REF}$)

*(n-channel devices sized same, p-channel devices sized the same)*

Assume $L_n = L_p = L_{min}$ and driving a load of $C_{REF}$

- $W_n = ?$
- $W_p = ?$
- Input capacitance = ?
- $F_I = ?$
- $t_{PROP} = ?$ (worst case)

Recall:

One degree of freedom was used to satisfy the constraint indicated

Other degree of freedom was used to achieve equal rise and fall times

- $W_n = W_{MIN}$
- $W_p = 6W_{MIN}$

\[
F_I = \left(\frac{7}{4}\right)C_{REF} \quad \text{or} \quad F_I = \frac{7}{4}
\]

\[
t_{PROP} = t_{REF} \quad \text{(worst case)}
\]
Example: Determine $t_{\text{prop}}$ in 0.5u process if $C=10\,\text{pF}$

\[
t_{\text{prop}} = t_{\text{REF}} \cdot F_1 = t_{\text{REF}} \cdot \frac{10\,\text{pF}}{4\,\text{fF}} = t_{\text{REF}} \cdot 2500
\]

\[
t_{\text{prop}} = t_{\text{REF}} \cdot 2500 = 50\,\text{nsec}
\]

Note this is unacceptably long!
Scaling widths of ALL devices by constant \( W_{\text{scaled}} = W \times \text{OD} \) will change “drive” capability relative to that of the reference inverter but not change relative value of \( t_{HL} \) and \( t_{LH} \)

\[
R_{PD} = \frac{L_1}{\mu_n C_{OX} W_1 (V_{DD} - V_{Tn})}
\]

\[
R_{PDOD} = \frac{L_1}{\mu_n C_{OX} [\text{OD} \cdot W_1] (V_{DD} - V_{Tn})} = \frac{R_{PD}}{\text{OD}}
\]

\[
R_{PU} = \frac{L_2}{\mu_p C_{OX} W_2 (V_{DD} + V_{Tp})}
\]

\[
R_{PUOD} = \frac{L_2}{\mu_p C_{OX} [\text{OD} \cdot W_2] (V_{DD} + V_{Tp})} = \frac{R_{PU}}{\text{OD}}
\]

Scaling widths of ALL devices by constant will change \( F_i \) by \( \text{OD} \)

\[
C_{IN} = C_{OX} (W_1 L_1 + W_2 L_2)
\]

\[
C_{INOD} = C_{OX} \left([\text{OD} \cdot W_1] L_1 + [\text{OD} \cdot W_2] L_2\right) = \text{OD} \cdot C_{IN}
\]
Overdrive Factors

- The factor by which the devices are W/L scaled above those of the reference inverter is termed the overdrive factor, OD

- Scaling widths by overdrive factor DECREASES resistance by same factor

- Scaling all widths by a constant does not compromise the symmetry between the rise and fall times

- Judicious use of overdrive can dramatically improve the speed of digital circuits

- Large overdrive factors are often used

- Scaling widths by overdrive factor INCREASES input capacitance by same factor
Define the Asymmetric Overdrive Factors of the stage to be the factor by which PU and PD resistors are scaled relative to those of the reference inverter.

\[ R_{PDEFF} = \frac{R_{PDREF}}{OD_{HL}} \quad R_{PUEFF} = \frac{R_{PUREF}}{OD_{LH}} \]

If inverter sized for equal rise/fall, define OD by \( OD_{HL}=OD_{LH}=OD \)

\[ t_{HL} = t_{LH} = \frac{R_{PDREF}C_L}{OD} = R_{PDREF}C_{REF} \frac{F_{IL}}{OD} \]

\[ t_{PROP} = t_{LH} + t_{HL} = t_{REF} \frac{F_{IL}}{OD} \]

OD may be larger or smaller than 1
Propagation Delay with Over-drive Capability

Example

Compare the propagation delays. Assume the OD is 900 in the third case and 30 in the fourth case. Don’t worry about the extra inversion at this time.

Note: Dramatic reduction in $t_{\text{PROP}}$ is possible
Will later determine what optimal number of stages and sizing is
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Summary: Propagation delay from A to F:

\[ t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^{n} \frac{F_{l(k+1)}}{OD_k} \]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

*Will consider an example with the five cases*

- Equal rise/fall (no overdrive)
- Equal rise/fall with overdrive
- Minimum Sized
- Asymmetric Overdrive
- Combination of equal rise/fall, minimum size and overdrive

*Will develop the analysis methods as needed*
Propagation Delay in Multiple-Levels of Logic with Stage Loading

- Equal rise/fall (no overdrive)
- Equal rise/fall with overdrive
- Minimum Sized
- Asymmetric overdrive
- Combination of equal rise/fall, minimum size and overdrive

\[
t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^{n} F_{l(k+1)}
\]

\[
t_{\text{PROP}} = t_{\text{REF}} \frac{\sum_{k=1}^{n} F_{l(k+1)}}{\text{OD}_k}
\]

\[
t_{\text{PROP}} = ?
\]

\[
t_{\text{PROP}} = ?
\]

\[
t_{\text{PROP}} = ?
\]
Driving Notation

- Equal rise/fall (no overdrive)
- Equal rise/fall with overdrive
- Minimum Sized
- Asymmetric Overdrive

Notation will be used only if it is not clear from the context what sizing is being used.
Recall:

Define the Asymmetric Overdrive Factors of the stage to be the factors by which PU and PD resistors are scaled relative to those of the reference inverter.

\[ R_{PDEFF} = \frac{R_{PDREF}}{OD_{HL}} \quad \quad R_{PUEFF} = \frac{R_{PUREF}}{OD_{LH}} \]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Asymmetric Overdrive

If inverter is not equal rise/fall

\[
\begin{align*}
    t_{\text{HL}} &= \frac{R_{\text{PDREF}}}{\text{OD}_{\text{HL}}} C_L, \\
    t_{\text{LH}} &= \frac{R_{\text{PUREF}}}{\text{OD}_{\text{LH}}} C_L, \\
    t_{\text{PROP}} &= t_{\text{HL}} + t_{\text{LH}} = \frac{t_{\text{REF}} F_{\text{IL}}}{\text{OD}} \\
    &\quad \left( \frac{1}{\text{OD}_{\text{HL}}} + \frac{1}{\text{OD}_{\text{LH}}} \right)
\end{align*}
\]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Asymmetric Overdrive

\[ t_{\text{PROP}} = t_{\text{HL}} + t_{\text{LH}} = \frac{1}{2} t_{\text{REF}} F_{\text{IL}} \left( \frac{1}{OD_{\text{HL}}} + \frac{1}{OD_{\text{LH}}} \right) \]

When propagating through \( n \) stages:

\[ t_{\text{PROP}} = t_{\text{REF}} \cdot \left( \frac{1}{2} \sum_{k=1}^{n} F_{i(k+1)} \left( \frac{1}{OD_{\text{HL}k}} + \frac{1}{OD_{\text{LH}k}} \right) \right) \]

\( F_{ik} \) denotes the total loading on stage \( k \) which is the sum of the \( F_i \) of all loading on stage \( k \)
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Overdrive Notation

Equal Rise/Fall with overdrive OD

Examples

Equal Rise/Fall with overdrive of 8

Rise/Fall may be different with overdrive OD\(_{HL}\) and OD\(_{LH}\)

If \(W_n = W_{\text{MIN}}\), minimum sized inverter
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Equal rise-fall gates, no overdrive

In 0.5u proc  $t_{REF}=20ps$, $C_{REF}=4fF$, $R_{PDREF}=2.5K$

$t_{REF}=2t_{HL_{REF}}$

$t_{PROP}=t_{REF} \sum_{k=1}^{n} F_{k+1}$
Propagation Delay in Multiple-Levels of Logic with Stage Loading

**Equal rise-fall gates, no overdrive**

<table>
<thead>
<tr>
<th>Operation</th>
<th>C_{IN}/C_{REF}</th>
<th>( t_{PROP}/t_{REF} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inverter</td>
<td>1/1</td>
<td>( \sum_{k=1}^{n} F_{f(k+1)} )</td>
</tr>
<tr>
<td>NOR</td>
<td>3k+1/4</td>
<td>( \sum_{k=1}^{n} F_{f(k+1)} )</td>
</tr>
<tr>
<td>NAND</td>
<td>3+k/4</td>
<td>( \sum_{k=1}^{n} F_{f(k+1)} )</td>
</tr>
<tr>
<td>Overdrive</td>
<td>( t = t_F )</td>
<td>( t_{PROP} = t_{REF} \sum_{k=1}^{5} F_{k+1} )</td>
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</tbody>
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<td></td>
</tr>
</tbody>
</table>

\( t_{PROP} = t_{REF} \sum_{k=1}^{5} F_{k+1} \)
Equal rise-fall gates, no overdrive

In 0.5u proc \( t_{REF} = 20 \text{ps} \),
\( C_{REF} = 4fF \), \( R_{PDREF} = 2.5K \)

(Note: This \( C_{OX} \) is somewhat larger than that in the 0.5u ON process)

\[ t_{PROP} = t_{REF} \sum_{k=1}^{5} F_{k+1} \]

\[ t_{PROP} = t_{REF} (10.25 + 4.25 + 4.25 + 1.25 + 12.5) \]

\[ t_{PROP} = 32.5t_{REF} \]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Equal rise-fall gates, with overdrive

In 0.5u proc $t_{REF}=20\text{ps}$, $C_{REF}=4\text{fF}, R_{PDREF}=2.5\text{K}$

(Note: This $C_{OX}$ is somewhat larger than that in the 0.5u ON process)
## Propagation Delay in Multiple-Levels of Logic with Stage Loading

**Equal rise-fall gates, with overdrive**

<table>
<thead>
<tr>
<th>C&lt;sub&gt;IN&lt;/sub&gt;/C&lt;sub&gt;REF&lt;/sub&gt;</th>
<th>Equal Rise/Fall</th>
<th>Equal Rise/Fall (with OD)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inverter</td>
<td>1</td>
<td>OD</td>
</tr>
<tr>
<td>NOR</td>
<td>(\frac{3k+1}{4})</td>
<td>(\frac{3k+1}{4}) • OD</td>
</tr>
<tr>
<td>NAND</td>
<td>(\frac{3+k}{4})</td>
<td>(\frac{3+k}{4}) • OD</td>
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Overdrive

<table>
<thead>
<tr>
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<tbody>
<tr>
<td></td>
<td>HL</td>
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<td>1</td>
<td>1</td>
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</tr>
</tbody>
</table>

NOR

<table>
<thead>
<tr>
<th></th>
<th>HL</th>
<th>LH</th>
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<th>LH</th>
</tr>
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<tbody>
<tr>
<td></td>
<td>1</td>
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NAND

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<tr>
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<tr>
<td></td>
<td>1</td>
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</table>

\[ t_{PROP} = t_{REF} \sum_{k=1}^{n} \frac{F_{k+1}}{OD_k} \]
Equal rise-fall gates, with overdrive

\[
\begin{align*}
\text{In 0.5u proc } & t_{REF} = 20\text{ps, } \\
& C_{REF} = 4fF, R_{PDREF} = 2.5K
\end{align*}
\]

(Note: This \(C_{OX}\) is somewhat larger than that in the 0.5u ON process)
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Minimum-sized gates

In 0.5u proc \( t_{REF}=20\text{ps} \), \( C_{REF}=4\text{fF}, R_{PDREF}=2.5\text{K} \)

(Note: This \( C_{OX} \) is somewhat larger than that in the 0.5u ON process)
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Minimum-sized gates

\[ t_{\text{PROP}} = t_{\text{REF}} \cdot ? \]
Propagation Delay with Minimum-Sized Gates

\[ t_{\text{PROP}} = t_{\text{REF}} \cdot \text{?} \]

\[ t_{\text{PROP}} = R_{\text{PD}}C_L + R_{\text{PU}}C_L \]

\[ t_{\text{PROP}} = \left( \frac{R_{\text{PDREF}}}{OD_{HL}} + \frac{R_{\text{PDREF}}}{OD_{LH}} \right)C_L \]

\[ t_{\text{PROP}} = R_{\text{PDREF}} \left( \frac{1}{OD_{HL}} + \frac{1}{OD_{LH}} \right) \left( C_{\text{REF}}F_L \right) \]

\[ t_{\text{PROP}} = \left( \frac{1}{OD_{HL}} + \frac{1}{OD_{LH}} \right) \left( R_{\text{PDREF}}C_{\text{REF}} \right) F_I \]

But recall

\[ t_{\text{REF}} = 2C_{\text{REF}}R_{\text{PDREF}} \]

Thus

\[ t_{\text{PROP}} = \left( \frac{1}{OD_{HL}} + \frac{1}{OD_{LH}} \right) \left( \frac{t_{\text{REF}}}{2} \right) F_I \]

Now, for k levels of logic

\[ t_{\text{PROP}} = \frac{t_{\text{REF}}}{2} \sum_{k=1}^{n} F_{l(k+1)} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \]

\[ t_{\text{PROP}} = t_{\text{REF}} \left( \frac{1}{2} \sum_{k=1}^{n} F_{l(k+1)} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right) \]
Propagation Delay with Minimum-Sized Gates

\[ t_{PROP} = t_{REF} \cdot \left( \frac{1}{2} \sum_{k=1}^{n} F_{I(k+1)} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right) \]

Still need OD_{HL} and OD_{LH}

Still need F_{I}
Propagation Delay with minimum-sized gates

\[ \text{OD}_{HL} = ? \]
\[ \text{OD}_{HL} = 1 \]
\[ \text{OD}_{LH} = ? \]
\[ \text{OD}_{LH} = \frac{1}{3k} \]

\[ \text{OD}_{HL} = ? \]
\[ \text{OD}_{HL} = 1/k \]
\[ \text{OD}_{LH} = ? \]
\[ \text{OD}_{LH} = \frac{1}{3} \]

\[ F_I = 2C_{OX}W_{MIN}L_{MIN} \]
\[ C_{REF} = 4C_{OX}W_{MIN}L_{MIN} \]
\[ F_I = \frac{C_{REF}}{2} \]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Minimum-sized gates

<table>
<thead>
<tr>
<th>C_{IN}/C_{REF}</th>
<th>Equal Rise/Fall</th>
<th>Equal Rise/Fall (with OD)</th>
<th>Minimum Sized</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inverter</td>
<td>1</td>
<td>OD</td>
<td></td>
</tr>
<tr>
<td>NOR</td>
<td>\frac{3k+1}{4}</td>
<td>\frac{3k+1}{4} \cdot OD</td>
<td></td>
</tr>
<tr>
<td>NAND</td>
<td>\frac{3+k}{4}</td>
<td>\frac{3+k}{4} \cdot OD</td>
<td></td>
</tr>
<tr>
<td>Overdrive</td>
<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>LH</td>
<td>1</td>
<td>OD</td>
<td></td>
</tr>
<tr>
<td>t_{PROP}/t_{REF}</td>
<td>\sum_{k=1}^{n} \frac{F_{I(k+1)}}{OD_k}</td>
<td>\sum_{k=1}^{n} \frac{F_{I(k+1)}}{OD_k}</td>
<td></td>
</tr>
</tbody>
</table>

\[
OD_{HL} = 1
\]

\[
OD_{LH} = \frac{1}{3k}
\]

\[
OD_{HL} = \frac{1}{k}
\]

\[
OD_{LH} = \frac{1}{3}
\]

\[
FL = \frac{C_{REF}}{2}
\]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

**Minimum-sized gates**

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Overdrive

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<thead>
<tr>
<th>\sum_{k=1}^{n} F_{i(k+1)}</th>
<th>\sum_{k=1}^{n} F_{i(k+1)} \cdot \frac{1}{OD_k}</th>
<th>\sum_{k=1}^{n} \left( \frac{1}{OD_{HL_k}} + \frac{1}{OD_{LH_k}} \right)</th>
</tr>
</thead>
<tbody>
<tr>
<td>\frac{1}{2}</td>
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\[
F_{I} = \frac{C_{REF}}{2}
\]

\[
OD_{HL} = \frac{1}{3k}
\]

\[
OD_{LH} = \frac{1}{1/k}
\]

\[
OD_{HL} = \frac{1}{k}
\]

\[
OD_{LH} = \frac{1}{3}
\]
Minimum-sized gates

\[ \text{PRO} \]

\[ \text{REF} \]

\[ I(k+1) = \left( \frac{1}{2} \sum_{k=1}^{5} F(k+1) \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right) \]

\[ t_{\text{PROP}} = t_{\text{REF}} \cdot \left( \frac{13}{2} \left(3 + 3 + 1 + 1 \cdot 1 + 1 + 1 + 9 + 1 + 1.25 \cdot 2 + 3\right) \right) \]

\[ t_{\text{PROP}} = 63.25 \cdot t_{\text{REF}} \]
End of Lecture 40