EE 330
Lecture 40
Digital Circuits

- Propagation Delay With Multiple Levels of Logic
- Overdrive
The Reference Inverter

\[ R_{PDREF} = R_{PUREF} \]

\[ C_{REF} = C_{IN} = 4C_{OX} W_{MIN} L_{MIN} \]

\[ R_{PDREF} = \frac{L_{MIN}}{\mu_n C_{OX} W_{MIN} (V_{DD} - V_{Tn})} = \frac{L_{MIN}}{\mu_n C_{OX} W_{MIN} (0.8V_{DD})} \]

\[ t_{HLREF} = t_{LHREF} = R_{PDREF} C_{REF} \]

\[ t_{REF} = t_{HLREF} + t_{LHREF} = 2R_{PDREF} C_{REF} \]

Assume \( \mu_n / \mu_p = 3 \)

\( W_n = W_{MIN}, \quad W_p = 3W_{MIN} \)

\( L_n = L_p = L_{MIN} \)

In 0.5u proc \( t_{REF} = 20 \text{ps}, \quad C_{REF} = 4 \text{fF}, \quad R_{PDREF} = R_{PUREF} = 2.5K \)

(Note: This \( C_{OX} \) is somewhat larger than that in the 0.5u ON process)
Question:

Why is $|V_{Tp}| \approx V_{Tn} \approx V_{DD}/5$ in many processes?
Device Sizing

Equal Worse-Case Rise/Fall Device Sizing Strategy
-- (same as $V_{\text{TRIP}} = V_{\text{DD}}/2$ for worst case delay in typical process considered in example)

Assume $\mu_n/\mu_p = 3$
$L_n = L_p = L_{\text{MIN}}$

\[
\begin{align*}
V_{\text{DD}} & \quad \text{V}_{\text{IN}} \\
V_{\text{OUT}} & \quad C_{\text{REF}} \quad \text{M}_1 \\
& \quad \text{M}_2 \\
& \quad \text{M}_{2k}
\end{align*}
\]

INV

$W_n = W_{\text{MIN}}, \quad W_p = 3W_{\text{MIN}}$

$C_{\text{IN}} = C_{\text{REF}}$

$F_l = 1$

\[
\begin{align*}
V_{\text{DD}} & \quad A_k \\
& \quad M_{2k} \\
& \quad \text{M}_{22} \\
& \quad A_1 \\
& \quad M_{21} \\
& \quad A_2 \\
& \quad M_{12} \\
& \quad \cdots \\
& \quad A_k \\
& \quad M_{1k} \\
& \quad \text{V}_{\text{OUT}} \\
& \quad C_{\text{REF}} \quad \text{M}_{11} \\
& \quad \text{M}_{12} \\
& \quad \text{M}_{1k}
\end{align*}
\]

k-input NOR

$W_n = W_{\text{MIN}}$, $W_p = 3kW_{\text{MIN}}$

$C_{\text{IN}} = \left(\frac{3k+1}{4}\right)C_{\text{REF}}$

$F_l = \left(\frac{3k+1}{4}\right)$

\[
\begin{align*}
V_{\text{DD}} & \quad A_k \\
& \quad M_{21} \\
& \quad A_2 \\
& \quad M_{22} \\
& \quad \cdots \\
& \quad A_k \\
& \quad M_{2k} \\
& \quad \text{V}_{\text{OUT}} \\
& \quad C_{\text{REF}} \quad \text{M}_{11} \\
& \quad \text{M}_{12} \\
& \quad \text{M}_{1k}
\end{align*}
\]

k-input NAND

$W_n = kW_{\text{MIN}}$, $W_p = 3W_{\text{MIN}}$

$C_{\text{IN}} = \left(\frac{3+k}{4}\right)C_{\text{REF}}$

$F_l = \left(\frac{3+k}{4}\right)$
Review from Last Time

**Device Sizing – minimum size driving** \( C_{\text{REF}} \)

**INV**

\[ t_{\text{PROP}} = ? \]

\[ t_{\text{PROP}} = 0.5t_{\text{REF}} + \frac{3}{2}t_{\text{REF}} \]

\[ t_{\text{PROP}} = 2t_{\text{REF}} \]

\[ F_{\text{I}} = \frac{C_{\text{REF}}}{2} \]

\[ R_{\text{PU}} = R_{\text{PD}} = R_{\text{PDREF}} \]

**k-input NOR**

\[ t_{\text{PROP}} = ? \]

\[ t_{\text{PROP}} = 0.5t_{\text{REF}} + \frac{3k}{2}t_{\text{REF}} \]

\[ t_{\text{PROP}} = \left(\frac{3k+1}{2}\right)t_{\text{REF}} \]

\[ F_{\text{I}} = \frac{C_{\text{REF}}}{2} \]

\[ R_{\text{PD}} = R_{\text{PDREF}} \quad R_{\text{PU}} = 3kR_{\text{PDREF}} \]

**k-input NAND**

\[ t_{\text{PROP}} = ? \]

\[ t_{\text{PROP}} = \frac{3}{2}t_{\text{REF}} + \frac{k}{2}t_{\text{REF}} \]

\[ t_{\text{PROP}} = \frac{3+k}{2}t_{\text{REF}} \]

\[ F_{\text{I}} = \frac{C_{\text{REF}}}{2} \]

\[ R_{\text{PD}} = 3R_{\text{PDREF}} \quad R_{\text{PU}} = 3R_{\text{PDREF}} \]
Device Sizing Summary

C_{IN} for \text{NAND} gates is considerably smaller than for \text{NOR} gates for equal worst-case rise and fall times.

\text{C_{IN}} for minimum-sized structures is independent of number of inputs and much smaller than \text{C_{IN}} for the equal rise/fall time case.

\text{R_{PU}} gets very large for minimum-sized \text{NOR} gate.
Digital Circuit Design

- Hierarchical Design
- Basic Logic Gates
- Properties of Logic Families
- Characterization of CMOS Inverter
- Static CMOS Logic Gates
  - Ratio Logic
- Propagation Delay
  - Simple analytical models
  - Elmore Delay
- Sizing of Gates

Propagation Delay with Multiple Levels of Logic
- Optimal driving of Large Capacitive Loads
- Power Dissipation in Logic Circuits
- Other Logic Styles
- Array Logic
- Ring Oscillators
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Assume all gates sized for equal worst-case rise/fall times

For $n$ levels of logic between A and F

$$t_{\text{PROP}} = \sum_{k=1}^{n} t_{\text{PROP}}(k)$$
Propagation Delay in Multiple-Levels of Logic with Stage Loading

**Analysis strategy:** Express delays in terms of those of reference inverter

**Reference Inverter**

- $C_{REF} = C_{IN} = 4C_OX W_{MIN} L_{MIN}$
- $F_I = 1$
- $R_{PDREF} = \frac{L_{MIN}}{\mu_n C_OX W_{MIN} (V_{DD} - V_{Tn})} = \frac{L_{MIN}}{\mu_n C_OX W_{MIN} (0.8V_{DD})}$
- $t_{REF} = t_{HLREF} + t_{LHREF} = 2R_{PDREF} C_{REF}$
- $L_n = L_p = L_{MIN}$

Assume $\mu_n/\mu_p = 3$

$W_n = W_{MIN}, W_p = 3W_{MIN}$

In 0.5u proc $t_{REF} = 20ps, C_{REF} = 4fF, R_{PDREF} = 2.5K$

(Note: This $C_OX$ is somewhat larger than that in the 0.5u ON process)
Propagation Delay in Multiple-Levels of Logic with Stage Loading

What loading will a gate see?

- Input capacitance to other gates
- Any load capacitors
- Parasitic interconnect capacitances

Assume:
- all gates sized for equal worst-case rise/fall times
- all gates sized to have rise and fall times equal to that of ref inverter when driving $C_{REF}$

Observe:
- Propagation delay of these gates will be scaled by the ratio of the total load capacitance on each gate to $C_{REF}$
Propagation Delay with Stage Loading

\[ t_{\text{REF}} = 2R_{\text{PDref}} C_{\text{REF}} \]

\[ C_{\text{REF}} = 4C_{\text{OX}} W_{\text{MIN}} L_{\text{MIN}} \]

**Fl of a capacitor**

\[ F_{\text{IC}} = \frac{C}{C_{\text{REF}}} \]

**Fl of a gate** (input k)

\[ F_{\text{IG}} = \frac{C_{\text{INk}}}{C_{\text{REF}}} \]

**Fl of an interconnect**

\[ F_{\text{III}} = \frac{C_{\text{INI}}}{C_{\text{REF}}} \]

**Overall Fl**

\[ F_{\text{I}} = \frac{\sum_{\text{Gates}} C_{\text{INGi}} + \sum_{\text{Capacitances}} C_{\text{INCi}} + \sum_{\text{Interconnects}} C_{\text{INIi}}}{C_{\text{REF}}} \]

Fl can be expressed either in units of capacitance or normalized to \( C_{\text{REF}} \).

Most commonly Fl is normalized but must determine from context.

If gates sized to have same drive as ref inverter

\[ t_{\text{prop-k}} = t_{\text{REF}} \cdot F_{\text{LOAD-k}} \]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Example

Assume all gates sized for equal worst-case rise/fall times

Assume all gate drives are the same as that of reference inverter
Neglect interconnect capacitance, assume load of $10C_{REF}$ on F output

Determine propagation delay from A to F
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Assume all gates sized for equal worst-case rise/fall times
Assume all gate drives are the same as that of reference inverter
Neglect interconnect capacitance, assume load of \(10C_{\text{REF}}\) on F output

Determine propagation delay from A to F

What loading will a gate see?

Derivation:

\[ F_{I_2} = \frac{6}{4} C_{\text{REF}} \]
\[ F_{I_3} = C_{\text{REF}} + \frac{7}{4} C_{\text{REF}} \]
\[ F_{I_4} = \frac{7}{4} C_{\text{REF}} + \frac{13}{4} C_{\text{REF}} \]
\[ F_{I_{\text{LOAD}}} = F_{I_{\text{LOAD}}} = 10C_{\text{REF}} \]
Propogation Delay in Multiple-Levels of Logic with Stage Loading

Example

Assume all gates sized for equal worst-case rise/fall times
Assume all gate drives are the same as that of reference inverter
Neglect interconnect capacitance, assume load of $10C_{REF}$ on F output

**DERIVATIONS**

\[
\begin{align*}
F_{I2} &= \frac{6}{4} C_{REF} \\
F_{I3} &= C_{REF} + \frac{7}{4} C_{REF} \\
F_{I4} &= \frac{7}{4} C_{REF} + \frac{13}{4} C_{REF} \\
F_{I5} &= 10C_{REF}
\end{align*}
\]

\[
\begin{align*}
t_{PROP1} &= \frac{6}{4} t_{REF} \\
t_{PROP2} &= \left(1 + \frac{7}{4}\right) t_{REF} \\
t_{PROP3} &= \left(\frac{7}{4} + \frac{13}{4}\right) t_{REF} \\
t_{PROP4} &= 10t_{REF}
\end{align*}
\]

\[
t_{PROP} = \sum_{k=1}^{n} t_{PROP_k} = t_{REF} \sum_{k=1}^{n} F_{I(k+1)} = t_{REF} \left(\frac{6}{4} + \frac{11}{4} + \frac{20}{4} + 10\right) = t_{REF} (19.25)
\]
Propagation Delay Through Multiple Stages of Logic with Stage Loading

(assuming gate drives are all same as that of reference inverter)

Identify the gate path from A to F

\[ t_{PROP_k} = t_{REF} F_l(k+1) \]

Propagation delay from A to F:

\[ t_{PROP} = t_{REF} \sum_{k=1}^{n} F_l(k+1) \]

This approach is analytically manageable, provides modest accuracy and is “faithful”
Digital Circuit Design

Hierarchical Design
Basic Logic Gates
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  - Simple analytical models
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Sizing of Gates

Propagation Delay with Multiple Levels of Logic
Optimal driving of Large Capacitive Loads
  - Power Dissipation in Logic Circuits
  - Other Logic Styles
  - Array Logic
  - Ring Oscillators

---

done
partial
What if the propagation delay is too long (or too short)?

Propagation delay from A to F:

\[ t_{PROP} = t_{REF} \sum_{k=1}^{n} F_{I(k+1)} \]

\[ t_{PROP_k} = t_{REF} F_{I(k+1)} \]
Recall:

Multiple Input Gates:

2-input NOR

Equal Worst Case Rise/Fall

2-input NAND

(and equal to that of ref inverter when driving $C_{REF}$)

k-input NOR

Fastest response ($t_{HL}$ or $t_{LH}$) = ?

Worst case response ($t_{PROP}$, usually of most interest)?

Input capacitance ($F_I$) = ?

Minimum Sized (assume driving a load of $C_{REF}$)

$W_n = W_{min}$

$W_p = W_{min}$

Fastest response ($t_{HL}$ or $t_{LH}$) = ?

Slowest response ($t_{HL}$ or $t_{LH}$) = ?

Worst case response ($t_{PROP}$, usually of most interest)?

Input capacitance ($F_I$) = ?

consider the fine print!
Device Sizing

Multiple Input Gates: 2-input NOR

(n-channel devices sized same, p-channel devices sized the same)
Assume $L_n = L_p = L_{\text{min}}$ and driving a load of $C_{\text{REF}}$

$W_n = ?$

$W_p = ?$

Input capacitance = ?

$F_I = ?$

$t_{\text{PROP}} = ?$ (worst case)

$W_n = W_{\text{MIN}}$

$W_p = 6W_{\text{MIN}}$

One degree of freedom was used to satisfy the constraint indicated

Other degree of freedom was used to achieve equal rise and fall times

$C_{\text{INA}} = C_{\text{INB}} = C_{\text{OX}}W_{\text{MIN}}L_{\text{MIN}} + 6C_{\text{OX}}W_{\text{MIN}}L_{\text{MIN}} = 7C_{\text{OX}}W_{\text{MIN}}L_{\text{MIN}} = \left(\frac{7}{4}\right)4C_{\text{OX}}W_{\text{MIN}}L_{\text{MIN}} = \left(\frac{7}{4}\right)C_{\text{REF}}$

$F_I = \left(\frac{7}{4}\right)C_{\text{REF}}$ or $F_I = \frac{7}{4}$

$t_{\text{PROP}} = t_{\text{REF}}$ (worst case)
Overdrive Factors

Example: Determine $t_{prop}$ in 0.5u process if $C=10pF$

In 0.5u proc $t_{REF}=20ps$, $C_{REF}=4fF, R_{PDREF}=2.5K$

\[
t_{PROP} = t_{REF} \cdot \frac{10pF}{4fF} = t_{REF} \cdot 2500
\]

$ t_{PROP} = 20ps \cdot 2500 = 50nsec$

Note this is unacceptably long!
Overdrive Factors

Scaling widths of ALL devices by constant \( (W_{\text{scaled}} = W \times \text{OD}) \) will change “drive” capability relative to that of the reference inverter but not change relative value of \( t_{\text{HL}} \) and \( t_{\text{LH}} \)

\[
R_{\text{PD}} = \frac{L_1}{\mu_n C_{\text{OX}} W_1 (V_{\text{DD}} - V_{\text{Tn}})}
\]

\[
R_{\text{PDOD}} = \frac{L_1}{\mu_n C_{\text{OX}} [\text{OD} \cdot W_1] (V_{\text{DD}} - V_{\text{Tn}})} = \frac{R_{\text{PD}}}{\text{OD}}
\]

\[
R_{\text{PU}} = \frac{L_2}{\mu_p C_{\text{OX}} W_2 (V_{\text{DD}} + V_{\text{Tp}})}
\]

\[
R_{\text{PUOD}} = \frac{L_2}{\mu_p C_{\text{OX}} [\text{OD} \cdot W_2] (V_{\text{DD}} + V_{\text{Tp}})} = \frac{R_{\text{PU}}}{\text{OD}}
\]

Scaling widths of ALL devices by constant will change \( f_I \) by \( \text{OD} \)

\[
C_{\text{IN}} = C_{\text{OX}} (W_1 L_1 + W_2 L_2)
\]

\[
C_{\text{INOD}} = C_{\text{OX}} \left( [\text{OD} \cdot W_1] L_1 + [\text{OD} \cdot W_2] L_2 \right) = \text{OD} \cdot C_{\text{IN}}
\]
Overdrive Factors

- The factor by which the devices are W/L scaled above those of the reference inverter is termed the overdrive factor, OD.

- Scaling widths by overdrive factor DECREASES resistance by same factor.

- Scaling all widths by a constant does not compromise the symmetry between the rise and fall times.

- Judicious use of overdrive can dramatically improve the speed of digital circuits.

- Large overdrive factors are often used.

- Scaling widths by overdrive factor INCREASES input capacitance by same factor.
Overdrive

Define the Asymmetric Overdrive Factors of the stage to be the factor by which PU and PD resistors are scaled relative to those of the reference inverter.

\[ R_{PDEFF} = \frac{R_{PDREF}}{OD_{HL}} \quad R_{PUEFF} = \frac{R_{PUREF}}{OD_{LH}} \]

If inverter sized for equal rise/fall, define OD by \( OD_{HL} = OD_{LH} = OD \)

\[ t_{HL} = t_{LH} = \frac{R_{PDREF}}{OD} C_L = R_{PDREF} C_{REF} \frac{F_{IL}}{OD} \]

\[ t_{PROP} = t_{LH} + t_{HL} = t_{REF} \frac{F_{IL}}{OD} \]

OD may be larger or smaller than 1
Propagation Delay with Over-drive Capability

Example

Compare the propagation delays. Assume the OD is 900 in the third case and 30 in the fourth case. Don’t worry about the extra inversion at this time.

\[ t_{\text{PROP}} = 900 t_{\text{REF}} \]

\[ t_{\text{PROP}} = t_{\text{REF}} + 900 t_{\text{REF}} = 901 t_{\text{REF}} \]

\[ t_{\text{PROP}} = 900 t_{\text{REF}} + t_{\text{REF}} = 901 t_{\text{REF}} \]

\[ t_{\text{PROP}} = 30 t_{\text{REF}} + 30 t_{\text{REF}} = 60 t_{\text{REF}} \]

Note: Dramatic reduction in \( t_{\text{PROP}} \) is possible. Will later determine what optimal number of stages and sizing is.
Propagation Delay in Multiple-Levels of Logic with Stage Loading

\[ t_{PROP} = t_{REF} \sum_{k=1}^{n} \frac{F_{I(k+1)}}{OD_k} \]

Summary: Propagation delay from A to F:

\[ t_{PROP} = t_{REF} \sum_{k=1}^{n} \frac{F_{I(k+1)}}{OD_k} \]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Will consider an example with the five cases

• Equal rise/fall (no overdrive)

• Equal rise/fall with overdrive

• Minimum Sized

• Asymmetric Overdrive

• Combination of equal rise/fall, minimum size and overdrive

Will develop the analysis methods as needed
Propagation Delay in Multiple-Levels of Logic with Stage Loading

- Equal rise/fall (no overdrive)
- Equal rise/fall with overdrive
- Minimum Sized
- Asymmetric overdrive
- Combination of equal rise/fall, minimum size and overdrive

\[
t_{PROP} = t_{REF} \sum_{k=1}^{n} \frac{F_l(k+1)}{OD_k}
\]

\[
t_{PROP} = \ ?
\]

\[
t_{PROP} = \ ?
\]

\[
t_{PROP} = \ ?
\]
Driving Notation

- Equal rise/fall (no overdrive)
- Equal rise/fall with overdrive
- Minimum Sized
- Asymmetric Overdrive

Notation will be used only if it is not clear from the context what sizing is being used
Define the Asymmetric Overdrive Factors of the stage to be the factors by which PU and PD resistors are scaled relative to those of the reference inverter.

\[ R_{PDEFF} = \frac{R_{PDREF}}{OD_{HL}} \quad \quad R_{PUEFF} = \frac{R_{PUREF}}{OD_{LH}} \]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

**Asymmetric Overdrive**

\[ t_{\text{PROP}} = t_{\text{HL}} + t_{\text{LH}} = t_{\text{REF}} \frac{F_{\text{IL}}}{\text{OD}} \]

If inverter is not equal rise/fall

\[ t_{\text{HL}} = \frac{R_{\text{PDREF}}}{\text{OD}_{\text{HL}}} C_L = \frac{1}{2} t_{\text{REF}} \frac{F_{\text{IL}}}{\text{OD}_{\text{HL}}} \]

\[ t_{\text{LH}} = \frac{R_{\text{PUREF}}}{\text{OD}_{\text{LH}}} C_L = \frac{1}{2} t_{\text{REF}} \frac{F_{\text{IL}}}{\text{OD}_{\text{LH}}} \]

\[ t_{\text{PROP}} = t_{\text{HL}} + t_{\text{LH}} = \frac{1}{2} t_{\text{REF}} F_{\text{IL}} \left( \frac{1}{\text{OD}_{\text{HL}}} + \frac{1}{\text{OD}_{\text{LH}}} \right) \]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Asymmetric Overdrive

\[ t_{PROP} = t_{HL} + t_{LH} = \frac{1}{2} t_{REF} F_{IL} \left( \frac{1}{OD_{HL}} + \frac{1}{OD_{LH}} \right) \]

When propagating through \( n \) stages:

\[ t_{PROP} = t_{REF} \cdot \left( \frac{1}{2} \sum_{k=1}^{n} F_{I(k+1)} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right) \]

\( F_{Ik} \) denotes the total loading on stage \( k \) which is the sum of the \( F_{I} \) of all loading on stage \( k \)
Propagation Delay in Multiple-Levels of Logic with Stage Loading and Overdrives

Will now consider A to F propagation for this circuit as an example with different overdrives
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Equal rise-fall gates, no overdrive

In 0.5u proc  \( t_{\text{REF}}=20\text{ps} \),
\( C_{\text{REF}}=4\text{fF} \), \( R_{\text{PDREF}}=2.5\text{K} \)

\[ t_{\text{REF}} = 2t_{H_{\text{L-REF}}} \]

\[ t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^{n} F_{k+1} \]
## Propagation Delay in Multiple-Levels of Logic with Stage Loading

**Equal rise-fall gates, no overdrive**

<table>
<thead>
<tr>
<th></th>
<th>Equal Rise/Fall</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{IN}/C_{REF}$</td>
<td></td>
</tr>
<tr>
<td>Inverter</td>
<td>1</td>
</tr>
<tr>
<td>NOR</td>
<td>$\frac{3k+1}{4}$</td>
</tr>
<tr>
<td>NAND</td>
<td>$\frac{3+k}{4}$</td>
</tr>
<tr>
<td>Overdrive</td>
<td></td>
</tr>
<tr>
<td>Inverter</td>
<td></td>
</tr>
<tr>
<td>HL</td>
<td>1</td>
</tr>
<tr>
<td>LH</td>
<td>1</td>
</tr>
<tr>
<td>NOR</td>
<td>1</td>
</tr>
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<td></td>
</tr>
<tr>
<td>HL</td>
<td>1</td>
</tr>
<tr>
<td>LH</td>
<td>1</td>
</tr>
<tr>
<td>$t_{PROP}/t_{REF}$</td>
<td>$\sum_{k=1}^{5} F_{k+1}$</td>
</tr>
</tbody>
</table>

$$t_{PROP} = t_{REF} \sum_{k=1}^{5} F_{k+1}$$
Equal rise-fall gates, no overdrive

In 0.5μ proc, $t_{REF}=20$ps, $C_{REF}=4fF$, $R_{PDREF}=2.5K$

(Note: This $C_{OX}$ is somewhat larger than that in the 0.5μ ON process)

$t_{PROP} = t_{REF} \sum_{k=1}^{5} F_{k+1}$

$F_{I2}=10.25$
$F_{I3}=4.25$
$F_{I4}=4.25$
$F_{I5}=1.25$
$F_{I6}=12.5$

$t_{PROP} = 32.5t_{REF}$
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Equal rise-fall gates, with overdrive

In 0.5u proc\ $t_{REF}=20\text{ps},$\n\[C_{REF}=4fF, R_{PDREF}=2.5K\]

(Note: This $C_{OX}$ is somewhat larger than that in the 0.5u ON process)

\[t_{PROP} = t_{REF} \sum_{k=1}^{n} \frac{F_{k+1}}{OD_k}\]
# Propagation Delay in Multiple-Levels of Logic with Stage Loading

### Equal rise-fall gates, with overdrive

<table>
<thead>
<tr>
<th>$C_{IN}/C_{REF}$</th>
<th>Equal Rise/Fall</th>
<th>Equal Rise/Fall (with OD)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inverter</td>
<td>$1$</td>
<td>$OD$</td>
</tr>
<tr>
<td>NOR</td>
<td>$\frac{3k+1}{4}$</td>
<td>$\frac{3k+1}{4} \bullet OD$</td>
</tr>
<tr>
<td>NAND</td>
<td>$\frac{3+k}{4}$</td>
<td>$\frac{3+k}{4} \bullet OD$</td>
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</tbody>
</table>

### Overdrive

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<th>Equal Rise/Fall</th>
<th>Equal Rise/Fall (with OD)</th>
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</thead>
<tbody>
<tr>
<td>Inverter</td>
<td></td>
<td></td>
</tr>
<tr>
<td>HL</td>
<td>$1$</td>
<td>$OD$</td>
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<td>NOR</td>
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<td>HL</td>
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</tr>
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<td>LH</td>
<td>$1$</td>
<td>$OD$</td>
</tr>
</tbody>
</table>

$$t_{PROP}/t_{REF} = \sum_{k=1}^{n} F_{i(k+1)}$$

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} \frac{F_{i(k+1)}}{OD_k}$$
Equal rise-fall gates, with overdrive

In 0.5u proc  $t_{\text{REF}}=20\text{ps}$,
$C_{\text{REF}}=4\text{fF}, R_{\text{PDREF}}=2.5\text{K}$

(Note: This $C_{\text{OX}}$ is somewhat larger than that in the 0.5u ON process)
End of Lecture 40