EE 330
Lecture 40

Digital Circuits

- Propagation Delay With Multiple Levels of Logic
- Overdrive
Propagation Delay in Static CMOS Family

Propagation through k levels of logic

\[ t_{HL} \approx t_{HLn} + t_{LH(n-1)} + t_{HL(n-2)} + \cdots + t_{XY1} \]

\[ t_{LH} \approx t_{LHn} + t_{HL(n-1)} + t_{LH(n-2)} + \cdots + t_{YX1} \]

where \( x=H \) and \( Y=L \) if \( n \) odd and \( X=L \) and \( Y=h \) if \( n \) even

\[ t_{PROP} = \sum_{i=1}^{n} t_{PROP_i} \]

Will return to propagation delay after we discuss device sizing
The Reference Inverter

Assume $\mu_n/\mu_p = 3$

$W_n = W_{MIN}, \quad W_p = 3W_{MIN}$

$L_n = L_p = L_{MIN}$

In 0.5u proc, $t_{REF} = 20ps$

$C_{REF} = 4C_{OX} W_{MIN} L_{MIN}$

$R_{PDREF} = R_{PUREF}$

$t_{HLREF} = t_{LHREF} = R_{PDREF} C_{REF}$

$t_{REF} = t_{HLREF} + t_{LHREF} = 2R_{PDREF} C_{REF}$

$t_{REF} = \frac{8L_{MIN}^2}{\mu_n (V_{DD} - V_{Tn})}$

(Note: This $C_{OX}$ is somewhat larger than that in the 0.5u ON process)
Fan In

- The Fan In (FI) to an input of a gate device, circuit or interconnect that is capacitive is the input capacitance.
- Often this is normalized to some capacitance (typically $C_{REF}$ of ref inverter).

$$FI = \frac{C_{IN}}{C_{REF}}$$
Device Sizing

Equal Worst Case Rise/Fall (and equal to that of ref inverter when driving $C_{REF}$)

Multiple Input Gates: $k$-input NOR

$W_n = W_{MIN}$

$W_p = 3kW_{MIN}$

$C_{INx} = C_{OX}W_{MIN}L_{MIN} + 3kC_{OX}W_{MIN}L_{MIN}$

$= (3k+1)C_{OX}W_{MIN}L_{MIN} = \left( \frac{3k+1}{4} \right) 4C_{OX}W_{MIN}L_{MIN}$

$= \left( \frac{3k+1}{4} \right) C_{REF}$

$FI = \left( \frac{3k+1}{4} \right) C_{REF}$ or $FI = \frac{3k+1}{4}$

$t_{PROP} = t_{REF}$
Device Sizing

Equal Worst Case Rise/Fall (and equal to that of ref inverter when driving $C_{\text{REF}}$)

Multiple Input Gates: $k$-input NAND

$W_n = kW_{\text{MIN}}$

$W_p = 3W_{\text{MIN}}$

$C_{\text{INx}} = kC_{\text{OX}}W_{\text{MIN}}L_{\text{MIN}} + 3C_{\text{OX}}W_{\text{MIN}}L_{\text{MIN}}$

$= (3+k)C_{\text{OX}}W_{\text{MIN}}L_{\text{MIN}} = \left(\frac{3+k}{4}\right)4C_{\text{OX}}W_{\text{MIN}}L_{\text{MIN}}$

$= \left(\frac{3+k}{4}\right)C_{\text{REF}}$

$F_I = \left(\frac{3+k}{4}\right)C_{\text{REF}} \quad \text{or} \quad F_I = \frac{3+k}{4}$

$t_{\text{PROP}} = t_{\text{REF}}$
Review from Last Time

Device Sizing

The minimum-sized inverter pair

Assume $\mu_n/\mu_p = 3$

$L_n = L_p = L_{MIN}$ \hspace{1cm} $W_n = W_{MIN}$, $W_p = W_n$

$C_{REF} = 4C_{OX} W_{MIN} L_{MIN}$

$C_{L1} = 0.5C_{REF} = 2C_{OX} W_{MIN} L_{MIN}$

$R_{PDREF} = \frac{L_{MIN}}{\mu_n C_{OX} W_{MIN} (V_{DD} - V_{Tn})}$

$t_{PROP} = t_{HLREF} + t_{LHREF} = R_{PDREF} (0.5C_{REF}) + 3R_{PDREF} (0.5C_{REF}) = 2R_{PDREF} C_{REF}$

$t_{PROP} = t_{REF}$

$F_l = 0.5C_{REF}$ \hspace{1cm} or \hspace{1cm} $F_l = 0.5$
## Device Sizing

### Multiple Input Gates:

<table>
<thead>
<tr>
<th>Gate Type</th>
<th>Circuit Illustration</th>
</tr>
</thead>
<tbody>
<tr>
<td>2-input NOR</td>
<td><img src="image" alt="2-input NOR Circuit" /></td>
</tr>
<tr>
<td>2-input NAND</td>
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</tr>
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<td><img src="image" alt="k-input NAND Circuit" /></td>
</tr>
</tbody>
</table>

**Equal Worst Case Rise/Fall** (and equal to that of ref inverter when driving $C_{REF}$)

- $W_n =$?
- $W_p =$?
- Fastest response ($t_{HL}$ or $t_{LH}$) = ?
- Worst case response ($t_{PROP}$, usually of most interest)?
- Input capacitance (FI) = ?

**Minimum Sized** (assume driving a load of $C_{REF}$)

- $W_n = W_{min}$
- $W_p = W_{min}$
- Fastest response ($t_{HL}$ or $t_{LH}$) = ?
- Slowest response ($t_{HL}$ or $t_{LH}$) = ?
- Worst case response ($t_{PROP}$, usually of most interest)?
- Input capacitance (FI) = ?
Minimum Sized (assume driving a load of \( C_{\text{REF}} \))

Input capacitance (\( F_I \)) = ?

\[
C_{\text{IN}} = C_{\text{OX}} W_n L_n + C_{\text{OX}} W_p L_p = C_{\text{OX}} W_{\text{min}} L_{\text{min}} + C_{\text{OX}} W_{\text{min}} L_{\text{min}} = 2 C_{\text{OX}} W_{\text{min}} L_{\text{min}} = \frac{C_{\text{REF}}}{2}
\]

\[
F_I = \frac{1}{2}
\]

Fastest response (\( t_{\text{HL}} \) or \( t_{\text{LH}} \)) = ?

Slowest response (\( t_{\text{HL}} \) or \( t_{\text{LH}} \)) = ?

Worst case response (\( t_{\text{PROP}} \), usually of most interest)?
Device Sizing – minimum size driving $C_{\text{REF}}$

**INV**

$t_{\text{PROP}} = \frac{3}{2} t_{\text{REF}}$

$t_{\text{PROP}} = 0.5 t_{\text{REF}} + \frac{3}{2} t_{\text{REF}}$

$t_{\text{PROP}} = 2 t_{\text{REF}}$

$F_{\text{I}} = \frac{C_{\text{REF}}}{2}$

$R_{\text{PU}} = 3 R_{\text{PDREF}}$

$R_{\text{PD}} = R_{\text{PDREF}}$

$k$-input **NOR**

$t_{\text{PROP}} = \left(\frac{3k+1}{2}\right) t_{\text{REF}}$

$t_{\text{PROP}} = 0.5 t_{\text{REF}} + \frac{3k}{2} t_{\text{REF}}$

$F_{\text{I}} = \frac{C_{\text{REF}}}{2}$

$R_{\text{PD}} = R_{\text{PDREF}}$

$R_{\text{PU}} = 3 k R_{\text{PDREF}}$

$k$-input **NAND**

$t_{\text{PROP}} = \frac{3}{2} t_{\text{REF}} + \frac{k}{2} t_{\text{REF}}$

$t_{\text{PROP}} = \frac{3+k}{2} t_{\text{REF}}$

$F_{\text{I}} = \frac{C_{\text{REF}}}{2}$

$R_{\text{PD}} = k R_{\text{PDREF}}$

$R_{\text{PU}} = 3 R_{\text{PDREF}}$
Device Sizing Summary

$C_{IN}$ for $N_{AND}$ gates is considerably smaller than for NOR gates for equal worst-case rise and fall times.

$C_{IN}$ for minimum-sized structures is independent of number of inputs and much smaller than $C_{IN}$ for the equal rise/fall time case.

$R_{PU}$ gets very large for minimum-sized NOR gate.
Digital Circuit Design

- Hierarchical Design
- Basic Logic Gates
- Properties of Logic Families
- Characterization of CMOS Inverter
- Static CMOS Logic Gates – Ratio Logic
- Propagation Delay – Simple analytical models – Elmore Delay
- Sizing of Gates

- Propagation Delay with Multiple Levels of Logic
- Optimal driving of Large Capacitive Loads
- Power Dissipation in Logic Circuits
- Other Logic Styles
- Array Logic
- Ring Oscillators
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Assume all gates sized for equal worst-case rise/fall times

For $n$ levels of logic between A and F

\[ t_{PROP} = \sum_{i=1}^{n} t_{PROP_i} \]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

**Analysis strategy:** Express delays in terms of those of reference inverter

**Reference Inverter**

\[ C_{\text{REF}} = C_{\text{IN}} = 4C_{\text{OX}} W_{\text{MIN}} L_{\text{MIN}} \]

\[ R_{\text{PDREF}} = \frac{L_{\text{MIN}}}{\mu_n C_{\text{OX}} W_{\text{MIN}} (V_{\text{DD}} - V_{Tn})} = \frac{L_{\text{MIN}}}{\mu_n C_{\text{OX}} W_{\text{MIN}} (0.8V_{\text{DD}})} \]

\[ t_{\text{REF}} = t_{\text{HLREF}} + t_{\text{LHREF}} = 2R_{\text{PDREF}} C_{\text{REF}} \]

\[ t_{\text{REF}} = \frac{10L_{\text{MIN}}^2}{\mu_n V_{\text{DD}}} \]

Assume \( \mu_n/\mu_p = 3 \)

\( W_n = W_{\text{MIN}}, \quad W_p = 3W_{\text{MIN}} \)

In 0.5u proc \( t_{\text{REF}} = 20\text{ps}, \quad C_{\text{REF}} = 4\text{fF}, \quad R_{\text{PDREF}} = 2.5\text{K} \)

(Note: This \( C_{\text{OX}} \) is somewhat larger than that in the 0.5u ON process)
Propagation Delay in Multiple-Levels of Logic with Stage Loading

What loading will a gate see?

- Input capacitance to other gates
- Any load capacitors
- Parasitic interconnect capacitances

Assume:
- all gates sized for equal worst-case rise/fall times
- all gates sized to have rise and fall times equal to that of ref inverter when driving $C_{REF}$

Observe:
- Propagation delay of these gates will be scaled by the ratio of the total load capacitance on each gate to $C_{REF}$
Propagation Delay with Stage Loading

\[ t_{\text{REF}} = 2R_{\text{PD ref}} C_{\text{REF}} \]

\[ C_{\text{REF}} = 4C_{\text{OX}} W_{\text{MIN}} L_{\text{MIN}} \]

**Fl of a capacitor**

\[ F_{\text{FI C}} = \frac{C}{C_{\text{REF}}} \]

**Fl of a gate (input k)**

\[ F_{\text{FI G}} = \frac{C_{\text{IN k}}}{C_{\text{REF}}} \]

**Fl of an interconnect**

\[ F_{\text{FI I}} = \frac{C_{\text{INI}}}{C_{\text{REF}}} \]

**Overall Fl**

\[ F_{\text{FI}} = \frac{\sum C_{\text{ING i}} + \sum C_{\text{IN Ci}} + \sum C_{\text{INI li}}}{C_{\text{REF}}} \]

Fl can be expressed either in units of capacitance or normalized to \( C_{\text{REF}} \).

Most commonly Fl is normalized but must determine from context.

If gates sized to have same drive as ref inverter

\[ t_{\text{prop - i}} = t_{\text{REF}} \cdot F_{\text{LOAD - i}} \]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Example

Assume all gates sized for equal worst-case rise/fall times
Assume all gate drives are the same as that of reference inverter
Neglect interconnect capacitance, assume load of $10C_{REF}$ on F output

Determine propagation delay from A to F
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Assume all gates sized for equal worst-case rise/fall times
Assume all gate drives are the same as that of reference inverter
Neglect interconnect capacitance, assume load of $10C_{REF}$ on F output

Determine propagation delay from A to F

What loading will a gate see?

Derivation:

$$F_{I_2} = \frac{6}{4}C_{REF}$$
$$F_{I_3} = C_{REF} + \frac{7}{4}C_{REF}$$
$$F_{I_4} = \frac{7}{4}C_{REF} + \frac{13}{4}C_{REF}$$
$$F_{LOAD} = F_{I_5} = 10C_{REF}$$
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Example

Assume all gates sized for equal worst-case rise/fall times
Assume all gate drives are the same as that of reference inverter
Neglect interconnect capacitance, assume load of $10C_{REF}$ on F output

Determine propagation delay from A to F

DERIVATIONS

$F_{I_2} = \frac{6}{4}C_{REF}$
$F_{I_3} = C_{REF} + \frac{7}{4}C_{REF}$
$F_{I_4} = \frac{7}{4}C_{REF} + \frac{13}{4}C_{REF}$
$F_{I_5} = 10C_{REF}$

$t_{PROP_1} = \frac{6}{4}t_{REF}$
$t_{PROP_2} = \left(1 + \frac{7}{4}\right)t_{REF}$
$t_{PROP_3} = \left(\frac{7}{4} + \frac{13}{4}\right)t_{REF}$
$t_{PROP_4} = 10t_{REF}$

$t_{PROP} = \sum_{i=1}^{n} t_{PROP_i} = t_{REF} \sum_{i=1}^{n} F_{I_{(i+1)}} = t_{REF} \left(\frac{6}{4} + \frac{11}{4} + \frac{20}{4} + 10\right) = t_{REF} (19.25)$
Propagation Delay Through Multiple Stages of Logic with Stage Loading

(assuming gate drives are all same as that of reference inverter)

Identify the gate path from A to F

\[ t_{\text{PROPI}} = t_{\text{REF}} F_{I(i+1)} \]

Propagation delay from A to F:

\[ t_{\text{PROP}} = t_{\text{REF}} \sum_{i=1}^{n} F_{I(i+1)} \]

This approach is analytically manageable, provides modest accuracy and is “faithful”
What if the propagation delay is too long (or too short)?

\[ t_{PROP} = t_{REF} \sum_{i=1}^{n} F_i(i+1) \]

\[ t_{PROP_i} = t_{REF} F_i(i+1) \]
Device Sizing

Equal Worst Case Rise/Fall (and equal to that of ref inverter when driving $C_{REF}$)

$W_n =$?
$W_p =$?

Fastest response ($t_{HL}$ or $t_{LH}$) = ?

Worst case response ($t_{PROP}$, usually of most interest)?

Input capacitance (FI) = ?

Minimum Sized (assume driving a load of $C_{REF}$)

$W_n = W_{min}$
$W_p = W_{min}$

Fastest response ($t_{HL}$ or $t_{LH}$) = ?

Slowest response ($t_{HL}$ or $t_{LH}$) = ?

Worst case response ($t_{PROP}$, usually of most interest)?

Input capacitance (FI) = ?
Equal Worst Case Rise/Fall (and equal to that of ref inverter when driving $C_{REF}$)

Multiple Input Gates: 2-input NOR

(n-channel devices sized same, p-channel devices sized the same)
Assume $L_n = L_p = L_{min}$ and driving a load of $C_{REF}$

$W_n = ?$

$W_p = ?$

Input capacitance = ?

$F_I = ?$

$t_{PROP} = ?$ (worst case)

$W_n = W_{MIN}$

$W_p = 6W_{MIN}$

Recall:
One degree of freedom was used to satisfy the constraint indicated

Other degree of freedom was used to achieve equal rise and fall times

$C_{INA} = C_{INB} = C_{OX} W_{MIN} L_{MIN} + 6 C_{OX} W_{MIN} L_{MIN} = 7 C_{OX} W_{MIN} L_{MIN} = \left( \frac{7}{4} \right) 4 C_{OX} W_{MIN} L_{MIN} = \left( \frac{7}{4} \right) C_{REF}$

$F_I = \left( \frac{7}{4} \right) C_{REF}$ or $F_I = \frac{7}{4}$

$t_{PROP} = t_{REF}$ (worst case)
Example: Determine $t_{prop}$ in 0.5u process if $C=10\,pF$

In 0.5u proc $t_{REF}=20\,ps$, $C_{REF}=4\,fF$, $R_{PDREF}=2.5\,K$

$$t_{prop}=t_{REF} \cdot F I = t_{REF} \cdot \frac{10\,pF}{4\,fF} = t_{REF} \cdot 2500$$

$$t_{prop}=20\,ps \cdot 2500 = 50\,nsec$$

Note this is unacceptably long!
Overdrive Factors

Scaling widths of ALL devices by constant \((W_{\text{scaled}}=W_{\text{OD}})\) will change “drive” capability relative to that of the reference inverter but not change relative value of \(t_{\text{HL}}\) and \(t_{\text{LH}}\)

\[
R_{\text{PD}} = \frac{L_1}{\mu_n C_{\text{OX}} W_1 (V_{\text{DD}}-V_{\text{Tn}})}
\]

\[
R_{\text{PDOD}} = \frac{L_1}{\mu_n C_{\text{OX}} [\text{OD} \cdot W_1] (V_{\text{DD}}-V_{\text{Tn}})} = \frac{R_{\text{PD}}}{\text{OD}}
\]

\[
R_{\text{PU}} = \frac{L_2}{\mu_p C_{\text{OX}} W_2 (V_{\text{DD}}+V_{\text{Tp}})}
\]

\[
R_{\text{PUOD}} = \frac{L_2}{\mu_p C_{\text{OX}} [\text{OD} \cdot W_2] (V_{\text{DD}}+V_{\text{Tp}})} = \frac{R_{\text{PU}}}{\text{OD}}
\]

Scaling widths of ALL devices by constant will change FI by OD

\[
C_{\text{IN}} = C_{\text{OX}} (W_1 L_1 + W_2 L_2)
\]

\[
C_{\text{INOD}} = C_{\text{OX}} ([\text{OD} \cdot W_1] L_1 + [\text{OD} \cdot W_2] L_2) = \text{OD} \cdot C_{\text{IN}}
\]
Overdrive Factors

- The factor by which the devices are W/L scaled above those of the reference inverter is termed the overdrive factor, OD.

- Scaling widths by overdrive factor DECREASES resistance by the same factor.

- Scaling all widths by a constant does not compromise the symmetry between the rise and fall times.

- Judicious use of overdrive can dramatically improve the speed of digital circuits.

- Large overdrive factors are often used.

- Scaling widths by overdrive factor INCREASES input capacitance by the same factor.
Define the Asymmetric Overdrive Factors of the stage to be the factor by which PU and PD resistors are scaled relative to those of the reference inverter.

\[
R_{PDEFF} = \frac{R_{PDREF}}{OD_{HL}} \quad R_{PUEFF} = \frac{R_{PUREF}}{OD_{LH}}
\]

If inverter sized for equal rise/fall, define OD by \( OD_{HL} = OD_{LH} = OD \)

\[
t_{HL} = t_{LH} = \frac{R_{PDREF}}{OD} C_L = R_{PDREF} C_{REF} \frac{F_{IL}}{OD}
\]

\[
C_{IN} = C_{REF} \cdot OD
\]

\[
t_{PROP} = t_{LH} + t_{HL} = t_{REF} \frac{F_{IL}}{OD}
\]

OD may be larger or smaller than 1
Propagation Delay with Over-drive Capability

Example

Compare the propagation delays. Assume the OD is 900 in the third case and 30 in the fourth case. Don’t worry about the extra inversion at this time.

\[ t_{\text{PROP}} = 900t_{\text{REF}} \]

\[ t_{\text{PROP}} = t_{\text{REF}} + 900t_{\text{REF}} = 901t_{\text{REF}} \]

\[ t_{\text{PROP}} = 900t_{\text{REF}} + t_{\text{REF}} = 901t_{\text{REF}} \]

\[ t_{\text{PROP}} = 30t_{\text{REF}} + 30t_{\text{REF}} = 60t_{\text{REF}} \]

Note: Dramatic reduction in \( t_{\text{PROP}} \) is possible
Will later determine what optimal number of stages and sizing is
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Fl_i denotes the total loading on stage i which is the sum of the Fl of all loading on stage i

Summary: Propagation delay from A to F:

$$t_{PROP} = t_{REF} \sum_{i=1}^{n} \frac{Fl_{(i+1)}}{OD_i}$$

$$Fl_{NOR_{i}} = OD_{i} \left( \frac{3k_{i} + 1}{4} \right) C_{REF}$$

$$Fl_{NAND_{i}} = OD_{i} \left( \frac{3 + k_{i}}{4} \right) C_{REF}$$
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Will consider an example with the five cases

- Equal rise/fall (no overdrive)
- Equal rise/fall with overdrive
- Minimum Sized
- Asymmetric Overdrive
- Combination of equal rise/fall, minimum size and overdrive

Will develop the analysis methods as needed
Propagation Delay in Multiple-Levels of Logic with Stage Loading

- Equal rise/fall (all overdrive = 1)
- Equal rise/fall with overdrive
- Minimum Sized
- Asymmetric overdrive
- Combination of equal rise/fall, minimum size and overdrive
Driving Notation

- Equal rise/fall (no overdrive)
- Equal rise/fall with overdrive
- Minimum Sized
- Asymmetric Overdrive

Notation will be used only if it is not clear from the context what sizing is being used
Asymmetric Overdrive

**Recall:**

Define the Asymmetric Overdrive Factors of the stage to be the factors by which PU and PD resistors are scaled relative to those of the reference inverter.

\[ R_{PDEFF} = \frac{R_{PDREF}}{OD_{HL}} \quad \quad \quad \quad R_{PUEFF} = \frac{R_{PUREF}}{OD_{LH}} \]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Asymmetric Overdrive

\[ t_{\text{PROP}} = t_{\text{HL}} + t_{\text{LH}} = t_{\text{REF}} \frac{F_L}{OD} \]

If inverter is not equal rise/fall

\[ t_{\text{HL}} = R_{\text{PDREF}} \frac{C_L}{OD_{\text{HL}}} = \frac{1}{2} t_{\text{REF}} \frac{F_L}{OD_{\text{HL}}} \]

\[ t_{\text{LH}} = R_{\text{PUREF}} \frac{C_L}{OD_{\text{LH}}} = \frac{1}{2} t_{\text{REF}} \frac{F_L}{OD_{\text{LH}}} \]

\[ t_{\text{PROP}} = t_{\text{HL}} + t_{\text{LH}} = \frac{1}{2} t_{\text{REF}} F_L \left( \frac{1}{OD_{\text{HL}}} + \frac{1}{OD_{\text{LH}}} \right) \]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

**Asymmetric Overdrive**

\[ V_{IN} \rightarrow \underbrace{\text{Gate}}_{C_L} \rightarrow V_{OUT} \]

\[ \text{PROP} = \text{HL} + \text{LH} = \frac{1}{2} \text{REF} \cdot \text{OD}_L \left( \frac{1}{\text{OD}_{HL}} + \frac{1}{\text{OD}_{LH}} \right) \]

When propagating through \( n \) stages:

\[ t_{PROP} = t_{HL} + t_{LH} = \frac{1}{2} \text{REF} \cdot \sum_{i=1}^{n} \text{FI}_{i(i+1)} \left( \frac{1}{\text{OD}_{HL_i}} + \frac{1}{\text{OD}_{LH_i}} \right) \]

\( \text{FI}_k \) denotes the total loading on stage \( k \) which is the sum of the \( \text{FI} \) of all loading on stage \( k \)
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Overdrive Notation

Equal Rise/Fall with overdrive OD

Rise/Fall may be different with overdrive \( \text{OD}_{\text{HL}} \) and \( \text{OD}_{\text{LH}} \)

Examples

Equal Rise/Fall with overdrive of 8

If \( W_n = W_{\text{MIN}} \), minimum sized inverter
Propagation Delay Through Multiple Stages of Logic with Stage Loading

(assuming gate *drives* are all same as that of reference inverter)

\[
\begin{align*}
F_{\text{NOR}} &= \left( \frac{3k+1}{4} \right) \\
F_{\text{NAND}} &= \left( \frac{3+k}{4} \right)
\end{align*}
\]

Identify the gate path from A to F

Identify each gate FI and delay:

\[
t_{\text{PROP}i} = t_{\text{REF}} F_{I(i+1)}
\]

Propagation delay from A to F:

\[
t_{\text{PROP}} = t_{\text{REF}} \sum_{i=1}^{n} F_{I(i+1)}
\]
Propagation Delay Through Multiple Stages of Logic with Stage Loading

Each gate has its own overdrive relative to that of reference inverter

Identify the gate path from A to F
Identify each gate’s FI
Identify each gate’s OD

Propagation delay from A to F:

\[ t_{PROP} = t_{REF} \sum_{i=1}^{n} \frac{FI_{(i+1)}}{OD_i} \]
Propagation Delay Through Multiple Stages of Logic with Stage Loading

Each gate has possibly asymmetric overdrives

\[
\text{Fl}_{\text{NOR}} = \frac{3k_i \text{OD}_{LHi} + 1 \cdot \text{OD}_{HLi}}{4}
\]

\[
\text{Fl}_{\text{NAND}} = \frac{3 \text{OD}_{LHi} + k_i \text{OD}_{HLi}}{4}
\]

Identify the gate path from A to F

Identify each gate’s FI

Identify each gate’s OD<sub>HL</sub> and OD<sub>LH</sub>

Propagation delay from A to F:

\[
t_{\text{PROP}} = \frac{t_{\text{REF}}}{2} \sum_{i=1}^{n} \text{Fl}_{(i+1)} \left( \frac{1}{\text{OD}_{HLi}} + \frac{1}{\text{OD}_{LHi}} \right)
\]
Propagation Delay Through Multiple Stages of Logic with Stage Loading

Minimum size strategy:

$$\text{FL}_{\text{NOR}} = \frac{3k_i \text{OD}_{LH_i} + 1 \cdot \text{OD}_{HL_i}}{4} = \frac{1+1}{4}$$

$$\text{OD}_{LH} = \frac{1}{3}k; \quad \text{OD}_{HL} = 1$$

$$\text{FL}_{\text{NAND}} = \frac{3 \text{OD}_{LH_i} + k_i \text{OD}_{HL_i}}{4} = \frac{1+1}{4}$$

$$\text{OD}_{LH} = \frac{1}{3}; \quad \text{OD}_{HL} = \frac{1}{k}$$

Identify the gate path from A to F

All gate inputs have FL = 1/2, Caps still have FL=C/C_{REF}

Plugin the above OD_{HL} and OD_{LH}

$$t_{PROP_i} = t_{REF} \cdot \text{FL}_{i+1} (1+3k \text{ or } k+3)$$

Propagation delay from A to F:

$$t_{PROP} = \frac{t_{REF}}{2} \sum_{i=1}^{n} \text{FL}_{i+1} (1+3k \text{ or } k+3)$$
End of Lecture 40
Equal rise-fall gates, no overdrive

In 0.5u proc $t_{\text{REF}}=20\text{ps}$, $C_{\text{REF}}=4fF, R_{\text{PDREF}}=2.5K$

(Note: This $C_{\text{OX}}$ is somewhat larger than that in the 0.5u ON process)

$20fF = \frac{C}{C_{\text{REF}}} \rightarrow 5$

$\sum_{i=2}^{5} \frac{3k+1}{4} \rightarrow \frac{13}{4}$

$\sum_{i=3}^{5} \frac{3k+1}{4} \rightarrow \frac{7}{4}$

$\sum_{i=3}^{5} \frac{3k+1}{4} \rightarrow \frac{10}{4}$

$\sum_{i=4}^{5} \frac{3k+1}{4} \rightarrow \frac{5}{4}$

$C \rightarrow \frac{50fF}{4fF} = 12.5$

$t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^{5} \text{FI}_{k+1}$

$t_{\text{PROP}} = t_{\text{REF}} (10.25 + 4.25 + 4.25 + 1.25 + 12.5)$

$t_{\text{PROP}} = 32.5t_{\text{REF}}$
Equal rise-fall gates, with overdrive

In 0.5μm process, $t_{REF} = 20\text{ps}$, $C_{REF} = 4\text{fF}$, $R_{PDREF} = 2.5\text{K}

(Note: This $C_{OX}$ is somewhat larger than that in the 0.5μm ON process)