EE 330
Lecture 41

Digital Circuits

- Propagation Delay With Multiple Levels of Logic
- Optimally driving large capacitive loads
Scaling widths of ALL devices by constant \((W_{\text{scaled}} = W \times \text{OD})\) will change “drive” capability relative to that of the reference inverter but not change relative value of \(t_{\text{HL}}\) and \(t_{\text{LH}}\)

\[
R_{PD} = \frac{L_1}{\mu_n C_{\text{OX}} W_1 (V_{DD} - V_{Tn})} \quad \Rightarrow \quad R_{PDOD} = \frac{L_1}{\mu_n C_{\text{OX}} [\text{OD} \cdot W_1] (V_{DD} - V_{Tn})} = \frac{R_{PD}}{\text{OD}}
\]

\[
R_{PU} = \frac{L_2}{\mu_p C_{\text{OX}} W_2 (V_{DD} + V_{Tp})} \quad \Rightarrow \quad R_{PUOD} = \frac{L_2}{\mu_p C_{\text{OX}} [\text{OD} \cdot W_2] (V_{DD} + V_{Tp})} = \frac{R_{PU}}{\text{OD}}
\]

Scaling widths of ALL devices by constant will change \(F_I\) by \(\text{OD}\)

\[
C_{IN} = C_{\text{OX}} (W_1 L_1 + W_2 L_2) \quad \Rightarrow \quad C_{INOD} = C_{\text{OX}} \left([\text{OD} \cdot W_1] L_1 + [\text{OD} \cdot W_2] L_2\right) = \text{OD} \cdot C_{IN}
\]
Review from Last Time

Propagation Delay with Over-drive Capability

Example

Compare the propagation delays. Assume the OD is 900 in the third case and 30 in the fourth case. Don’t worry about the extra inversion at this time.

\[ t_{\text{PROP}} = 900t_{\text{REF}} \]

\[ t_{\text{PROP}} = t_{\text{REF}} + 900t_{\text{REF}} = 901t_{\text{REF}} \]

\[ t_{\text{PROP}} = 900t_{\text{REF}} + t_{\text{REF}} = 901t_{\text{REF}} \]

\[ t_{\text{PROP}} = 30t_{\text{REF}} + 30t_{\text{REF}} = 60t_{\text{REF}} \]

Note: Dramatic reduction in \( t_{\text{PROP}} \) is possible
Will later determine what optimal number of stages and sizing is
Propagation Delay in Multiple-Levels of Logic with Stage Loading

F_{lk} denotes the total loading on stage k which is the sum of the F_{l} of all loading on stage k

Summary: Propagation delay from A to F:

\[ t_{PROP} = t_{REF} \sum_{k=1}^{n} \frac{F_{l(k+1)}}{OD_k} \]
Review from Last Time

Propagation Delay in Multiple-Levels of Logic with Stage Loading

Will consider an example with the five cases

- Equal rise/fall (no overdrive)
- Equal rise/fall with overdrive
- Minimum Sized
- Asymmetric Overdrive
- Combination of equal rise/fall, minimum size and overdrive

Will develop the analysis methods as needed
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Asymmetric Overdrive

\[ t_{PROP} = t_{HL} + t_{LH} = \frac{1}{2} t_{REF} F_i L \left( \frac{1}{OD_{HL}} + \frac{1}{OD_{LH}} \right) \]

When propagating through \( n \) stages:

\[ A \rightarrow G_1 \rightarrow G_2 \rightarrow G_3 \rightarrow \cdots \rightarrow G_n \rightarrow F \rightarrow \cdots \]

\( F_{ik} \) denotes the total loading on stage \( k \) which is the sum of the \( F_i \) of all loading on stage \( k \)

\[ t_{PROP} = t_{REF} \cdot \left( \frac{1}{2} \sum_{k=1}^{n} F_{i(k+1)} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right) \]
Propagation Delay in Multiple-Levels of Logic with Stage Loading and Overdrives

Will now consider A to F propagation for this circuit as an example with different overdrives

Review from Last Time
Equal rise-fall gates, no overdrive

<table>
<thead>
<tr>
<th>C_{IN}/C_{REF}</th>
<th>Inverter</th>
<th>NOR</th>
<th>NAND</th>
<th>Overdrive</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1</td>
<td>3k+1</td>
<td>4</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>3+k</td>
<td></td>
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<td></td>
</tr>
</tbody>
</table>

\[ t_{PROP} = t_{REF} \sum_{k=1}^{5} F_{k+1} \]
Review from Last Time

*Equal rise-fall gates, no overdrive*

In 0.5u proc $t_{REF}=20ps$, $C_{REF}=4fF, R_{PDREF}=2.5K$

(Note: This $C_{OX}$ is somewhat larger than that in the 0.5u ON process)

$t_{PROP} = t_{REF} \sum_{k=1}^{5} F_{k+1}$

$t_{PROP} = t_{REF} (10.25 + 4.25 + 4.25 + 1.25 + 12.5)$

$t_{PROP} = 32.5 t_{REF}$
Propagation Delay in Multiple-Levels of Logic with Stage Loading

*Equal rise-fall gates, with overdrive*

\[ t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^{n} \frac{F_{k+1}}{OD_k} \]

In 0.5u proc  \( t_{\text{REF}} = 20\text{ps} \),  
\( C_{\text{REF}} = 4\text{fF} \),  
\( R_{\text{PDREF}} = 2.5\text{K} \)

(Note: This \( C_{\text{OX}} \) is somewhat larger than that in the 0.5u ON process)
# Propagation Delay in Multiple-Levels of Logic with Stage Loading

**Equal rise-fall gates, with overdrive**

<table>
<thead>
<tr>
<th>$C_{IN}/C_{REF}$</th>
<th>Equal Rise/Fall</th>
<th>Equal Rise/Fall (with OD)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inverter</td>
<td>$1$</td>
<td>$OD$</td>
</tr>
<tr>
<td>NOR</td>
<td>$\frac{3k+1}{4}$</td>
<td>$\frac{3k+1}{4} \cdot OD$</td>
</tr>
<tr>
<td>NAND</td>
<td>$\frac{3+k}{4}$</td>
<td>$\frac{3+k}{4} \cdot OD$</td>
</tr>
<tr>
<td>Overdrive</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Inverter</td>
<td></td>
<td></td>
</tr>
<tr>
<td>HL</td>
<td>$1$</td>
<td>$OD$</td>
</tr>
<tr>
<td>LH</td>
<td>$1$</td>
<td>$OD$</td>
</tr>
<tr>
<td>NOR</td>
<td></td>
<td></td>
</tr>
<tr>
<td>HL</td>
<td>$1$</td>
<td>$OD$</td>
</tr>
<tr>
<td>LH</td>
<td>$1$</td>
<td>$OD$</td>
</tr>
<tr>
<td>NAND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>HL</td>
<td>$1$</td>
<td>$OD$</td>
</tr>
<tr>
<td>LH</td>
<td>$1$</td>
<td>$OD$</td>
</tr>
</tbody>
</table>

\[
\frac{t_{PROP}}{t_{REF}} = \sum_{k=1}^{n} \frac{F_{l(k+1)}}{OD_k}
\]

\[
t_{PROP} = t_{REF} \sum_{k=1}^{n} \frac{F_{k+1}}{OD_k}
\]
Equal rise-fall gates, with overdrive

\[
\begin{align*}
\text{PROP REF} & \quad \sum_{k=1}^{n} \frac{F_{i_{k+1}}}{\text{OD}_k} \\
t_{\text{PROP}} & = t_{\text{REF}} \left( \frac{14.25/8 + 13/1 + 4.25/6 + 5/1 + 12.5/4}{1} \right) \\
t_{\text{PROP}} & = 23.6 \ t_{\text{REF}} \\
\end{align*}
\]

In 0.5u proc \( t_{\text{REF}}=20\text{ps} \), \( C_{\text{REF}}=4\text{fF}, R_{\text{PDREF}}=2.5\text{K} \)

(Note: This \( C_{\text{OX}} \) is somewhat larger than that in the 0.5u ON process)

\[
\begin{align*}
F_{i2} & = 14.25 \\
F_{i3} & = 13 \\
F_{i4} & = 4.25 \\
F_{i5} & = 5 \\
F_{i6} & = 12.5 \\
\end{align*}
\]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

**Minimum-sized gates**

In 0.5μm process, \( t_{\text{REF}} = 20\text{ps}, \ C_{\text{REF}} = 4\text{fF}, R_{\text{PDREF}} = 2.5\text{K} \)

(Note: This \( C_{\text{OX}} \) is somewhat larger than that in the 0.5μm ON process)

\[ t_{\text{PROP}} = t_{\text{REF}} \cdot ? \]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Minimum-sized gates

\[ t_{\text{PROP}} = t_{\text{REF}} \cdot ? \]
Propagation Delay with Asymmetric Overdrive

\[ t_{\text{PROP}} = t_{\text{REF}} \cdot ? \]

\[ t_{\text{PROP}} = R_{PD} C_L + R_{PU} C_L \]

\[ t_{\text{PROP}} = \left( \frac{R_{PDREF}}{\text{OD}_{HL}} + \frac{R_{PDREF}}{\text{OD}_{LH}} \right) C_L \]

\[ t_{\text{PROP}} = R_{PDREF} \left( \frac{1}{\text{OD}_{HL}} + \frac{1}{\text{OD}_{LH}} \right) \left( C_{\text{REF}} F_{\text{LOAD}} \right) \]

\[ t_{\text{PROP}} = \left( \frac{1}{\text{OD}_{HL}} + \frac{1}{\text{OD}_{LH}} \right) \left( R_{PDREF} C_{\text{REF}} \right) F_{\text{LOAD}} \]

But recall

\[ t_{\text{REF}} = 2 C_{\text{REF}} R_{PDREF} \]

Thus

\[ t_{\text{PROP}} = \left( \frac{1}{\text{OD}_{HL}} + \frac{1}{\text{OD}_{LH}} \right) \left( \frac{t_{\text{REF}}}{2} \right) F_{\text{LOAD}} \]

Now, for \( k \) levels of logic

\[ t_{\text{PROP}} = \frac{t_{\text{REF}}}{2} \sum_{k=1}^{n} F_{l(k+1)} \left( \frac{1}{\text{OD}_{HLk}} + \frac{1}{\text{OD}_{LHk}} \right) \]

\[ t_{\text{PROP}} = t_{\text{REF}} \cdot \left( \frac{1}{2} \sum_{k=1}^{n} F_{l(k+1)} \left( \frac{1}{\text{OD}_{HLk}} + \frac{1}{\text{OD}_{LHk}} \right) \right) \]
Propagation Delay with Minimum-Sized Gates

\[ t_{\text{PROP}} = t_{\text{REF}} \cdot \left( \sum_{k=1}^{n} F_{i(k+1)} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right) \]

Still need \( OD_{HL} \) and \( OD_{LH} \) for minimum-sized gates

Still need \( F_i \)
Propagation Delay with minimum-sized gates

\[ F_I = 2C_{OX} W_{MIN} L_{MIN} \]

\[ C_{REF} = 4C_{OX} W_{MIN} L_{MIN} \]

\[ F_I = \frac{C_{REF}}{2} \]
## Propagation Delay in Multiple-Levels of Logic with Stage Loading

### Minimum-sized gates

<table>
<thead>
<tr>
<th>CIN/CREF</th>
<th>Equal Rise/Fall</th>
<th>Equal Rise/Fall (with OD)</th>
<th>Minimum Sized</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inverter</td>
<td>1</td>
<td>OD</td>
<td></td>
</tr>
<tr>
<td>NOR</td>
<td>(\frac{3k+1}{4})</td>
<td>(\frac{3k+1}{4} \cdot OD)</td>
<td></td>
</tr>
<tr>
<td>NAND</td>
<td>(\frac{3+k}{4})</td>
<td>(\frac{3+k}{4} \cdot OD)</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Overdrive</th>
<th>Inverter</th>
<th>HL</th>
<th>LH</th>
<th>NOR</th>
<th>HL</th>
<th>LH</th>
<th>NAND</th>
<th>HL</th>
<th>LH</th>
</tr>
</thead>
<tbody>
<tr>
<td>ODHL</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>OD LH</td>
<td>(\frac{1}{3k})</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

\[
\text{ODHL} = \frac{1}{k} \quad \text{OD LH} = \frac{1}{3}
\]

\[
\text{FI} = \frac{C_{REF}}{2}
\]

\[
\text{ODHL} = \frac{1}{k} \quad \text{OD LH} = \frac{1}{3}
\]
# Propagation Delay in Multiple-Levels of Logic with Stage Loading

## Minimum-sized gates

<table>
<thead>
<tr>
<th>C_IN/C_REF</th>
<th>Equal Rise/Fall</th>
<th>Equal Rise/Fall (with OD)</th>
<th>Minimum Sized</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inverter</td>
<td>1 (\frac{3k+1}{4})</td>
<td>OD (\frac{3k+1}{4} \cdot \text{OD})</td>
<td>1/2</td>
</tr>
<tr>
<td>NOR</td>
<td>3+k (\frac{4}{4})</td>
<td>3+k (\frac{4}{4} \cdot \text{OD})</td>
<td>1/2</td>
</tr>
<tr>
<td>NAND</td>
<td>3+k (\frac{4}{4})</td>
<td>3+k (\frac{4}{4} \cdot \text{OD})</td>
<td>1/2</td>
</tr>
</tbody>
</table>

Overdrive

<table>
<thead>
<tr>
<th>Inverter</th>
<th>HL 1</th>
<th>OD 1</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>LH 1</td>
<td>OD 1/3</td>
</tr>
<tr>
<td>NOR</td>
<td>HL 1</td>
<td>OD 1</td>
</tr>
<tr>
<td></td>
<td>LH 1</td>
<td>OD 1/3</td>
</tr>
<tr>
<td>NAND</td>
<td>HL 1</td>
<td>OD 1/k</td>
</tr>
<tr>
<td></td>
<td>LH 1</td>
<td>OD 1/3</td>
</tr>
</tbody>
</table>

| t_PROP/t_REF | \(\sum_{k=1}^{n} F(k+1)\) | \(\sum_{k=1}^{n} F(k+1) \cdot \text{OD}_k\) | \(\frac{1}{2} \sum_{k=1}^{n} F(k+1) \left(\frac{1}{\text{OD}_{HLk}} + \frac{1}{\text{OD}_{LHk}}\right)\) |

\[\text{OD}_{HL} = 1\]
\[\text{OD}_{LH} = \frac{1}{3k}\]

\[\text{OD}_{HL} = \frac{1}{k}\]
\[\text{OD}_{LH} = \frac{1}{3}\]

\[\text{F}_L = \frac{C_{\text{REF}}}{2}\]
Minimum-sized gates

\[ t_{\text{PROP}} = t_{\text{REF}} \cdot \left( \frac{1}{2} \sum_{k=1}^{5} F_{(k+1)} \left( \frac{1}{OD_{\text{HL}}^{k}} + \frac{1}{OD_{\text{LH}}^{k}} \right) \right) \]

\[ t_{\text{PROP}} = t_{\text{REF}} \cdot \frac{1}{2} \left( \frac{13}{2} (3 + 3) + 1(12 + 1) + 1(6 + 10) + \frac{1}{2} (9 + 1) + 12.5 (2 + 3) \right) \]

\[ t_{\text{PROP}} = 63.25 \cdot t_{\text{REF}} \]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Asymmetric-sized gates
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Asymmetric-sized gates

<table>
<thead>
<tr>
<th>C_{IN}/C_{REF}</th>
<th>Equal Rise/Fall</th>
<th>Equal Rise/Fall (with OD)</th>
<th>Minimum Sized</th>
<th>Asymmetric OD (OD_{HL}, OD_{LH})</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inverter</td>
<td>1</td>
<td>OD</td>
<td>1/2</td>
<td>OD_{HL} + 3 \cdot OD_{LH}</td>
</tr>
<tr>
<td>NOR</td>
<td>\frac{3k+1}{4}</td>
<td>\frac{3k+1}{4} \cdot OD</td>
<td>1/2</td>
<td>\frac{OD_{HL} + 3k \cdot OD_{LH}}{4}</td>
</tr>
<tr>
<td>NAND</td>
<td>\frac{3+k}{4}</td>
<td>\frac{3+k}{4} \cdot OD</td>
<td>1/2</td>
<td>\frac{k \cdot OD_{HL} + 3 \cdot OD_{LH}}{4}</td>
</tr>
<tr>
<td>Overdrive</td>
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</tr>
<tr>
<td>Inverter</td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HL</td>
<td>1</td>
<td>OD</td>
<td>1</td>
<td>OD_{HL}</td>
</tr>
<tr>
<td>LH</td>
<td>1</td>
<td>OD</td>
<td>1/3</td>
<td>OD_{LH}</td>
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<td></td>
<td></td>
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<tr>
<td>HL</td>
<td>1</td>
<td>OD</td>
<td>1</td>
<td>OD_{HL}</td>
</tr>
<tr>
<td>LH</td>
<td>1</td>
<td>OD</td>
<td>1/(3k)</td>
<td>OD_{LH}</td>
</tr>
<tr>
<td>NAND</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HL</td>
<td>1</td>
<td>OD</td>
<td>1/k</td>
<td>OD_{HL}</td>
</tr>
<tr>
<td>LH</td>
<td>1</td>
<td>OD</td>
<td>1/3</td>
<td>OD_{LH}</td>
</tr>
</tbody>
</table>

\[ t_{PROP} = t_{REF} \cdot \left( \frac{1}{2} \sum_{k=1}^{n} \frac{F_{(k+1)}}{OD_k} \right) \left( \frac{1}{OD_{HL_k}} + \frac{1}{OD_{LH_k}} \right) \]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Asymmetric-sized gates

\[ t_{\text{PROP}} = t_{\text{REF}} \cdot \left( \frac{1}{2} \sum_{k=1}^{5} \frac{F_{l(k+1)}}{\text{OD}_{\text{HLk}}} + \frac{1}{\text{OD}_{\text{LHk}}} \right) \]
Asymmetric-sized gates

(Note: This C_{OX} is somewhat larger than that in the 0.5μm ON process)

NAND: \( k \cdot \text{OD}_{HL} + 3 \cdot \text{OD}_{LH} \)

NOR: \( \frac{\text{OD}_{HL}}{4} + 3k \cdot \text{OD}_{LH} \)

\( \text{OD}_{HL} = \frac{1}{4} \)
\( \text{OD}_{LH} = \frac{1}{4} \)

\( C \rightarrow \frac{50\text{fF}}{4\text{fF}} = 12.5 \)

\( t_{\text{PROP}} = t_{\text{REF}} \cdot \left( \frac{1}{2} \sum_{k=1}^{5} F_{i(k+1)} \left( \frac{1}{\text{OD}_{HLk}} + \frac{1}{\text{OD}_{LHk}} \right) \right) \)

\( t_{\text{PROP}} = t_{\text{REF}} \cdot \left( \frac{1}{2} \left( \frac{63}{8} + \frac{29}{4} (1+1) + \frac{1}{2} (2+4) + \frac{77}{16} (1+1) + \frac{7}{2} (4+1) + 12.5 \left( \frac{1}{2} + \frac{1}{4} \right) \right) \right) \)

\( t_{\text{PROP}} = 44.6 \cdot t_{\text{REF}} \)
Propagation Delay in Multiple-Levels of Logic with Stage Loading

*Mixture of Minimum-sized gates, equal rise/fall gates and OD*

\[ t_{\text{PROP}} = t_{\text{REF}} \cdot ? \]
Driving Notation

- Equal rise/fall (no overdrive)
- Equal rise/fall with overdrive
- Minimum Sized
- Asymmetric Overdrive
Propagation Delay in Multiple-Levels of Logic with Stage Loading

*Mixture of Minimum-sized gates, equal rise/fall gates and OD*

\[ t_{PROP} = t_{REF} \cdot \left( \frac{1}{2} \sum_{k=1}^{5} F_{i(k+1)} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right) \]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

*Mixture of Minimum-sized gates, equal rise/fall gates and OD*

\[ t_{\text{PROP}} = t_{\text{REF}} \cdot \left( \frac{1}{2} \sum_{k=1}^{5} F \left( k+1 \right) \left( \frac{1}{O_{DHLk}} + \frac{1}{O_{DLHk}} \right) \right) \]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

- Equal rise/fall (no overdrive)
  \[ t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^{n} F_{l(k+1)} \]

- Equal rise/fall with overdrive
  \[ t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^{n} \frac{F_{l(k+1)}}{OD_k} \]

- Minimum Sized
  \[ t_{\text{PROP}} = t_{\text{REF}} \left( \frac{1}{2} \sum_{k=1}^{n} F_{l(k+1)} \left( \frac{1}{OD_{HL_k}} + \frac{1}{OD_{LH_k}} \right) \right) \]

- Asymmetric overdrive
  \[ t_{\text{PROP}} = t_{\text{REF}} \left( \frac{1}{2} \sum_{k=1}^{n} F_{l(k+1)} \left( \frac{1}{OD_{HL_k}} + \frac{1}{OD_{LH_k}} \right) \right) \]

- Combination of equal rise/fall, minimum size and overdrive
  \[ t_{\text{PROP}} = t_{\text{REF}} \left( \frac{1}{2} \sum_{k=1}^{n} F_{l(k+1)} \left( \frac{1}{OD_{HL_k}} + \frac{1}{OD_{LH_k}} \right) \right) \]
Driving Large Capacitive Loads

Example

Assume driving by a reference inverter

Assume $C_L = 1000C_{REF}$

$t_{PROP} = ?$

In 0.5u proc $t_{REF} = 20ps$, $C_{REF} = 4fF$, $R_{PDREF} = 2.5K$
Driving Large Capacitive Loads

Example

Assume driving by a reference inverter

Assume \( C_L = 1000C_{REF} \)

\[
t_{PROP} = 1000t_{REF}
\]

\( t_{PROP} \) is too long!

In 0.5u proc \( t_{REF} = 20\text{ps} \),
\( C_{REF} = 4fF, R_{PDREF} = 2.5K \)
Driving Large Capacitive Loads

Example

Assume first stage is a reference inverter

\[ t_{PROP} = \sum_{k=1}^{2} \frac{F_{I(k+1)}}{OD_k} \]

\[ t_{PROP} = t_{REF} \left( \frac{1}{1000} + \frac{1}{1000} \right) = t_{REF} (1000 + 1) \]

\[ t_{PROP} = t_{REF} (1001) \]

Delay of second inverter is really small but overall delay is even longer than before!
Driving Large Capacitive Loads

Example

Assume first stage is a reference inverter

Assume \( C_L = 1000C_{REF} \)

\[
\sum_{k=1}^{3} \frac{F_l(k+1)}{O_{D_k}} = \frac{1}{10} + \frac{1}{100} + \frac{1}{1000} = 0.1111
\]

\[
t_{\text{PROP}} = t_{\text{REF}} \left( 10 + 10 + 10 \right) = 30t_{\text{REF}}
\]

Dramatic reduction is propagation delay (over a factor of 30!)

What is the fastest way to drive a large capacitive load?
Optimal Driving of Capacitive Loads

Assume first stage is a reference inverter

Need to determine the number of stages, $n$, and the OD factors for each stage to minimize $t_{\text{PROP}}$.

$$t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^{n} \frac{F_l(k+1)}{OD_k}$$

where $\theta_0 = 1$, $\theta_n = \frac{C_L}{C_{\text{REF}}}$

This becomes an $n$-parameter optimization (minimization) problem!

Unknown parameters: $\{\theta_1, \theta_2, \ldots \theta_{n-1}, n\}$

An $n$-parameter nonlinear optimization problem is generally difficult !!!!
Optimal Driving of Capacitive Loads

Assume first stage is a reference inverter

\[ t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^{n} \frac{\theta_k}{\theta_{k-1}} \]

Order reduction strategy: Assume overdrive of stages increases by the same factor clear until the load

\[ \theta^n C_{\text{REF}} = C_L \]

This becomes a 2-parameter optimization (minimization) problem!

Unknown parameters: \( \{\theta, n\} \)

One constraint: \( \theta^n C_{\text{REF}} = C_L \)
Optimal Driving of Capacitive Loads

\[ t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^{n} \frac{\theta_k}{\theta_{k-1}} \]

\[ t_{\text{PROP}} = t_{\text{REF}} n \theta \]

Unknown parameters: \( \{\theta, n\} \)

Thus obtain an expression for \( t_{\text{PROP}} \) in terms of only \( \theta \)

\[ t_{\text{PROP}} = t_{\text{REF}} \frac{\theta}{\ln(\theta)} \left[ \ln \left( \frac{C_L}{C_{\text{REF}}} \right) \right] \]
Optimal Driving of Capacitive Loads

\[ t_{\text{PROP}} = t_{\text{REF}} \frac{\theta}{\ln(\theta)} \left[ \ln \frac{C_L}{C_{\text{REF}}} \right] \]

Is suffices to minimize the function \( f(\theta) = \frac{\theta}{\ln(\theta)} \)

\[
\frac{df}{d\theta} = -\theta \cdot \frac{1}{\theta} \cdot \frac{1}{\ln(\theta)} = 0
\]

\[
\ln(\theta) - 1 = 0 \quad \Rightarrow \quad \theta = e
\]

\[
n = \frac{1}{\ln(\theta)} \ln\left( \frac{C_L}{C_{\text{REF}}} \right) \quad \Rightarrow \quad n = \ln\left( \frac{C_L}{C_{\text{REF}}} \right)
\]
Optimal Driving of Capacitive Loads

\[ \theta_{\text{OPT}} = e \]

\[ n_{\text{OPT}} = \ln\left( \frac{C_L}{C_{\text{REF}}} \right) \]

\[ t_{\text{PROP}} = t_{\text{REF}} \frac{\theta}{\ln(\theta)} \left[ \ln \left( \frac{C_L}{C_{\text{REF}}} \right) \right] \]

\[ t_{\text{PROP}} = t_{\text{REF}} e \left[ \ln \left( \frac{C_L}{C_{\text{REF}}} \right) \right] = n\theta t_{\text{REF}} \]

\[ \theta^n C_{\text{REF}} = C_L \]
Optimal Driving of Capacitive Loads

- Minimum at $\theta = e$ but shallow inflection point for $2 < \theta < 3$
- Practically pick $\theta = 2$, $\theta = 2.5$, or $\theta = 3$
- Since optimization may provide non-integer for $n$, must pick close integer
Optimal Driving of Capacitive Loads

- Often termed a pad driver
- Often used to drive large internal busses as well
- Generally included in standard cells or in cell library
- Device sizes can become very large
- Odd number of stages will cause signal inversion but usually not a problem
End of Lecture 41