EE 330
Lecture 41
Digital Circuits

• Propagation Delay With Multiple Levels of Logic
• Optimally driving large capacitive loads
• Elmore Delays
Scaling widths of ALL devices by constant \((W_{\text{scaled}} = W \times OD)\) will change “drive” capability relative to that of the reference inverter but not change relative value of \(t_{\text{HL}}\) and \(t_{\text{LH}}\).

\[
R_{\text{PD}} = \frac{L_1}{\mu_n C_{\text{OX}} W_1 (V_{\text{DD}} - V_{\text{Th}})}
\]

\[
R_{\text{PDOD}} = \frac{L_1}{\mu_n C_{\text{OX}} [OD \cdot W_1] (V_{\text{DD}} - V_{\text{Th}})} = \frac{R_{\text{PD}}}{OD}
\]

\[
R_{\text{PU}} = \frac{L_2}{\mu_p C_{\text{OX}} W_2 (V_{\text{DD}} + V_{\text{Th}})}
\]

\[
R_{\text{PUOD}} = \frac{L_2}{\mu_p C_{\text{OX}} [OD \cdot W_2] (V_{\text{DD}} + V_{\text{Th}})} = \frac{R_{\text{PU}}}{OD}
\]

Scaling widths of ALL devices by constant will change \(F_I\) by \(OD\).

\[
C_{\text{IN}} = C_{\text{OX}} (W_1 L_1 + W_2 L_2)
\]

\[
C_{\text{INOD}} = C_{\text{OX}} \left( [OD \cdot W_1] L_1 + [OD \cdot W_2] L_2 \right) = OD \cdot C_{\text{IN}}
\]
Review from Last Time

Propagation Delay with Over-drive Capability

Example

Compare the propagation delays. Assume the OD is 900 in the third case and 30 in the fourth case. Don’t worry about the extra inversion at this time.

\[ t_{\text{PROP}} = 900t_{\text{REF}} \]

\[ t_{\text{PROP}} = t_{\text{REF}} + 900t_{\text{REF}} = 901t_{\text{REF}} \]

\[ t_{\text{PROP}} = 900t_{\text{REF}} + t_{\text{REF}} = 901t_{\text{REF}} \]

\[ t_{\text{PROP}} = 30t_{\text{REF}} + 30t_{\text{REF}} = 60t_{\text{REF}} \]

Note: Dramatic reduction in \( t_{\text{PROP}} \) is possible

Will later determine what optimal number of stages and sizing is
Propagation Delay in Multiple Levels of Logic with Stage Loading

\[ t_{PROP} = t_{REF} \sum_{k=1}^{n} \frac{F_{I(k+1)}}{OD_k} \]

Summary: Propagation delay from A to F:

Review from Last Time
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Will consider an example with the five cases

- Equal rise/fall (no overdrive)
- Equal rise/fall with overdrive
- Minimum Sized
- Asymmetric Overdrive
- Combination of equal rise/fall, minimum size and overdrive

Will develop the analysis methods as needed
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Asymmetric Overdrive

\[ t_{\text{PROP}} = t_{\text{HL}} + t_{\text{LH}} = \frac{1}{2} t_{\text{REF}} F_{iL} \left( \frac{1}{OD_{HL}} + \frac{1}{OD_{LH}} \right) \]

When propagating through \( n \) stages:

\[ F_{ik} \text{ denotes the total loading on stage } k \text{ which is the sum of the } F_i \text{ of all loading on stage } k \]

\[ t_{\text{PROP}} = t_{\text{REF}} \cdot \left( \frac{1}{2} \sum_{k=1}^{n} F_{i(k+1)} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right) \]
In 0.5u proc \( t_{\text{REF}} = 20\text{ps} \),
\( C_{\text{REF}} = 4\text{fF} \), \( R_{\text{PDREF}} = 2.5\text{K} \)

(Note: This \( C_{\text{OX}} \) is somewhat larger than that in the 0.5u ON process)

Review from Last Time

**Equal rise-fall gates, no overdrive**

\[ t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^{5} F_{k+1} \]

\[ t_{\text{PROP}} = t_{\text{REF}} (10.25 + 4.25 + 4.25 + 1.25 + 12.5) \]

\[ t_{\text{PROP}} = 32.5t_{\text{REF}} \]
Equal rise-fall gates, with overdrive

In 0.5u proc \( t_{\text{REF}}=20\,\text{ps} \),
\( C_{\text{REF}}=4\,\text{fF}, R_{\text{PDREF}}=2.5\,\text{K} \)

(Note: This \( C_{\text{OX}} \) is somewhat larger than that in the 0.5u ON process)
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Minimum-sized gates

In 0.5u proc \( t_{\text{REF}}=20\text{ps} \), \( C_{\text{REF}}=4\text{fF}, R_{\text{PDREF}}=2.5\text{K} \)

(Note: This \( C_{\text{OX}} \) is somewhat larger than that in the 0.5u ON process)
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Minimum-sized gates

Observe that a minimum-sized gate is simply a gate with asymmetric overdrive
Recall:

Propagation Delay with Minimum-Sized Gates

\[ t_{\text{PROP}} = t_{\text{REF}} \times \left( \frac{1}{2} \sum_{k=1}^{n} F_{i(k+1)} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right) \]

- Still need \( OD_{HL} \) and \( OD_{LH} \) for minimum-sized gates
- Still need \( F_{i} \)
Propogation Delay with minimum-sized gates

\[ OD_{HL} = 1 \]
\[ OD_{LH} = \frac{1}{3k} \]

\[ OD_{HL} = ? \]
\[ OD_{LH} = ? \]

\[ FI = 2C_{OX}W_{MIN}L_{MIN} \]
\[ C_{REF} = 4C_{OX}W_{MIN}L_{MIN} \]
\[ FI = \frac{C_{REF}}{2} \]
### Propagation Delay in Multiple-Levels of Logic with Stage Loading

#### Minimum-sized gates

<table>
<thead>
<tr>
<th>C(<em>{\text{IN/}})/C(</em>{\text{REF}})</th>
<th>Equal Rise/Fall</th>
<th>Equal Rise/Fall (with OD)</th>
<th>Minimum Sized</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inverter</td>
<td>1</td>
<td>OD</td>
<td></td>
</tr>
<tr>
<td>NOR</td>
<td>(\frac{3k+1}{4})</td>
<td>(\frac{3k+1}{4}) (\cdot) OD</td>
<td></td>
</tr>
<tr>
<td>NAND</td>
<td>(\frac{3+k}{4})</td>
<td>(\frac{3+k}{4}) (\cdot) OD</td>
<td></td>
</tr>
<tr>
<td>Overdrive</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Inverter</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HL</td>
<td>1</td>
<td>OD</td>
<td></td>
</tr>
<tr>
<td>LH</td>
<td>1</td>
<td>OD</td>
<td></td>
</tr>
<tr>
<td>NOR</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HL</td>
<td>1</td>
<td>OD</td>
<td></td>
</tr>
<tr>
<td>LH</td>
<td>1</td>
<td>OD</td>
<td></td>
</tr>
<tr>
<td>NAND</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HL</td>
<td>1</td>
<td>OD</td>
<td></td>
</tr>
<tr>
<td>LH</td>
<td>1</td>
<td>OD</td>
<td></td>
</tr>
<tr>
<td>t(<em>{\text{PROP/}})/t(</em>{\text{REF}})</td>
<td>(\sum_{k=1}^{n} F_{l(k+1)})</td>
<td>(\sum_{k=1}^{n} \frac{F_{l(k+1)}}{OD_k})</td>
<td></td>
</tr>
</tbody>
</table>

\(\text{OD}_{\text{HL}} = 1\)

\(\text{OD}_{\text{LH}} = 1/k\)

\(\text{OD}_{\text{LH}} = \frac{1}{3}\)

\(F_I = \frac{C_{\text{REF}}}{2}\)
### Propagation Delay in Multiple-Levels of Logic with Stage Loading

**Minimum-sized gates**

<table>
<thead>
<tr>
<th>C&lt;sub&gt;IN&lt;/sub&gt;/C&lt;sub&gt;REF&lt;/sub&gt;</th>
<th>Equal Rise/Fall</th>
<th>Equal Rise/Fall (with OD)</th>
<th>Minimum Sized</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inverter</td>
<td>1</td>
<td>OD</td>
<td>1/2</td>
</tr>
<tr>
<td>NOR</td>
<td>(\frac{3k+1}{4})</td>
<td>OD (\cdot \text{OD})</td>
<td>1/2</td>
</tr>
<tr>
<td>NAND</td>
<td>(\frac{3+k}{4})</td>
<td>OD (\cdot \text{OD})</td>
<td>1/2</td>
</tr>
<tr>
<td>Overdrive</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Inverter</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HL</td>
<td>1</td>
<td>OD</td>
<td>1</td>
</tr>
<tr>
<td>LH</td>
<td>1</td>
<td>OD</td>
<td>1/3</td>
</tr>
<tr>
<td>NOR</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HL</td>
<td>1</td>
<td>OD</td>
<td>1</td>
</tr>
<tr>
<td>LH</td>
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<td>OD</td>
<td>1/3</td>
</tr>
<tr>
<td>NAND</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HL</td>
<td>1</td>
<td>OD</td>
<td>1/k</td>
</tr>
<tr>
<td>LH</td>
<td>1</td>
<td>OD</td>
<td>1/3</td>
</tr>
</tbody>
</table>

\[
\sum_{k=1}^{n} \frac{F_{1(k+1)}}{OD_k} = \frac{1}{2} \sum_{k=1}^{n} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right)
\]
Minimum-sized gates

\[ t_{PROP} = t_{REF} \cdot \frac{1}{2} \sum_{k=1}^{5} F_{(k+1)} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \]

\[ t_{PROP} = t_{REF} \cdot \frac{1}{2} \left( \frac{13}{2} (3 + 3) + 1(12 + 1) + 1(6 + 10) + \frac{1}{2} (9 + 1) + 12.5(2 + 3) \right) \]

\[ t_{PROP} = 63.25 \cdot t_{REF} \]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Asymmetric-sized gates

\[ t_{\text{PROP}} = t_{\text{REF}} \cdot ? \]
## Propagation Delay in Multiple-Levels of Logic with Stage Loading

### Asymmetric-sized gates

<table>
<thead>
<tr>
<th>C&lt;sub&gt;IN&lt;/sub&gt;/C&lt;sub&gt;REF&lt;/sub&gt;</th>
<th>Equal Rise/Fall</th>
<th>Equal Rise/Fall (with OD)</th>
<th>Minimum Sized</th>
<th>Asymmetric OD (OD&lt;sub&gt;HL&lt;/sub&gt;, OD&lt;sub&gt;LH&lt;/sub&gt;)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inverter</td>
<td>1, 3k+1/4</td>
<td>OD, 3k+1/4 OD</td>
<td>1/2</td>
<td>OD&lt;sub&gt;HL&lt;/sub&gt;+3k OD&lt;sub&gt;LH&lt;/sub&gt;/4</td>
</tr>
<tr>
<td>NOR</td>
<td>3+k/4</td>
<td>3+k/4 OD</td>
<td>1/2</td>
<td>OD&lt;sub&gt;HL&lt;/sub&gt;+3 OD&lt;sub&gt;LH&lt;/sub&gt;/4</td>
</tr>
<tr>
<td>NAND</td>
<td>3+k/4</td>
<td>3+k/4 OD</td>
<td>1/2</td>
<td>k OD&lt;sub&gt;HL&lt;/sub&gt;+3 OD&lt;sub&gt;LH&lt;/sub&gt;/4</td>
</tr>
</tbody>
</table>

### Overdrive

<table>
<thead>
<tr>
<th>C&lt;sub&gt;IN&lt;/sub&gt;/C&lt;sub&gt;REF&lt;/sub&gt;</th>
<th>Equal Rise/Fall</th>
<th>Equal Rise/Fall (with OD)</th>
<th>Minimum Sized</th>
<th>Asymmetric OD (OD&lt;sub&gt;HL&lt;/sub&gt;, OD&lt;sub&gt;LH&lt;/sub&gt;)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inverter</td>
<td>1, 3k+1/4</td>
<td>OD, 3k+1/4 OD</td>
<td>1/2</td>
<td>OD&lt;sub&gt;HL&lt;/sub&gt;+3k OD&lt;sub&gt;LH&lt;/sub&gt;/4</td>
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<td>k OD&lt;sub&gt;HL&lt;/sub&gt;+3 OD&lt;sub&gt;LH&lt;/sub&gt;/4</td>
</tr>
</tbody>
</table>

### t<sub>PROP</sub>/t<sub>REF</sub>

\[
\sum_{k=1}^{n} \frac{F_{(k+1)}}{OD_k} \quad \sum_{k=1}^{n} \frac{F_{(k+1)}}{OD_k} \quad \frac{1}{2} \sum_{k=1}^{n} F_{(k+1)} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \quad \frac{1}{2} \sum_{k=1}^{n} F_{(k+1)} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right)
\]

\[
t_{PROP} = t_{REF} \cdot \left( \frac{1}{2} \sum_{k=1}^{5} F_{(k+1)} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right)
\]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Asymmetric-sized gates

\[ t_{\text{PROP}} = t_{\text{REF}} \left( \sum_{k=1}^{5} \frac{F_{l(k+1)}}{2} \left( \frac{1}{\text{OD}_{\text{HLk}}} + \frac{1}{\text{OD}_{\text{LHk}}} \right) \right) \]
Asymmetric-sized gates

(Note: This $C_{OX}$ is somewhat larger than that in the 0.5μm ON process)

\[
\begin{align*}
\text{NAND:} & \quad k \cdot \text{OD}_{HL} + 3 \cdot \text{OD}_{LH} \\
\text{NOR:} & \quad \text{OD}_{HL} + 3k \cdot \text{OD}_{LH}
\end{align*}
\]

\[
\begin{align*}
\text{OD}_{HL} &= 4 \\
\text{OD}_{LH} &= 1/4 \\
\text{OD}_{HL} &= 1 \\
\text{OD}_{LH} &= 1 \\
\text{OD}_{HL} &= 4 \\
\text{OD}_{LH} &= 2
\end{align*}
\]

\[
\begin{align*}
F_{I2} &= 63/8 \\
F_{I3} &= 29/4 \\
F_{I4} &= 77/16 \\
F_{I5} &= 7/2 \\
F_{I6} &= 12.5
\end{align*}
\]

\[
t_{PROP} = t_{REF} \cdot \left( \frac{1}{2} \sum_{k=1}^{5} F_{I(k+1)} \left( \frac{1}{\text{OD}_{HLk}} + \frac{1}{\text{OD}_{LHk}} \right) \right)
\]

\[
t_{PROP} = 44.6 \cdot t_{REF}
\]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Mixture of Minimum-sized gates, equal rise/fall gates and OD

\[ t_{\text{PROP}} = t_{\text{REF}} \cdot ? \]
Driving Notation

- Equal rise/fall (no overdrive)
- Equal rise/fall with overdrive
- Minimum Sized
- Asymmetric Overdrive
Propagation Delay in Multiple-Levels of Logic with Stage Loading

*Mixture of Minimum-sized gates, equal rise/fall gates and OD*

\[ t_{\text{PROP}} = t_{\text{REF}} \cdot \left( \frac{1}{2} \sum_{k=1}^{5} F_{i(k+1)} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right) \]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Mixture of Minimum-sized gates, equal rise/fall gates and OD

\[
\begin{align*}
&\sum_{k=1}^{5} F_{(k+1)} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \\
&t_{\text{PROP}} = t_{\text{REF}} \cdot \left( \frac{1}{2} \sum_{k=1}^{5} F_{(k+1)} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right)
\end{align*}
\]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

- Equal rise/fall (no overdrive)
- Equal rise/fall with overdrive
- Minimum Sized
- Asymmetric overdrive
- Combination of equal rise/fall, minimum size and overdrive

\[ t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^{n} F_{l(k+1)} \]

where

- For equal rise/fall (no overdrive)
- For equal rise/fall with overdrive
- For minimum sized
- For asymmetric overdrive
- For combination of equal rise/fall, minimum size and overdrive
Driving Large Capacitive Loads

Example

Assume driving by a reference inverter

\[ C_L = 1000C_{REF} \]

Assume \( t_{PROP} = ? \)

In 0.5u proc \( t_{REF} = 20\text{ps} \),
\( C_{REF} = 4\text{fF}, R_{PDREF} = 2.5\text{K} \)
Driving Large Capacitive Loads

Example

Assume driving by a reference inverter

Assume $C_L = 1000 C_{REF}$

$t_{PROP} = 1000 t_{REF}$

$t_{PROP}$ is too long!

In 0.5u process $t_{REF} = 20$ps,
$C_{REF} = 4fF, R_{PDREF} = 2.5K$
Driving Large Capacitive Loads

Example

Assume first stage is a reference inverter

Assume \( C_L = 1000C_{REF} \)

\[ t_{PROP} = \sum_{k=1}^{2} \frac{F_{I(k+1)}}{OD_k} \]

\[ t_{PROP} = t_{REF} \left( \frac{1}{1000} + \frac{1}{1000} \right) = t_{REF} (1000 + 1) \]

\[ t_{PROP} = t_{REF} (1001) \]

Delay of second inverter is really small but overall delay is even longer than before!
Driving Large Capacitive Loads

Example

Assume first stage is a reference inverter

Assume \( C_L = 1000C_{REF} \)

\[
\begin{align*}
 t_{PROP} &= t_{REF} \sum_{k=1}^{3} \frac{F_{l(k+1)}}{OD_k} \\
 &= t_{REF} \left( \frac{1}{10} + \frac{1}{100} + \frac{1}{1000} \right) = t_{REF} (10 + 10 + 10) \\
 t_{PROP} &= 30t_{REF}
\end{align*}
\]

Dramatic reduction is propagation delay (over a factor of 30!)

What is the fastest way to drive a large capacitive load?
Optimal Driving of Capacitive Loads

Assume first stage is a reference inverter

Need to determine the number of stages, \( n \), and the OD factors for each stage to minimize \( t_{\text{PROP}} \).

\[
 t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^{n} \frac{F_{l(k+1)}}{OD_k}
\]

where \( \theta_0 = 1 \), \( \theta_n = C_L/C_{\text{REF}} \)

This becomes an \( n \)-parameter optimization (minimization) problem!

Unknown parameters: \( \{\theta_1, \theta_2, ..., \theta_{n-1}, n\} \)

An \( n \)-parameter nonlinear optimization problem is generally difficult !!!!
Optimal Driving of Capacitive Loads

Assume first stage is a reference inverter

Order reduction strategy: Assume overdrive of stages increases by the same factor clear until the load

\[ t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^{n} \frac{\theta_k}{\theta_{k-1}} \]

This becomes a 2-parameter optimization (minimization) problem!

Unknown parameters: \( \{\theta, n\} \)

One constraint: \( \theta^n C_{\text{REF}} = C_L \)

One degree of freedom
Optimal Driving of Capacitive Loads

\[ t_{PROP} = t_{REF} \sum_{k=1}^{n} \frac{\theta_k}{\theta_{k-1}} \]

Unknown parameters: \( \{\theta, n\} \)

Thus obtain an expression for \( t_{PROP} \) in terms of only \( \theta \)

\[ t_{PROP} = t_{REF} \frac{\theta}{\ln(\theta)} \left[ \ln \left( \frac{C_L}{C_{REF}} \right) \right] \]
Optimal Driving of Capacitive Loads

\[ t_{\text{PROP}} = t_{\text{REF}} \frac{\theta}{\ln(\theta)} \left[ \ln \frac{C_L}{C_{\text{REF}}} \right] \]

It suffices to minimize the function \[ f(\theta) = \frac{\theta}{\ln(\theta)} \]

\[ \frac{df}{d\theta} = \frac{\ln(\theta) - \theta \cdot \left( \frac{1}{\theta} \right)}{(\ln(\theta))^2} = 0 \]

\[ \ln(\theta) - 1 = 0 \quad \rightarrow \quad \theta = e \]

\[ n = \frac{1}{\ln(\theta)} \ln \left( \frac{C_L}{C_{\text{REF}}} \right) \quad \rightarrow \quad n = \ln \left( \frac{C_L}{C_{\text{REF}}} \right) \]
Optimal Driving of Capacitive Loads

\[ \theta_{\text{OPT}} = e \]

\[ n_{\text{OPT}} = \ln \left( \frac{C_L}{C_{\text{REF}}} \right) \]

\[ t_{\text{PROP}} = t_{\text{REF}} \frac{\theta}{\ln(\theta)} \left[ \ln \left( \frac{C_L}{C_{\text{REF}}} \right) \right] \]

\[ t_{\text{PROP}} = t_{\text{REF}} e \left[ \ln \left( \frac{C_L}{C_{\text{REF}}} \right) \right] = n\theta t_{\text{REF}} \]
Optimal Driving of Capacitive Loads

\[ f = \frac{\theta}{\ln(\theta)} \]

- minimum at \( \theta = e \) but shallow inflection point for \( 2 < \theta < 3 \)
- practically pick \( \theta = 2, \theta = 2.5, \) or \( \theta = 3 \)
- since optimization may provide non-integer for \( n \), must pick close integer
Optimal Driving of Capacitive Loads

- Often termed a pad driver
- Often used to drive large internal busses as well
- Generally included in standard cells or in cell library
- Device sizes can become very large
- Odd number of stages will cause signal inversion but usually not a problem
Example: Design a pad driver for driving a load capacitance of 10pF, determine $t_{\text{PROP}}$ for the pad driver, and compare this with the propagation delay for driving the pad with a minimum-sized reference inverter.

In 0.5μm process $t_{\text{REF}}=20\text{ps}$, $C_{\text{REF}}=4\text{fF}$, $R_{\text{PDREF}}=2.5\text{KΩ}$

$$n_{\text{OPT}} = \ln \left( \frac{C_L}{C_{\text{REF}}} \right) = \ln \left( \frac{10\text{pF}}{4\text{fF}} \right) = 7.8$$

Select $n=8$, $\theta=2.5$

$$W_{nk} = 2.5^{k-1}, \quad W_{pk} = 3 \cdot 2.5^{k-1}$$
Optimal Driving of Capacitive Loads

Example: Design a pad driver for driving a load capacitance of 10pF, determine $t_{\text{PROP}}$ for the pad driver, and compare this with the propagation delay for driving the pad with a minimum-sized reference inverter.

In 0.5μm process $t_{\text{REF}}=20\text{ps}$, $C_{\text{REF}}=4\text{fF}, R_{\text{PDREF}}=2.5\text{kΩ}$

$W_{nk}=2.5^k\cdot1^{-1}$, $W_{pk} = 3 \cdot 2.5^k\cdot1^{-1}$

$L_n=L_p=L_{\text{MIN}}$

<table>
<thead>
<tr>
<th>k</th>
<th>n-channel</th>
<th>p-channel</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1 $W_{\text{MIN}}$</td>
<td>3 $W_{\text{MIN}}$</td>
</tr>
<tr>
<td>2</td>
<td>2.5 $W_{\text{MIN}}$</td>
<td>7.5 $W_{\text{MIN}}$</td>
</tr>
<tr>
<td>3</td>
<td>6.25 $W_{\text{MIN}}$</td>
<td>18.75 $W_{\text{MIN}}$</td>
</tr>
<tr>
<td>4</td>
<td>15.6 $W_{\text{MIN}}$</td>
<td>46.9 $W_{\text{MIN}}$</td>
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<td>5</td>
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<td>117.2 $W_{\text{MIN}}$</td>
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<tr>
<td>6</td>
<td>97.7 $W_{\text{MIN}}$</td>
<td>293.0 $W_{\text{MIN}}$</td>
</tr>
<tr>
<td>7</td>
<td>244.1 $W_{\text{MIN}}$</td>
<td>732.4 $W_{\text{MIN}}$</td>
</tr>
<tr>
<td>8</td>
<td>610.4 $W_{\text{MIN}}$</td>
<td>1831.1 $W_{\text{MIN}}$</td>
</tr>
</tbody>
</table>

Note devices in last stage are very large!
Optimal Driving of Capacitive Loads

Example: Design a pad driver for driving a load capacitance of 10pF, determine $t_{PROP}$ for the pad driver, and compare this with the propagation delay for driving the pad with a minimum-sized reference inverter.

In 0.5μm proc $t_{REF}=20$ps, $C_{REF}=4fF, R_{PDREF}=2.5K$

$W_{nk}=2.5^{k-1}, \quad W_{pk} = 3 \cdot 2.5^{k-1}$

$t_{PROP} \approx n\theta t_{REF} = 8 \cdot 2.5 \cdot t_{REF} = 20t_{REF}$

More accurately:

$$t_{PROP} = t_{REF} \left( \sum_{k=1}^{7} \frac{1}{\theta^k} \frac{C_L}{C_{REF}} \right) = t_{REF} \left( 17.5 + \frac{1}{610} \frac{2500}{2500} \right) = 21.6t_{REF}$$
Example: Design a pad driver for driving a load capacitance of 10pF, determine $t_{\text{PROP}}$ for the pad driver, and compare this with the propagation delay for driving the pad with a minimum-sized reference inverter.

In 0.5μm proc $t_{\text{REF}}=20\text{ps}$, $C_{\text{REF}}=4\text{fF}$, $R_{\text{PDREF}}=2.5\text{K}$

$W_{nk}=2.5^{k-1}$, $W_{pk} = 3 \cdot 2.5^{k-1}$

If driven directly with the minimum-sized reference inverter

$t_{\text{PROP}} = t_{\text{REF}} \frac{C_L}{C_{\text{REF}}} = 2500t_{\text{REF}}$

Note an improvement in speed by a factor of

$r = \frac{2500}{20} = 125$
Optimal Driving of Capacitive Loads

Example: Design a pad driver for driving a load capacitance of 10pF, determine $t_{\text{PROP}}$ for the pad driver, and compare this with the propagation delay for driving the pad with a minimum-sized reference inverter.

In 0.5μm process, $t_{\text{REF}}=20\text{ps}$, $C_{\text{REF}}=4\text{fF}$, $R_{\text{PDREF}}=2.5k\Omega$

$W_{nk}=2.5^{k-1}$, $W_{pk} = 3 \cdot 2.5^{k-1}$

$L_n = L_p = L_{\text{MIN}}$

<table>
<thead>
<tr>
<th>$k$</th>
<th>n-channel</th>
<th>p-channel</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1 $W_{\text{MIN}}$</td>
<td>3 $W_{\text{MIN}}$</td>
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<tr>
<td>2</td>
<td>2.5 $W_{\text{MIN}}$</td>
<td>7.5 $W_{\text{MIN}}$</td>
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<td>3</td>
<td>6.25 $W_{\text{MIN}}$</td>
<td>18.75 $W_{\text{MIN}}$</td>
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Note devices in last stage are very large!
Pad Driver Size Implications

Consider a 7-stage pad driver and assume $\theta = 3$
Area of Last Stage Larger than that of all previous stages combined!
End of Lecture 41