EE 330
Lecture 41
Digital Circuits

• Propagation Delay With Multiple Levels of Logic
• Optimally driving large capacitive loads
Propagagation Delay in Multiple-Levels of Logic with Stage Loading

Analysis strategy: Express delays in terms of those of reference inverter

\[ C_{\text{REF}} = C_{\text{IN}} = 4C_{\text{OX}} W_{\text{MIN}} L_{\text{MIN}} \]

\[ F_1 = 1 \]

\[ R_{\text{PDREF}} = \frac{L_{\text{MIN}}}{\mu_n C_{\text{OX}} W_{\text{MIN}} (V_{DD} - V_{Tn})} = \frac{L_{\text{MIN}}}{\mu_n C_{\text{OX}} W_{\text{MIN}} (0.8V_{DD})} \]

\[ t_{\text{REF}} = t_{\text{HLREF}} + t_{\text{LHREF}} = 2R_{\text{PDREF}} C_{\text{REF}} \]

\[ = (RC)_{\text{HL}} + (RC)_{\text{LH}} \]

\[ = 0.5t_{\text{REF}} + 0.5t_{\text{REF}} \]

Reference Inverter

Assume \( \mu_n/\mu_p = 3 \)

\( W_n = W_{\text{MIN}}, \quad W_p = 3W_{\text{MIN}} \)

In 0.5u proc \( t_{\text{REF}} = 20\text{ps}, \quad C_{\text{REF}} = 4\text{fF}, R_{\text{PDREF}} = 2.5\text{K} \)
Propagation Delay Through Multiple Stages of Logic with Stage Loading

(All gates sized for equal worse-case rise/fall time as that of reference inverter)

\[ t_{PROP_i} = t_{REF} \cdot F_{I(i+1)} \]

\[ t_{PROP} = t_{REF} \sum_{i=1}^{n} F_{I(i+1)} \]

Review from Last Time
Define the (Asymmetric) Overdrive Factors of a gate to be the factors by which PU and PD resistors are scaled down relative to those of the reference inverter.

If scaled by the same factor:

\[ \text{OD}_{HL} = \text{OD}_{LH} = \text{OD} \]

\[ t_{HL} = t_{LH} = \frac{R_{PDREF}}{OD} \cdot C_{L} = \frac{R_{PDREF} \cdot C_{REF} \cdot t_{REF}}{OD} = \frac{R_{PDREF}}{OD} \cdot C_{L} = \frac{R_{PDREF} \cdot C_{REF} \cdot t_{REF}}{OD} \]

\[ t_{PROP} = t_{HL} + t_{LH} = t_{REF} \cdot \frac{F_{L}}{OD} \cdot \left( \frac{1}{OD_{HL}} + \frac{1}{OD_{LH}} \right) \]

OD's may be larger or smaller than 1
Propagation Delay Through Multiple Stages of Logic with Stage Loading

Each gate has symmetric overdrive relative to that of reference inverter.

Identify each gate’s FI

\[ F_{\text{NOR}_i} = OD_i \left( \frac{3k_i + 1}{4} \right) \]

\[ F_{\text{NAND}_i} = OD_i \left( \frac{3 + k_i}{4} \right) \]

Identify each gate’s delay

\[ t_{\text{PROP}_k} = t_{\text{REF}} \frac{F_{i+1}}{OD_i} \]

\[ F_{i+1} \) is the total FI at the output of \( G_i \)

Propagation delay from A to F:

\[ t_{\text{PROP}} = t_{\text{REF}} \sum_{i=1}^{n} \frac{F_{i+1}}{OD_i} \]
Propagation Delay Through Multiple Stages of Logic with Stage Loading

Each gate has possibly asymmetric overdrives

Identify each gate’s FI:

\[
F_{\text{NOR}_i} = \frac{3k_iOD_{LH_i} + 1 \cdot OD_{HL_i}}{4} \]

\[
F_{\text{NAND}_i} = \frac{3OD_{LH_i} + k_iOD_{HL_i}}{4} \]

Identify each gate’s delay:

\[
t_{\text{PROP}_i} = \frac{t_{\text{REF}}}{2} F_{\text{I}(i+1)} \left( \frac{1}{OD_{HL_i}} + \frac{1}{OD_{LH_i}} \right)
\]

\[F_{\text{I}(i+1)} \] is the total FI at the output of \( G_i \)

Propagation delay from A to F:

\[
t_{\text{PROP}} = \frac{t_{\text{REF}}}{2} \sum_{i=1}^{n} F_{\text{I}(i+1)} \left( \frac{1}{OD_{HL_i}} + \frac{1}{OD_{LH_i}} \right)
\]
Propagation Delay Through Multiple Stages of Logic with Stage Loading

Minimum size strategy:

Minimum sized gate has $\text{FI} = 1/2$. Caps still have $\text{FI} = C/C_{\text{REF}}$

$$\text{FI}_{\text{NOR}} = \frac{3k_i \text{OD}_{LH_i} + 1 \cdot \text{OD}_{HL_i}}{4} = \frac{1 + 1}{4}$$

$\text{OD}_{LH} = 1/3k; \text{OD}_{HL} = 1$

$$\text{FI}_{\text{NAND}} = \frac{3 \text{OD}_{LH_i} + k_i \text{OD}_{HL_i}}{4} = \frac{1 + 1}{4}$$

$\text{OD}_{LH} = 1/3; \text{OD}_{HL} = 1/k$

NOR gate delay $t_{\text{PROP}} = \frac{t_{\text{REF}}}{2} \text{FI}_{i+1} (1+3k)$

NAND gate delay $t_{\text{PROP}} = \frac{t_{\text{REF}}}{2} \text{FI}_{i+1} (k+3)$

Propagation delay from A to F:

$$t_{\text{PROP}} = \frac{t_{\text{REF}}}{2} \sum_{i=1}^{n} \text{FI}_{i+1} \left( \frac{1}{\text{OD}_{HL_i}} + \frac{1}{\text{OD}_{LH_i}} \right)$$
Propagation Delay in Multiple-Levels of Logic with Stage Loading and Overdrives

*Will now consider A to F propagation for this circuit as an example with different overdrives*
Propagation Delay in Multiple-Levels of Logic with Stage Loading

*Equal rise-fall gates, no overdrive*

\[ t_{REF} = 2t_{HL_{REF}} \]

\[ t_{PROP} = t_{REF} \sum_{i=1}^{n} F_{I_{i+1}} \]

In 0.5u proc \( t_{REF} = 20 \text{ps}, C_{REF} = 4\text{fF}, R_{PD_{REF}} = 2.5\text{K} \)
## Propagation Delay in Multiple-Levels of Logic with Stage Loading

*Equal rise-fall gates, no overdrive*

<table>
<thead>
<tr>
<th></th>
<th>Equal Rise/Fall</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{IN}/C_{REF}$</td>
<td></td>
</tr>
<tr>
<td>Inverter</td>
<td>1</td>
</tr>
<tr>
<td>NOR</td>
<td>$\frac{3k+1}{4}$</td>
</tr>
<tr>
<td>NAND</td>
<td>$\frac{3+k}{4}$</td>
</tr>
<tr>
<td>Overdrive</td>
<td></td>
</tr>
<tr>
<td>Inverter</td>
<td></td>
</tr>
<tr>
<td>HL</td>
<td>1</td>
</tr>
<tr>
<td>LH</td>
<td>1</td>
</tr>
<tr>
<td>NOR</td>
<td></td>
</tr>
<tr>
<td>HL</td>
<td>1</td>
</tr>
<tr>
<td>LH</td>
<td>1</td>
</tr>
<tr>
<td>NAND</td>
<td></td>
</tr>
<tr>
<td>HL</td>
<td>1</td>
</tr>
<tr>
<td>LH</td>
<td>1</td>
</tr>
<tr>
<td>$t_{PROP}/t_{REF}$</td>
<td>$\sum_{i=1}^{n} F_{(i+1)}$</td>
</tr>
<tr>
<td></td>
<td>$t_{PROP}=t_{REF} \sum_{i=1}^{5} F_{(i+1)}$</td>
</tr>
</tbody>
</table>
Equal rise-fall gates, no overdrive

In 0.5u proc \( t_{REF}=20\text{ps}, \quad C_{REF}=4\text{fF}, R_{PDREF}=2.5\text{K}\)

(Note: This \( C_{OX} \) is somewhat larger than that in the 0.5u ON process)
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Equal rise-fall gates, with symmetric overdrive

In 0.5u proc $t_{REF}=20\text{ps}$,
$C_{REF}=4\text{fF}, R_{PDREF}=2.5\text{K}$

(Note: This $C_{OX}$ is somewhat larger than that in the 0.5u ON process)

$\sum_{i=1}^{n} \frac{F_{I(i+1)}}{OD_i}$
Propagation Delay in Multiple-Levels of Logic with Stage Loading

**Equal rise-fall gates, with overdrive**

<table>
<thead>
<tr>
<th>$C_{IN}/C_{REF}$</th>
<th>Equal Rise/Fall</th>
<th>Equal Rise/Fall (with OD)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inverter</td>
<td>1</td>
<td>$\frac{3k+1}{4} \cdot OD$</td>
</tr>
<tr>
<td>NOR</td>
<td>$\frac{3+k}{4}$</td>
<td>$\frac{3+k}{4} \cdot OD$</td>
</tr>
<tr>
<td>NAND</td>
<td>$\frac{3+k}{4}$</td>
<td>$\frac{3+k}{4} \cdot OD$</td>
</tr>
<tr>
<td>Overdrive</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Inverter</td>
<td></td>
<td></td>
</tr>
<tr>
<td>HL</td>
<td>1</td>
<td>$OD$</td>
</tr>
<tr>
<td>LH</td>
<td>1</td>
<td>$OD$</td>
</tr>
<tr>
<td>NOR</td>
<td></td>
<td></td>
</tr>
<tr>
<td>HL</td>
<td>1</td>
<td>$OD$</td>
</tr>
<tr>
<td>LH</td>
<td>1</td>
<td>$OD$</td>
</tr>
<tr>
<td>NAND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>HL</td>
<td>1</td>
<td>$OD$</td>
</tr>
<tr>
<td>LH</td>
<td>1</td>
<td>$OD$</td>
</tr>
<tr>
<td>$t_{PROP}/t_{REF}$</td>
<td>$\sum_{i=1}^{n} F_{I(i+1)}$</td>
<td>$\sum_{i=1}^{n} \frac{F_{I(i+1)}}{OD_i}$</td>
</tr>
</tbody>
</table>

$$t_{PROP} = t_{REF} \sum_{i=1}^{n} \frac{F_{I(i+1)}}{OD_i}$$
Equal rise-fall gates, with overdrive

\[ F_{\text{NOR}_i} = OD_i \left( \frac{3k_i + 1}{4} \right) \]

\[ F_{\text{NAND}_i} = OD_i \left( \frac{3 + k_i}{4} \right) \]

\[ F_{i}^{2} = 14.25 \]

\[ F_{i}^{3} = 13 \]

\[ F_{i}^{4} = 4.25 \]

\[ F_{i}^{5} = 5 \]

\[ F_{i}^{6} = 12.5 \]

In 0.5μm process, \( t_{\text{REF}} = 20\,\text{ps} \), \( C_{\text{REF}} = 4\,\text{fF}, R_{\text{PDREF}} = 2.5\,\text{K} \)

(Note: This \( C_{\text{OX}} \) is somewhat larger than that in the 0.5μm ON process)
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Minimum-sized gates

In 0.5u proc \( t_{\text{REF}}=20\text{ps}, \)
\( C_{\text{REF}}=4\text{fF}, R_{\text{PDREF}}=2.5\text{K} \)

(Note: This \( C_{\text{OX}} \) is somewhat larger than that in the 0.5u ON process)

\( t_{\text{PROP}} = t_{\text{REF}} \cdot ? \)
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Minimum-sized gates

Observe that a minimum-sized gate is simply a gate with asymmetric overdrive
## Propagation Delay in Multiple-Levels of Logic with Stage Loading

### Minimum-sized gates

<table>
<thead>
<tr>
<th>C(<em>{\text{IN}}/C</em>{\text{REF}})</th>
<th>Equal Rise/Fall</th>
<th>Equal Rise/Fall (with OD)</th>
<th>Minimum Sized</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inverter</td>
<td>1</td>
<td>OD</td>
<td>1/2</td>
</tr>
<tr>
<td>(\frac{3k+1}{4})</td>
<td>(\frac{3k+1}{4}) (\cdot) OD</td>
<td>(1/2)</td>
<td></td>
</tr>
<tr>
<td>(\frac{3+k}{4})</td>
<td>(\frac{3+k}{4}) (\cdot) OD</td>
<td>(1/2)</td>
<td></td>
</tr>
</tbody>
</table>

### Overdrive

<table>
<thead>
<tr>
<th>Inverter</th>
<th>HL</th>
<th>LH</th>
<th>OD</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>OD</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>NOR</th>
<th>HL</th>
<th>LH</th>
<th>OD</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>OD</td>
<td>1/3</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>NAND</th>
<th>HL</th>
<th>LH</th>
<th>OD</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>OD</td>
<td>1/(3k)</td>
<td></td>
</tr>
</tbody>
</table>

### All gate FI=1/2

- **NOR:** \(OD_{\text{LH}}=1/3k; OD_{\text{HL}}=1\)
- **NAND:** \(OD_{\text{LH}}=1/3; OD_{\text{HL}}=1/k\)

\(k:\) # inputs

<table>
<thead>
<tr>
<th>(t_{\text{PROP}}/t_{\text{REF}})</th>
<th>(\sum_{i=1}^{n} F_{i})</th>
<th>(\frac{1}{2} \sum_{i=1}^{n} F_{i} \left( \frac{1}{OD_{\text{HLi}}} + \frac{1}{OD_{\text{LHi}}} \right))</th>
</tr>
</thead>
<tbody>
<tr>
<td>(\sum_{i=1}^{n} F_{i})</td>
<td>(\sum_{i=1}^{n} \frac{F_{i}}{OD_{i}})</td>
<td></td>
</tr>
</tbody>
</table>
Minimum-sized gates

All gate \( F^I = \frac{1}{2} \)

\( F^I_C = \frac{C}{C_{\text{REF}}} \)

NOR: \( OD_{LH} = \frac{1}{3}k; \ OD_{HL} = 1 \)

NAND: \( OD_{LH} = \frac{1}{3}; \ OD_{HL} = \frac{1}{k} \)

\( k: \ #\text{inputs} \)

\[ \begin{align*}
  &F_2 = \frac{13}{2} \\
  &F_3 = 1 \\
  &F_4 = 1 \\
  &F_5 = \frac{1}{2} \\
  &F_6 = 12.5
\end{align*} \]

\[ t_{\text{PROP}} = t_{\text{REF}} \cdot \left( \frac{1}{2} \sum_{i=1}^{5} F_i^{I+1} \left( \frac{1}{OD_{HLi}} + \frac{1}{OD_{LHi}} \right) \right) \]

\[ t_{\text{PROP}} = t_{\text{REF}} \cdot \frac{1}{2} \left( \frac{13}{2} \left( \frac{3 + 3}{} + 1 \left( \frac{12 + 1}{6 + 10} + \frac{1}{2} \left( \frac{9 + 1}{2 + 3} \right) + 12.5 \cdot 2 + 3 \right) \right) \]

\[ t_{\text{PROP}} = 63.25 \cdot t_{\text{REF}} \]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Asymmetric-sized gates

\[
F_{NOR} = \frac{3kOD_{LH} + 1 \cdot OD_{HL}}{4}
\]

\[
F_{NAND} = \frac{3OD_{LH} + kOD_{HL}}{4}
\]

\[
t_{PROP} = t_{REF} \cdot \?
\]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Asymmetric-sized gates

<table>
<thead>
<tr>
<th>CIN/CREF</th>
<th>Equal Rise/Fall</th>
<th>Equal Rise/Fall (with OD)</th>
<th>Minimum Sized</th>
<th>Asymmetric OD (OD_{HL}, OD_{LH})</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inverter</td>
<td>1</td>
<td>OD</td>
<td>1/2</td>
<td>OD_{HL} + 3 \cdot OD_{LH}</td>
</tr>
<tr>
<td>NOR</td>
<td>3k+1/4</td>
<td>3k+1 \cdot OD</td>
<td>1/2</td>
<td>OD_{HL} + 3k \cdot OD_{LH}</td>
</tr>
<tr>
<td>NAND</td>
<td>3+k/4</td>
<td>3+k \cdot OD</td>
<td>1/2</td>
<td>k \cdot OD_{HL} + 3 \cdot OD_{LH}</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Overdrive</th>
<th>Inverter</th>
<th>Equal Rise/Fall</th>
<th>Minimum Sized</th>
<th>Asymmetric OD</th>
</tr>
</thead>
<tbody>
<tr>
<td>HL</td>
<td>1</td>
<td>OD</td>
<td>1</td>
<td>OD_{HL}</td>
</tr>
<tr>
<td>LH</td>
<td>1</td>
<td>OD</td>
<td>1/3</td>
<td>OD_{LH}</td>
</tr>
<tr>
<td>NOR</td>
<td>1</td>
<td>OD</td>
<td>1</td>
<td>OD_{HL}</td>
</tr>
<tr>
<td>HL</td>
<td>1</td>
<td>OD</td>
<td>1/(3k)</td>
<td>OD_{LH}</td>
</tr>
<tr>
<td>LH</td>
<td>1</td>
<td>OD</td>
<td>1/k</td>
<td>OD_{HL}</td>
</tr>
</tbody>
</table>

| t_{PROP}/t_{REF} | \sum_{i=1}^{n} F_{i(i+1)} | \frac{1}{2} \sum_{i=1}^{n} F_{i(i+1)} \left( \frac{1}{OD_{HLi}} + \frac{1}{OD_{LHi}} \right) | \frac{1}{2} \sum_{i=1}^{n} F_{i(i+1)} \left( \frac{1}{OD_{HLi}} + \frac{1}{OD_{LHi}} \right) | \frac{1}{2} \sum_{i=1}^{n} F_{i(i+1)} \left( \frac{1}{OD_{HLi}} + \frac{1}{OD_{LHi}} \right) |

\[ t_{PROP} = t_{REF} \cdot \left( \frac{1}{2} \sum_{i=1}^{5} F_{i(i+1)} \left( \frac{1}{OD_{HLi}} + \frac{1}{OD_{LHi}} \right) \right) \]
Asymmetric-sized gates

NOR: \( \frac{\text{OD}_{HL} + 3k \cdot \text{OD}_{LH}}{4} \)

NAND: \( k \cdot \text{OD}_{HL} + 3 \cdot \text{OD}_{LH} \)

\[ t_{\text{PROP}} = t_{\text{REF}} \cdot \left( \frac{1}{2} \sum_{i=1}^{5} F_{i} \left( \frac{1}{\text{OD}_{HLi}} + \frac{1}{\text{OD}_{LHi}} \right) \right) \]

\[ t_{\text{PROP}} = t_{\text{REF}} \cdot \frac{1}{2} \left( \frac{63}{8} \left( \frac{1}{2} + \frac{1}{2} \right) + \frac{29}{4} \left( 2 + 4 \right) + \frac{77}{16} (1+1) + \frac{7}{2} \left( 4 + \frac{1}{4} \right) + 12.5 \left( \frac{1}{2} + \frac{1}{4} \right) \right) \]

\[ t_{\text{PROP}} = 44.6 \cdot t_{\text{REF}} \]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

*Mixture of Minimum-sized gates, equal rise/fall gates and OD*

\[ t_{\text{PROP}} = t_{\text{REF}} \cdot ? \]
Driving Notation

- Equal rise/fall (no overdrive)
- Equal rise/fall with overdrive
- Minimum Sized
- Asymmetric Overdrive
Propagation Delay in Multiple-Levels of Logic with Stage Loading

*Mixture of Minimum-sized gates, equal rise/fall gates and OD*

\[
t_{\text{PROP}} = t_{\text{REF}} \cdot \left( \frac{1}{2} \sum_{i=1}^{5} F_{l(i+1)} \left( \frac{1}{OD_{HLi}} + \frac{1}{OD_{LHi}} \right) \right)
\]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

*Mixture of Minimum-sized gates, equal rise/fall gates and OD*

\[
t_{\text{PROP}} = t_{\text{REF}} \cdot \left( \frac{1}{2} \sum_{i=1}^{5} F_{i(i+1)} \left( \frac{1}{\text{OD}_{\text{HLi}}} + \frac{1}{\text{OD}_{\text{LHi}}} \right) \right)
\]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

- Equal rise/fall (no overdrive)

- Equal rise/fall with overdrive

- Minimum Sized

- Asymmetric overdrive

- Combination of equal rise/fall, minimum size and overdrive

\[ t_{\text{PROP}} = t_{\text{REF}} \sum_{i=1}^{n} \frac{F_{i} (i+1)}{OD_{i}} \]
Driving Large Capacitive Loads

Example

Assume driving by a reference inverter

Assume \( C_L = 1000C_{REF} \)

\[ t_{PROP} = ? \]

In 0.5u proc \( t_{REF} = 20\text{ps}, \]
\( C_{REF} = 4fF, R_{PDREF} = 2.5K \)
Driving Large Capacitive Loads

Example

Assume driving by a reference inverter

Assume $C_L = 1000C_{REF}$

$t_{PROP} = 1000t_{REF}$

t$_{PROP}$ is too long!

In 0.5µ proc $t_{REF}=20\text{ps}$,
$C_{REF}=4\text{fF}$, $R_{PDREF}=2.5\text{K}$
Driving Large Capacitive Loads

Example

Assume first stage is a reference inverter

Assume $C_L = 1000C_{REF}$

$\sum_{i=1}^{2} \left( \frac{F_{I(i+1)}}{OD_i} \right) = t_{PROP} = t_{REF} (1000 + 1)$

$t_{PROP} = t_{REF} (1001)$
Driving Large Capacitive Loads

Example

Assume first stage is a reference inverter

Assume $C_L = 1000C_{REF}$

$$t_{PROP} = t_{REF} \left( \sum_{i=1}^{3} \frac{F_{I(i+1)}}{O_{D_i}} \right)$$

$$t_{PROP} = t_{REF} \left( \frac{1}{10} + \frac{1}{100} + \frac{1}{1000} \right) = t_{REF} (10 + 10 + 10)$$

$$t_{PROP} = 30t_{REF}$$

Dramatic reduction is propagation delay (over a factor of 30!)

What is the fastest way to drive a large capacitive load?
Optimal Driving of Capacitive Loads

Assume first stage is a reference inverter

Need to determine the number of stages, n, and the OD factors for each stage to minimize $t_{PROP}$.

$$t_{PROP} = t_{REF} \sum_{i=1}^{n} \frac{F_i (i+1)}{OD_i}$$

where $\theta_0 = 1$, $\theta_n = C_L/C_{REF}$

This becomes an n-parameter optimization (minimization) problem!

Unknown parameters: $\{\theta_1, \theta_2, \ldots \theta_{n-1}, n\}$

An n-parameter nonlinear optimization problem is generally difficult !!!!
Optimal Driving of Capacitive Loads

Assume first stage is a reference inverter

Order reduction strategy: Assume overdrive of stages increases by the same factor clear until the load

This becomes a 2-parameter optimization (minimization) problem!

Unknown parameters: \( \{ \theta, n \} \)

One constraint: \( \theta^n C_{REF} = C_L \)

One degree of freedom
Optimal Driving of Capacitive Loads

\[ t_{PROP} = t_{REF} \sum_{i=1}^{n} \frac{\theta_i}{\theta_{i-1}} \]

Unknown parameters: \( \{\theta, n\} \)

Thus obtain an expression for \( t_{PROP} \) in terms of only \( \theta \)

\[ t_{PROP} = t_{REF} \frac{\theta}{\ln(\theta)} \left[ \ln \left( \frac{C_L}{C_{REF}} \right) \right] \]
Optimal Driving of Capacitive Loads

\[ t_{\text{PROP}} = t_{\text{REF}} \frac{\theta}{\ln(\theta)} \left[ \ln \frac{C_L}{C_{\text{REF}}} \right] \]

It suffices to minimize the function

\[ f(\theta) = \frac{\theta}{\ln(\theta)} \]

\[ \frac{\mathrm{d}f}{\mathrm{d}\theta} = -\theta \cdot \left( \frac{1}{\theta} \right) \left( \ln(\theta) \right)^2 = 0 \]

\[ \ln(\theta) - 1 = 0 \quad \rightarrow \quad \theta = e \]

\[ n = \frac{1}{\ln(\theta)} \ln \left( \frac{C_L}{C_{\text{REF}}} \right) \quad \rightarrow \quad n = \ln \left( \frac{C_L}{C_{\text{REF}}} \right) \]
Optimal Driving of Capacitive Loads

\[ \theta_{\text{OPT}} = e \]

\[ n_{\text{OPT}} = \ln \left( \frac{C_L}{C_{\text{REF}}} \right) \]

\[ t_{\text{PROP}} = t_{\text{REF}} \frac{\theta}{\ln(\theta)} \left[ \ln \frac{C_L}{C_{\text{REF}}} \right] \]

\[ t_{\text{PROP}} = t_{\text{REF}} e^{\ln \frac{C_L}{C_{\text{REF}}}} = n \theta t_{\text{REF}} \]
Optimal Driving of Capacitive Loads

\[ f = \frac{\theta}{\ln(\theta)} \]

- minimum at \( \theta = e \) but shallow inflection point for \( 2 < \theta < 3 \)
- practically pick \( \theta = 2, \theta = 2.5, \) or \( \theta = 3 \)
- since optimization may provide non-integer for \( n \), must pick close integer
Optimal Driving of Capacitive Loads

- Often termed a pad driver
- Often used to drive large internal busses as well
- Generally included in standard cells or in cell library
- Device sizes can become very large
- Odd number of stages will cause signal inversion but usually not a problem
Optimal Driving of Capacitive Loads

Example: Design a pad driver for driving a load capacitance of 10pF, determine $t_{\text{PROP}}$ for the pad driver, and compare this with the propagation delay for driving the pad with a minimum-sized reference inverter.

In 0.5μm proc, $t_{\text{REF}}=20$ps, $C_{\text{REF}}=4fF, R_{P\text{DREF}}=2.5K$

$$n_{\text{OPT}} = \ln \left( \frac{C_L}{C_{\text{REF}}} \right) = \ln \left( \frac{10\text{pF}}{4\text{fF}} \right) = 7.8$$

Select $n=8$, $\theta=2.5$

$$W_{nk} = 2.5^{k-1}, \quad W_{pk} = 3 \cdot 2.5^{k-1}$$
Optimal Driving of Capacitive Loads

Example: Design a pad driver for driving a load capacitance of 10pF, determine $t_{\text{PROP}}$ for the pad driver, and compare this with the propagation delay for driving the pad with a minimum-sized reference inverter.

In 0.5µm process, $t_{\text{REF}}=20\text{ps}$, $C_{\text{REF}}=4\text{fF}, R_{\text{PDREF}}=2.5\text{K}$

$W_{nk}=2.5^{k-1}$, $W_{pk}=3\cdot2.5^{k-1}$

$L_n=L_p=L_{\text{MIN}}$

<table>
<thead>
<tr>
<th>$k$</th>
<th>n-channel</th>
<th>p-channel</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1 WMIN</td>
<td>3 WMIN</td>
</tr>
<tr>
<td>2</td>
<td>2.5 WMIN</td>
<td>7.5 WMIN</td>
</tr>
<tr>
<td>3</td>
<td>6.25 WMIN</td>
<td>18.75 WMIN</td>
</tr>
<tr>
<td>4</td>
<td>15.6 WMIN</td>
<td>46.9 WMIN</td>
</tr>
<tr>
<td>5</td>
<td>39.1 WMIN</td>
<td>117.2 WMIN</td>
</tr>
<tr>
<td>6</td>
<td>97.7 WMIN</td>
<td>293.0 WMIN</td>
</tr>
<tr>
<td>7</td>
<td>244.1 WMIN</td>
<td>732.4 WMIN</td>
</tr>
<tr>
<td>8</td>
<td>610.4 WMIN</td>
<td>1831.1 WMIN</td>
</tr>
</tbody>
</table>

Note devices in last stage are very large!
Example: Design a pad driver for driving a load capacitance of 10pF, determine $t_{\text{PROP}}$ for the pad driver, and compare this with the propagation delay for driving the pad with a minimum-sized reference inverter.

In 0.5μm process $t_{\text{REF}}=20\text{ps}$, $C_{\text{REF}}=4\text{fF}, R_{\text{PDREF}}=2.5\text{K}$

$W_{nk}=2.5^{k-1}$, $W_{pk}=3\cdot2.5^{k-1}$

$t_{\text{PROP}} \approx n\theta t_{\text{REF}} = 8\cdot2.5\cdot t_{\text{REF}} = 20t_{\text{REF}}$

More accurately:

$t_{\text{PROP}} = t_{\text{REF}} \left( \sum_{k=1}^{n} \frac{1}{\theta^k} \frac{C_L}{C_{\text{REF}}} \right) = t_{\text{REF}} \left( 17.5 + \frac{1}{610} \cdot \frac{2500}{2500} \right) = 21.6t_{\text{REF}}$
Example: Design a pad driver for driving a load capacitance of 10pF, determine $t_{\text{PROP}}$ for the pad driver, and compare this with the propagation delay for driving the pad with a minimum-sized reference inverter.

In 0.5µm process, $t_{\text{REF}}=20\text{ps}$, $C_{\text{REF}}=4\text{fF}$, $R_{\text{PDREF}}=2.5\text{K}\Omega$

- $W_{nk}=2.5^{k-1}$
- $W_{pk}=3\cdot2.5^{k-1}$

If driven directly with the minimum-sized reference inverter

$$t_{\text{PROP}}=t_{\text{REF}} \frac{C_L}{C_{\text{REF}}}=2500t_{\text{REF}}$$

Note an improvement in speed by a factor of

$$r = \frac{2500}{20} = 125$$
Optimal Driving of Capacitive Loads

Example:  Design a pad driver for driving a load capacitance of 10pF, determine $t_{PROP}$ for the pad driver, and compare this with the propagation delay for driving the pad with a minimum-sized reference inverter.

In 0.5u proc $t_{REF}=20ps$, $C_{REF}=4fF$, $R_{PDREF}=2.5k$

$W_{nk}=2.5^{k-1}$,  $W_{pk}=3\cdot2.5^{k-1}$

$\begin{array}{|c|c|c|}
\hline
k & n-channel & p-channel \\
\hline
1 & 1 \cdot \text{MIN} & 3 \cdot \text{MIN} \\
2 & 2.5 \cdot \text{MIN} & 7.5 \cdot \text{MIN} \\
3 & 6.25 \cdot \text{MIN} & 18.75 \cdot \text{MIN} \\
4 & 15.6 \cdot \text{MIN} & 46.9 \cdot \text{MIN} \\
5 & 39.1 \cdot \text{MIN} & 117.2 \cdot \text{MIN} \\
6 & 97.7 \cdot \text{MIN} & 293.0 \cdot \text{MIN} \\
7 & 244.1 \cdot \text{MIN} & 732.4 \cdot \text{MIN} \\
8 & 610.4 \cdot \text{MIN} & 1831.1 \cdot \text{MIN} \\
\hline
\end{array}$

Note devices in last stage are very large!
Consider a 7-stage pad driver and assume $\theta = 3$.
Area of Last Stage Larger than that of all previous stages combined!
End of Lecture 41