EE 330
Lecture 42
Digital Circuits

Power Dissipation in Logic Circuits
Other Logic Styles
Propagation Delay in “Logic Effort” approach

Propagation delay for equal rise/fall gates was derived to be

\[ t_{PROP} = t_{REF} \sum_{k=1}^{3} \frac{F_{I(k+1)}}{OD_k} \]

Delay calculations with “logical effort” approach

Author’s definition:

\[ t_{PROP} = \sum_{k=1}^{n} f_k \]

(will show small error in this equation)

where \( f_k \) is the “effort delay” of stage \( k \)

\[ f_k = g_k h_k \]

\( g_k = \) logical effort

\( h_k = \) electrical effort
**Propagation Delay in “Logic Effort” approach**

\[ t_{\text{PROP}} = \sum_{k=1}^{n} f_k = \sum_{k=1}^{n} g_k h_k = \sum_{k=1}^{n} \frac{F_{\text{OD}}^{(k+1)}}{OD_k} \]

- Note with the exception of the \( t_{\text{REF}} \) that was omitted in the text, this expression is identical to what we have derived previously.

- Probably more tedious to use the “Logical Effort” approach.

- Extensions to asymmetric overdrive factors may not be trivial.

- Extensions to include parasitics may be tedious as well.

- Logical Effort is widely used throughout the industry.
Elmore Delay Calculations

- Interconnects have a distributed resistance and a distributed capacitance
  - Often modeled as resistance/unit length and capacitance per unit length

- These delay the propagation of the signal

- Effectively a transmission line
  - Analysis is really complicated

- Can have much more complicated geometries
Elmore Delay Calculations

Elmore delay:

\[ t_{PD} = \sum_{i=1}^{n} \left( \sum_{j=1}^{i} C_i R_j \right) \]

- Numbering is critical (resistors and capacitors numbered from input to output)
- As stated, only applies to this specific structure
Review from last time

Elmore Delay Calculations

Extensions:

Lumped Network Model:
Power Dissipation in Logic Circuits

Assume current periodic with period $T_{CL}$

$$P_{AVG,T} = \frac{1}{T_{CL}} \int_{t_1}^{t_1 + T_{CL}} V_{DD} I_{DD}(t) dt$$
Power Dissipation in Logic Circuits

Types of Power Dissipation

- Static
- Pipe
- Dynamic
- Leakage
  - Gate
  - Diffusion
  - Drain
Static Power Dissipation

If Boolean output averages H and L 50% of the time

\[
P_{\text{STAT, AVG}} = \frac{P_H + P_L}{2}
\]

\[
P_{\text{STAT, AVG}} = \frac{V_{\text{DD}}(I_{\text{DDH}} + I_{\text{DDL}})}{2}
\]

Generally decreases with \( V_{\text{DD}} \)

\( I_{\text{DDH}} = I_{\text{DDL}} = 0 \) for static CMOS gates so \( P_{\text{STAT}} = 0 \)
Pipe Power Dissipation

Due to conduction of both PUN and PDN during transitions

- Can be made small if transitions are fast
- Usually negligible in Static CMOS circuits
Dynamic Power Dissipation

Due to charging and discharging $C_L$ on logic transitions

$C_L$ dissipates no power but PUN and PDN dissipate power during charge and discharge of $C_L$

$C_L$ includes all gate input capacitances of loads and interconnect capacitances
Dynamic Power Dissipation

Energy supplied by $V_{DD}$ when $C_L$ charges:

$$E = \int_{t_1}^{\infty} V_{DD} I_{DD}(t) dt$$

$$I_{DD} = C_L \frac{dV_C}{dt}$$

$$E = \int_{t_1}^{\infty} V_{DD} C_L \frac{dV_C}{dt} dt$$

$$V_{DD}$$

$$E = \int_{V_C=0}^{V_{DD}} V_{DD} C_L dV_C = V_{DD} C_L \int_{V_C=0}^{V_{DD}} dV_C = V_{DD} C_L V_C \bigg|_{V_C=0}^{V_{DD}} = V_{DD}^2 C_L$$

Energy stored in $C_L$ after $C_L$ is charged to $V_{DD}$:

$$E = \frac{1}{2} C_L V_{DD}^2$$
Dynamic Power Dissipation

Energy supplied by $V_{DD}$ when $C_L$ charges

$$E_{DIS} = \frac{1}{2} C_L V_{DD}^2$$

Energy stored on $C_L$ after L-H transition

$$E_{STORE} = \frac{1}{2} C_L V_{DD}^2$$

Thus, energy from $V_{DD}$ for one L-H output transition is

$$E = C_L V_{DD}^2$$

When the output transitions from H to L, energy stored on $C_L$ is dissipated in PDN

If $f$ is the average transition rate of the output, determine $P_{AVG}$
Dynamic Power Dissipation

Energy from $V_{DD}$ for one L-H output transition is

$$E = C_L V_{DD}^2$$

If $f$ is the average transition rate of the output, determine $P_{AVG}$

$$P_{AVG} = \frac{E}{T} = Ef$$

$$P_{DYN} = fC_L V_{DD}^2$$

If a gate has a transition duty cycle of 50% with a clock frequency of $f_{CL}$

$$P_{DYN} = \frac{f_{CL}}{2} C_L V_{DD}^2$$

Note dependent on the square of $V_{DD}$! .... Want to make $V_{DD}$ small !!!

Major source of power dissipation in many static CMOS circuits for $L_{min}>0.1\mu$
Leakage Power Dissipation

- Gate
  with very thin gate oxides, some gate leakage current flows
  major concern in 60nm and smaller processes
  actually a type of static power dissipation

- Diffusion
  Leakage across a reverse-biased pn junction
  Dependent upon total diffusion area
  May actually be dominant power loss on longer-channel devices
  Actually a type of static power dissipation

- Drain
  channel current due to small $V_{GS} - V_T$
  of significant concern only with low $V_{DD}$ processes
  actually a type of static power dissipation
Example: Determine the dynamic power dissipation in the last stage of a 6-stage CMOS pad driver if used to drive a 10pF capacitive load if clocked at 500MHz. Assume pad driver with OD of $\theta = 2.5$ and $V_{DD} = 3.5V$.

Solution: (assume output changes with 50% of clock transitions)

$$P_{DYN} = \frac{f_{CL} C_L V_{DD}^2}{2} = 5E8 \cdot 10pF \cdot 3.5^2 = 61mW$$

Note this solution is independent of the OD and the process.
Example: Will the CMOS pad driver actually be able to drive the 10pF load at 500MHz in the previous example in the 0.5u process?

Solution:

\[
t_{CLK} = \frac{1}{500\text{MHz}} = 2\text{nsec}
\]

\[
t_{PROP} = n\theta \cdot t_{REF} = 6 \cdot 2.5 \cdot 20\text{psec} = 0.3\text{nsec}
\]

since \( t_{CLK} > t_{PROP} \), this pad driver can drive the 10pF load at 500MHz
Example: Determine the dynamic power dissipation in the next to the last stage of a 6-stage CMOS pad driver if used to drive a 10pF capacitive load if clocked at 500MHz. Assume pad driver with OD of $\theta=2.5$ and $V_{DD}=3.5V$.

Solution:

$C_{IN} = \theta^5 C_{REF} = 2.5^5 \cdot 4fF = 390fF$

$P_{DYN} = f_{CL} C_L V_{DD}^2 = 5E8 \cdot 390fF \cdot 3.5^2 = 2.4mW$
Example:  Is the 6-stage CMOS pad driver adequate to drive the 10pF capacitive load as fast as possible?  Assume pad driver with OD of $\theta=2.5$ and $V_{DD}=3.5V$

Solution:

$$n_{OPT} = \ln\left(\frac{C_L}{C_{REF}}\right) = \ln\left(\frac{10pF}{4fF}\right) = 7.8$$

No – an 8-stage pad driver would drive the load much faster (but is not needed if clocked at only 500MHz)
Example: Determine the power that would be required in the last stage of a CMOS pad driver to drive a 32-bit data bus off-chip if the capacitive load on each line is 2pF. Assume the clock speed is 500MHz and that each bit has an average 50% toggle rate. Assume $V_{DD}=3.5V$.

Solution:

$$P_{DYN} = 32 \cdot \frac{f_{CL}}{2} C_L V_{DD}^2 = 32 \cdot \frac{5 \times 10^8}{2} \cdot 2pF \cdot 3.5^2 = 196mW$$

Note: A very large amount of power is required to take a large bus off-chip if bus has a high rate of activity.
End of Lecture 42