Device Sizing

Propagation Delay in Multiple Levels of Logic

Optimally Driving Large Capacitive Loads
How does the propagation delay compare for a minimum-sized strategy to that of an equal rise/fall sizing strategy?

Minimum Sized
\[ W_2 = W_1 = W_{\text{MIN}} \]
\[ t_{\text{PROP}} = t_{\text{REF}} \]

Reference Inverter
\[ W_2 = (\mu_n / \mu_p) W_1, \quad W_1 = W_{\text{MIN}} \]
\[ t_{\text{PROP}} = t_{\text{REF}} \]

They are the same!

Even though the \( t_{\text{LH}} \) rise time has been reduced with the equal rise/fall sizing strategy, this was done at the expense of an increase in the total load capacitance that resulted in no net change in propagation delay!
Review from last lecture

Device Sizing

Will consider now the multiple-input gates

Will consider both minimum sizing and equal **worst-case** rise/fall

Will assume $C_L$ (not shown)=$C_{REF}$

Note: worst-case has been added since fall time in NOR gates or rise time in NAND gates depends upon how many transistors are conducting
Sizing of Multiple-Input Gates

Analysis strategy: Express delays in terms of those of reference inverter

Reference Inverter

\[ C_{\text{REF}} = C_{\text{IN}} = 4C_{\text{OX}} W_{\text{MIN}} L_{\text{MIN}} \]

\[ R_{\text{PDREF}} = \frac{L_{\text{MIN}}}{\mu_n C_{\text{OX}} W_{\text{MIN}} (V_{\text{DD}} - V_{Tn})} = \frac{L_{\text{MIN}}}{\mu_n C_{\text{OX}} W_{\text{MIN}} (0.8V_{\text{DD}})} \]

\[ t_{\text{HLREF}} = t_{\text{LHREF}} = R_{\text{PDREF}} C_{\text{REF}} \]

\[ t_{\text{REF}} = t_{\text{HLREF}} + t_{\text{LHREF}} = 2R_{\text{PDREF}} C_{\text{REF}} \]

\[ L_{n} = L_{p} = L_{\text{MIN}} \]

Assume \( \mu_n / \mu_p = 3 \)

\( W_n = W_{\text{MIN}}, \quad W_p = 3W_{\text{MIN}} \)

In 0.5u proc \( t_{\text{REF}} = 20\text{ps}, \quad C_{\text{REF}} = 4\text{fF}, R_{\text{PDREF}} = 2.5K \)
Device Sizing

Equal Worse-Case Rise/Fall Device Sizing Strategy \((t_{prop} = t_{REF})\)
--- (same as \(V_{TRIP} = V_{DD}/2\) in typical process considered in example)

Assume \(\mu_n / \mu_p = 3\)
\(L_n = L_p = L_{MIN}\)

\(V_{IN} \rightarrow V_{OUT} \quad V_{DD} \quad M_1 \quad M_2 \quad V_{OUT}\)

INV

\(W_n = W_{MIN}, \quad W_p = 3W_{MIN}\)
\(C_{IN} = C_{REF}\)
\(R_{PU} = R_{PD} = R_{PDREF}\)

k-input NOR

\(W_n = W_{MIN}, \quad W_p = 3kW_{MIN}\)
\(C_{IN} = \left(\frac{3k+1}{4}\right)C_{REF}\)
\(R_{PU} = R_{PD} = R_{PDREF}\)

\(IN_{REF} \quad V_{DD} \quad M_{21} \quad M_{22} \quad \ldots \quad M_{2k} \quad V_{OUT}\)

\(V_{OUT} \rightarrow V_{DD} \quad A_k \quad M_{2k} \quad V_{OUT} \quad A_1 \quad M_{1k}\)

\(IN_{REF} \quad V_{DD} \quad M_{1k} \quad V_{OUT} \quad A_1 \quad M_{1k}\)

\(k\)-input NOR

\(W_n = kW_{MIN}, \quad W_p = 3W_{MIN}\)
\(C_{IN} = \left(\frac{3+k}{4}\right)C_{REF}\)
\(R_{PU} = R_{PD} = R_{PDREF}\)
Device Sizing

Multiple Input Gates:

2-input NOR  2-input NAND  k-input NOR  k-input NAND

Equal Worst Case Rise/Fall (and equal to that of ref inverter when driving $C_{REF}$)

$W_n=$?

$W_p=$?

Fastest response ($t_{HL}$ or $t_{HL}$) = ?

Worst case response ($t_{PROP}$, usually of most interest)?

Input capacitance = ?

Minimum Sized (assume driving a load of $C_{REF}$)

$W_n=W_{min}$

$W_p=W_{min}$

Fastest response ($t_{HL}$ or $t_{HL}$) = ?

Slowest response ($t_{HL}$ or $t_{HL}$) = ?

Worst case response ($t_{PROP}$, usually of most interest)?

Input capacitance = ?
Device Sizing

Minimum Sized  (assume driving a load of  $C_{REF}$)

\[ W_n = W_{min} \]
\[ W_p = W_{min} \]

Input capacitance = ?

Fastest response ($t_{HL}$ or $t_{HL}$) = ?

Slowest response ($t_{HL}$ or $t_{HL}$) = ?

Worst case response ($t_{PROP}$, usually of most interest)?
Device Sizing – minimum size driving $C_{REF}$

k-input NOR

$t_{PROP} = ?$

$t_{PROP} = 0.5t_{REF} + \frac{3k}{2}t_{REF}$

$t_{PROP} = \left( \frac{3k+1}{2} \right)t_{REF}$

$F_I = \frac{C_{REF}}{2}$

$R_{PU} = R_{PD} = R_{PDREF}$

$R_{PD} = R_{PDREF}$

$R_{PU} = 3R_{PDREF}$

$R_{PD} = 3R_{PDREF}$

$R_{PU} = 3R_{PDREF}$
Device Sizing Summary

$C_{IN}$ for $N_{AND}$ gates is considerably smaller than for NOR gates for equal worst-case rise and fall times.

$C_{IN}$ for minimum-sized structures is independent of number of inputs and much smaller than $C_{IN}$ for the equal rise/fall time case.

$R_{PU}$ gets very large for minimum-sized NOR gate.
Digital Circuit Design

- Hierarchical Design
- Basic Logic Gates
- Properties of Logic Families
- Characterization of CMOS Inverter
- Static CMOS Logic Gates
  - Ratio Logic
- Propagation Delay
  - Simple analytical models
  - Elmore Delay
- Sizing of Gates

- Propagation Delay with Multiple Levels of Logic
- Optimal driving of Large Capacitive Loads
- Power Dissipation in Logic Circuits
- Other Logic Styles
- Array Logic
- Ring Oscillators
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Assume all gates sized for equal worst-case rise/fall times

For n levels of logic between A and F

\[ t_{\text{PROP}} = \sum_{k=1}^{n} t_{\text{PROP}}(k) \]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Analysis strategy: Express delays in terms of those of reference inverter

Reference Inverter

\[ C_{REF} = C_{IN} = 4C_{OX} W_{MIN} L_{MIN} \]

\[ R_{PDREF} = \frac{L_{MIN}}{\mu_n C_{OX} W_{MIN} (V_{DD} - V_{Tn})} \quad V_{Tn} = 2V_{DD} \]

\[ t_{REF} = t_{HLREF} + t_{LHREF} = 2R_{PDREF} C_{REF} \]

Assume \( \mu_n/\mu_p = 3 \)

\( W_n = W_{MIN}, \quad W_p = 3W_{MIN} \)

In 0.5u proc \( t_{REF} = 20ps, \quad C_{REF} = 4fF, R_{PDREF} = 2.5k \)

\( V_{IN} \)

\( V_{OUT} \)}
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Assume all gates sized for equal worst-case rise/fall times

What loading will a gate see?

- Input capacitance to other gates
- Any load capacitors
- Parasitic interconnect capacitances
Propagation Delay with Stage Loading

\[ t_{\text{REF}} = 2R_{\text{PDref}} C_{\text{REF}} \]

\[ C_{\text{REF}} = C_{\text{IN}} = 4C_{\text{OX}} W_{\text{MIN}} L_{\text{MIN}} \]

Fl of a capacitor

\[ F_{\text{Ic}} = \frac{C}{C_{\text{REF}}} \]

Fl of a gate (input k)

\[ F_{\text{Ig}} = \frac{C_{\text{INK}}}{C_{\text{REF}}} \]

Fl of an interconnect

\[ F_{\text{Ii}} = \frac{C_{\text{INI}}}{C_{\text{REF}}} \]

Overall Fl

\[ F_{\text{I}} = \sum_{\text{Gates}} C_{\text{INGi}} + \sum_{\text{Capacitances}} C_{\text{INCi}} + \sum_{\text{Interconnects}} C_{\text{INIi}} \]

Fl can be expressed either in units of capacitance or normalized to \( C_{\text{REF}} \)

Most commonly Fl is normalized but must determine from context
Propagation Delay in Multiple-Levels of Logic with Stage Loading

What loading will a gate see?

Assume all gates sized for equal worst-case rise/fall times

Derivation:

\[ F_{I_2} = \frac{6}{4} C_{REF} \]
\[ F_{I_3} = C_{REF} + \frac{7}{4} C_{REF} \]
\[ F_{I_4} = \frac{7}{4} C_{REF} + \frac{13}{4} C_{REF} \]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Neglect interconnect capacitance, assume load of $10C_{\text{REF}}$ on F output.

Assume all gates sized for equal worst-case rise/fall times.

DERIVATIONS
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Assume all gates sized for equal worst-case rise/fall times

Neglect interconnect capacitance, assume load of $10C_{REF}$ on $F$ output

**DERIVATIONS**

- $F_{I2} = \frac{6}{4}C_{REF}$
- $F_{I3} = C_{REF} + \frac{7}{4}C_{REF}$
- $F_{I4} = \frac{7}{4}C_{REF} + \frac{13}{4}C_{REF}$
- $F_{I5} = 10C_{REF}$

- $t_1 = \frac{6}{4}t_{REF}$
- $t_2 = \left(1 + \frac{7}{4}\right)t_{REF}$
- $t_3 = \left(\frac{7}{4} + \frac{13}{4}\right)t_{REF}$
- $t_4 = 10t_{REF}$
Propagation Delay Through Multiple Stages of Logic with Stage Loading

(assuming gate drives are all same as that of reference inverter)

Identify the gate path from A to F

\[ t_{\text{PROP}k} = t_{\text{REF}} F_{I(k+1)} \]

Propagation delay from A to F:

\[ t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^{n} F_{I(k+1)} \]