EE 330
Lecture 42
Digital Circuits

- Elmore Delay
- Power Dissipation
- Other Logic Styles
- Dynamic Logic Circuits
Digital Circuit Design

- Hierarchical Design
- Basic Logic Gates
- Properties of Logic Families
- Characterization of CMOS Inverter
- Static CMOS Logic Gates
  - Ratio Logic
- Propagation Delay
  - Simple analytical models
    - FI/OD
    - Logical Effort
  - Elmore Delay
- Sizing of Gates
  - done
  - partial

- Propagation Delay with Multiple Levels of Logic
- Optimal driving of Large Capacitive Loads
  - Power Dissipation in Logic Circuits
  - Other Logic Styles
  - Array Logic
  - Ring Oscillators
Propagation Delay in “Logic Effort” approach

(Discussed in Chapter 4 of Text but definitions are not rigorous)

Propagation delay for equal rise/fall gates was derived to be

\[ t_{PROP} = t_{REF} \sum_{k=1}^{n} \frac{F_{l(k+1)}}{OD_k} \]

Delay calculations with “logical effort” approach

Logical effort delay approach:

\[ t_{PROP} = \sum_{k=1}^{n} f_k \]

(t_{REF} scaling factor not explicitly stated)

where \( f_k \) is the “effort delay” of stage \( k \)

\[ f_k = g_k h_k \]

\( g_k = \) logical effort

\( h_k = \) electrical effort
Propagation Delay in “Logic Effort” approach

\[ t_{\text{PROP}} = \sum_{k=1}^{n} f_k \]

\[ f_k = g_k h_k \]

\[ f_k = \text{“effort delay” of stage } k \]

\[ g_k = \text{logical effort} \]

\[ h_k = \text{electrical effort} \]

Logic Effort is the ratio of the input capacitance of a gate to the input capacitance of an inverter that can deliver the same output current.

Electrical Effort is the ratio of the gate load capacitance to the input capacitance of a gate.
Propagation Delay in “Logic Effort” approach

\[ t_{\text{PROP}} = \sum_{k=1}^{n} f_k \quad f_k = g_k h_k \]

Logic Effort \((g)\) is the ratio of the input capacitance of a gate to the input capacitance of an inverter that can deliver the same output current

Electrical Effort \((h)\) is the ratio of the gate load capacitance to the input capacitance of a gate

\[ g_k = \frac{C_{\text{IN}_k}}{C_{\text{REF}} \cdot \text{OD}_k} \quad h_k = \frac{C_{\text{REF}} \cdot F_l k+1}{C_{\text{IN}_k}} \]
Propagation Delay in “Logic Effort” approach

\[ t_{PROP} = \sum_{k=1}^{n} f_k \]

\[ f_k = g_k h_k \]

\[ g_k = \frac{C_{IN_k}}{C_{REF} \cdot OD_k} \]

\[ h_k = \frac{C_{REF} \cdot F_{I(k+1)}}{C_{IN_k}} \]

\[ f_k = \frac{F_{I(k+1)}}{OD_k} \]
Propagation Delay in “Logic Effort” approach

\[ t_{PROP} = \sum_{k=1}^{n} f_k = \sum_{k=1}^{n} g_k h_k = \sum_{k=1}^{n} \frac{F_{l(k+1)}}{OD_k} \]

• Note with the exception of the \( t_{REF} \) scaling factor, this expression is identical to what we have derived previously

• Probably more tedious to use the “Logical Effort” approach

• Extensions to asymmetric overdrive factors may not be trivial

• Extensions to include parasitics may be tedious as well

• Logical Effort is widely used throughout the industry
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Elmore Delay Calculations

- Interconnects have a distributed resistance and a distributed capacitance
  - Often modeled as resistance/unit length and capacitance per unit length

- These delay the propagation of the signal

- Effectively a transmission line
  - analysis is really complicated

- Can have much more complicated geometries
Elmore Delay Calculations

Can have much more complicated geometries
Elmore Delay Calculations

For \( x_1 < x_2 < x_3 \)
Elmore Delay Calculations

A lumped element model of transmission line

Even this lumped model is 4-th order and a closed-form solution is very tedious!

Need a quick (and reasonably good) approximation to the delay of a delay line!
Elmore Delay Calculations

A lumped element model of transmission line

Even this lumped model is 4-th order and a closed-form solution is very tedious!

Need a quick (and reasonably good) approximation to the delay of a delay line!!
Elmore Delay Calculations

It can be shown that this is a reasonably good approximation to the actual delay.

Numbering is critical (resistors and capacitors numbered from input to output).

As stated, only applies to this specific structure.

Elmore delay:

\[
t_{PD} = \sum_{i=1}^{n} \left( C_i \sum_{j=1}^{i} R_j \right)
\]
Elmore Delay Calculations

Elmore delay: 

\[ t_{PD} = \sum_{i=1}^{n} \left( C_i \sum_{j=1}^{i} R_j \right) \]

- Note error in text on Page 161 of first edition of WH

- Not detailed definition on Page 150 of second edition of WH
Elmore delay\cite{1} is a simple approximation to the delay through an RC network in an electronic system. It is often used in applications such as logic synthesis, delay calculation, static timing analysis, placement and routing, since it is simple to compute (especially in tree structured networks, which are the vast majority of signal nets within ICs) and is reasonably accurate. Even where it is not accurate, it is usually faithful, in the sense that reducing the Elmore delay will almost always reduce the true delay, so it is still useful in optimization.

\cite{1} W.C. Elmore. The Transient Analysis of Damped Linear Networks with Particular Regard to Wideband Amplifiers. J. Applied Physics, vol. 19(1), 1948.
Elmore Delay Calculations

Example:

Elmore delay:
\[ t_{PD} = \sum_{i=1}^{4} \left( \sum_{j=1}^{i} R_j \right) \]

Where
\[ t_i = C_i \sum_{j=1}^{i} R_j \quad j = 1, 2, 3, 4 \]

What is really happening?

- Creating 4 first-order circuits
- Delay to \( V_1, V_2, V_3 \) and \( V_4 \) calculated separately by considering capacitors one at a time and assuming others are 0
Elmore Delay Calculations

Extensions:

Lumped Network Model:
Elmore Delay Calculations

Extensions:

1. Create a lumped element model

2. Identify the path from input to output
Elmore Delay Calculations

Extensions:

3. Renumber elements along path from input to output and neglect off-path elements.

4. Use Elmore Delay equation for elements on this RC network

\[ t_{PD} = \sum_{i=1}^{4} \left( C_i \sum_{j=1}^{i} R_j \right) \]
Elmore Delay Calculations

How is a resistive load handled?
**Elmore Delay Calculations**

**Example with resistive load:**

\[ t = \sum_{i=1}^{4} \sum_{j=1}^{4} \left( \frac{C_i}{R_j} \right) \]

**Elmore delay:**

\[ t_{PD} = \sum_{i=1}^{4} t_i \]

where

\[ t_i = C_i \sum_{j=1}^{i} R_j \quad j = 1, 2, 3 \]

\[ t_4 = C_4 \left( \sum_{j=1}^{4} R_j \right) / R_5 \]
Elmore Delay Calculations

With resistive load:

\[
\begin{align*}
V_{\text{IN}} & \quad R_1 \quad C_1 \quad R_2 \quad C_2 \quad R_3 \quad C_3 \quad \cdots \quad R_n \quad C_n \quad V_{\text{OUT}} \\
\end{align*}
\]

Simple Elmore delay:

\[
t_{PD} = \sum_{i=1}^{n-1} \left( C_i \sum_{j=1}^{i} R_j \right) + C_n \left( \sum_{j=1}^{n} R_j \right) / R_L
\]

Actually, \( R_L \) affects all of the delays and a modestly better but modestly more complicated delay model is often used.
Elmore Delay Calculations

How are the number of stages chosen?

• For hand analysis, keep number of stages small (maybe 3 or 4 for simple delay line) if possible)
• If “faithfulness” is important, should keep the number of stages per unit length constant
Elmore Delay Calculations
Elmore Delay Calculations

\[ R = \frac{1}{6} R_i \frac{L}{W} \]

\[ C = \frac{1}{3} C_D \]

\[ t_1 = R(C + C_{REF}) \]

\[ t_2 = 3RC \]

\[ t_3 = 5R \left( C + \frac{1}{2} C_{REF} \right) \]

\[ t_4 = \left[ 6R \parallel R_L \right]^{25} C_{REF} \]

\[ t_5 = t_{REF} \frac{20}{5} \]

\[ t_{PROP} = \sum_{i=1}^{5} t_i \]
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Assume current periodic with period $T_{CL}$

$$P_{AVG,T} = \frac{1}{T_{CL}} \int_{t_1}^{t_1+T_{CL}} V_{DD}I_{DD}(t)dt$$
Power Dissipation in Logic Circuits

Types of Power Dissipation

- Static
- Pipe
- Dynamic
- Leakage
  - Gate
  - Diffusion
  - Drain
Static Power Dissipation

If Boolean output averages H and L 50% of the time

\[ P_{\text{STAT, AVG}} = \frac{P_H + P_L}{2} \]
\[ P_{\text{STAT, AVG}} = \frac{V_{DD}(I_{DDH} + I_{DDL})}{2} \]

- Generally decreases with \( V_{DD} \)
- \( I_{DDH} = I_{DDL} = 0 \) for static CMOS gates so \( P_{\text{STAT}} = 0 \)
- A major source of power dissipation in ratio logic circuits and the major reason CMOS is so widely used
Pipe Power Dissipation

Due to conduction of both PUN and PDN during transitions

- Can be made small if transitions are fast
- Usually negligible in Static CMOS circuits
Due to charging and discharging $C_L$ on logic transitions

$C_L$ dissipates no power but PUN and PDN dissipate power during charge and discharge of $C_L$

$C_L$ includes all gate input capacitances of loads and interconnect capacitances
Dynamic Power Dissipation

Energy supplied by $V_{DD}$ when $C_L$ charges:

$$E = \int_{t_1}^{\infty} V_{DD} I_{DD}(t) \, dt$$

$$I_{DD} = C_L \frac{dV_C}{dt}$$

Energy stored in $C_L$ after $C_L$ is charged to $V_{DD}$:

$$E = \frac{1}{2} C_L V_{DD}^2$$
Dynamic Power Dissipation

Energy supplied by $V_{DD}$ and dissipated in $R_{PU}$ when $C_L$ charges

$$E_{DIS} = \frac{1}{2} C_L V_{DD}^2$$

Energy stored on $C_L$ after L-H transition

$$E_{STORE} = \frac{1}{2} C_L V_{DD}^2$$

Thus, energy from $V_{DD}$ for one L-H: H-L output transition sequence is

$$E = E_{DIS} + E_{STORE} = C_L V_{DD}^2$$

When the output transitions from H to L, energy stored on $C_L$ is dissipated in PDN

If $f$ is the average transition rate of the output, determine $P_{AVG}$
Dynamic Power Dissipation

Energy from $V_{DD}$ for one L-H: H-L output transition sequence is

$$E = C_L V_{DD}^2$$

If $f$ is the average transition rate of the output, determine $P_{AVG}$

$$P_{AVG} = \frac{E}{T} = Ef$$

$$P_{DYN} = fC_L V_{DD}^2$$

If a gate has a transition duty cycle of 50% with a clock frequency of $f_{CL}$

$$P_{DYN} = \frac{f_{CL}}{2} C_L V_{DD}^2$$

Note dependent on the square of $V_{DD}$! .... Want to make VDD small!!!

Major source of power dissipation in many static CMOS circuits for $L_{min} > 0.1\mu m$
Dynamic Power Dissipation

Energy dissipated with clock signal itself

\[ P_{\text{DYN}} = f C_L V_{\text{DD}}^2 \]

The clock transitions on every clock cycle (i.e. it has a transition duty cycle of 100%)

\[ P_{\text{DYN}} = \frac{f C_L}{2} C_L V_{\text{DD}}^2 \]

Clock distribution can cause significant power dissipation
End of Lecture 42