Overdrive

Propagation Delay in Multiple Levels of Logic

Optimally Driving Large Capacitive Loads
Review from last lecture

Device Sizing – minimum size driving $C_{REF}$

$k$-input NOR

$t_{PROP} = \, \, ?$

$\begin{align*}
    t_{PROP} &= 0.5t_{REF} + \frac{3k}{2}t_{REF} \\
    t_{PROP} &= \left(\frac{3k+1}{2}\right)t_{REF}
\end{align*}$

$FI = \frac{C_{REF}}{2}$

$k$-input NOR

$t_{PROP} = \, \, ?$

$\begin{align*}
    t_{PROP} &= \frac{3}{2}t_{REF} + \frac{k}{2}t_{REF} \\
    t_{PROP} &= \frac{3+k}{2}t_{REF}
\end{align*}$

$FI = \frac{C_{REF}}{2}$
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Analysis strategy: Express delays in terms of those of reference inverter

Reference Inverter

\[ \text{C}_{\text{REF}} = \text{C}_{\text{IN}} = 4 \text{C}_{\text{OX}} \text{W}_{\text{MIN}} \text{L}_{\text{MIN}} \]

\[ R_{\text{PDREF}} = \frac{\text{L}_{\text{MIN}}}{\mu_n \text{C}_{\text{OX}} \text{W}_{\text{MIN}} (\text{V}_{\text{DD}} - V_{Tn})} = \frac{\text{L}_{\text{MIN}}}{\mu_n \text{C}_{\text{OX}} \text{W}_{\text{MIN}} (0.8 \text{V}_{\text{DD}})} \]

\[ t_{\text{REF}} = t_{\text{HLREF}} + t_{\text{LHREF}} = 2 R_{\text{PDREF}} \text{C}_{\text{REF}} \]

Assume \( \frac{\mu_n}{\mu_p} = 3 \)

\( \text{W}_n = \text{W}_{\text{MIN}}, \text{W}_p = 3 \text{W}_{\text{MIN}} \)

In 0.5μm process \( t_{\text{REF}} = 20 \text{ps}, \text{C}_{\text{REF}} = 4 \text{fF}, R_{\text{PDREF}} = 2.5 \text{K} \)

Ln=Lp=LMIN
Review from last lecture

Propagation Delay with Stage Loading

\[ t_{\text{REF}} = 2R_{P_{\text{Dref}}} C_{\text{REF}} \]
\[ C_{\text{REF}} = C_{\text{IN}} = 4C_{\text{OX}} W_{\text{MIN}} L_{\text{MIN}} \]

Fl of a capacitor

\[ F_{\text{I}_C} = \frac{C}{C_{\text{REF}}} \]

Fl of a gate (input k)

\[ F_{\text{I}_G} = \frac{C_{\text{IN}k}}{C_{\text{REF}}} \]

Fl of an interconnect

\[ F_{\text{I}_I} = \frac{C_{\text{INI}}}{C_{\text{REF}}} \]

Overall Fl

\[ F_{\text{I}} = \sum_{\text{Gates}} C_{\text{INGi}} + \sum_{\text{Capacitances}} C_{\text{INCi}} + \sum_{\text{Interconnects}} C_{\text{INII}} \]

Fl can be expressed either in units of capacitance or normalized to \( C_{\text{REF}} \)

Most commonly Fl is normalized but must determine from context
Review from last lecture

Propagation Delay Through Multiple Stages of Logic with Stage Loading

(assuming gate drives are all same as that of reference inverter)

Identify the gate path from A to F

\[ t_{\text{PROP}k} = t_{\text{REF}} F_{I(k+1)} \]

Propagation delay from A to F:

\[ t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^{n} F_{I(k+1)} \]
Digital Circuit Design

- Hierarchical Design
- Basic Logic Gates
- Properties of Logic Families
- Characterization of CMOS Inverter
- Static CMOS Logic Gates
  - Ratio Logic
- Propagation Delay
  - Simple analytical models
  - Elmore Delay
- Sizing of Gates
- Propagation Delay with Multiple Levels of Logic
- Optimal driving of Large Capacitive Loads
  - Power Dissipation in Logic Circuits
  - Other Logic Styles
  - Array Logic
  - Ring Oscillators

done

partial
Overdrive Factors

The factor by which the devices are scaled above those of the reference inverter is termed the overdrive factor, OD.

Scaling all widths by a constant does not compromise the symmetry between the rise and fall times.

Judicious use of overdrive can dramatically improve the speed of digital circuits.

Large overdrive factors are often used.
Define the Asymmetric Overdrive Factors of the stage to be the factor by which PU and PD resistors are scaled relative to those of the reference inverter.

\[ R_{PDEFF} = \frac{R_{PDREF}}{OD_{HL}} \]

\[ R_{PUEFF} = \frac{R_{PUREF}}{OD_{LH}} \]

If inverter sized for equal rise/fall, define OD by \( OD_{HL} = OD_{LH} = OD \)

\[ t_{HL} = t_{LH} = \frac{R_{PDREF}}{OD} \]

\[ C = R_{PDREF} C_{REF} \frac{F_{IL}}{OD} \]

\[ t_{PROP} = t_{LH} + t_{HL} = t_{REF} \frac{F_{IL}}{OD} \]

OD may be larger or smaller than 1
Propagation Delay with Over-drive Capability

Example

Compare the propagation delays. Assume the OD is 900 in the second case and 30 in the third case.
Propagation Delay in Multiple-Levels of Logic with Stage Loading

\[ t_k = t_{PROP_k} \]

Notation: \( t_{PROP} = t_{REF} \sum_{k=1}^{n} \frac{F_{I(k+1)}}{OD_k} \)

\( F_{I_k} \) denotes the total loading on stage \( k \) which is the sum of the \( F_I \) of all loading on stage \( k \).
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Will consider an example with the five cases

- Equal rise/fall (no overdrive)
- Equal rise/fall with overdrive
- Minimum Sized
- Asymmetric Overdrive
- Combination of equal rise/fall, minimum size and overdrive

Will develop the analysis methods as needed
Propagation Delay in Multiple-Levels of Logic with Stage Loading

- Equal rise/fall (no overdrive)
- Equal rise/fall with overdrive
- Minimum Sized
- Asymmetric overdrive
- Combination of equal rise/fall, minimum size and overdrive
Driving Notation

- Equal rise/fall (no overdrive)
- Equal rise/fall with overdrive
- Minimum Sized
- Asymmetric Overdrive

Notation will be used only if it is not clear from the context what sizing is being used
Define the Asymmetric Overdrive Factors of the stage to be the factors by which PU and PD resistors are scaled relative to those of the reference inverter.

\[ R_{PDEFF} = \frac{R_{PDREF}}{OD_{HL}} \quad R_{PUEFF} = \frac{R_{PUREF}}{OD_{LH}} \]
Propagating Delay in Multiple-Levels of Logic with Stage Loading

Asymmetric Overdrive

\[ \text{PROP LH LH REF IL} \]

If inverter is not equal rise/fall

\[ t_{\text{HL}} = \frac{R_{\text{PDREF}}}{\text{OD}_{\text{HL}}} \quad C_L = \frac{1}{2} t_{\text{REF}} \frac{F_{\text{IL}}}{\text{OD}_{\text{HL}}} \]

\[ t_{\text{LH}} = \frac{R_{\text{PURE}}}{\text{OD}_{\text{LH}}} \quad C_L = \frac{1}{2} t_{\text{REF}} \frac{F_{\text{IL}}}{\text{OD}_{\text{LH}}} \]

\[ t_{\text{PROP}} = t_{\text{HL}} + t_{\text{LH}} = \frac{1}{2} t_{\text{REF}} F_{\text{IL}} \left( \frac{1}{\text{OD}_{\text{HL}}} + \frac{1}{\text{OD}_{\text{LH}}} \right) \]

\[ t_{\text{PROP}} = t_{\text{LH}} + t_{\text{HL}} = t_{\text{REF}} \frac{F_{\text{IL}}}{\text{OD}} \]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Asymmetric Overdrive

Asymmetric Overdrive

\[ t_{PROP} = t_{HL} + t_{LH} = \frac{1}{2} t_{REF} F_{IL} \left( \frac{1}{OD_{HL}} + \frac{1}{OD_{LH}} \right) \]

When propagating through n stages:

\[ t_{PROP} = t_{REF} \cdot \left( \frac{1}{2} \sum_{k=1}^{n} F_{I(k+1)} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right) \]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

**Overdrive Notation**

Equal Rise/Fall with overdrive OD

Rise/Fall may be different with overdrive \( \text{OD}_{HL} \) and \( \text{OD}_{LH} \)

**Examples**

Equal Rise/Fall with overdrive of 8

If \( W_n = W_{\text{MIN}} \), minimum sized inverter
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Equal rise-fall gates, no overdrive

In 0.5u proc \( t_{\text{REF}}=20\text{ps}, \)
\( C_{\text{REF}}=4fF, R_{\text{PDREF}}=2.5K \)

\[ t_{\text{REF}} = 2t_{\text{HL-REF}} \]

\[ t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^{n} F_{k+1} \]
## Propagation Delay in Multiple-Levels of Logic with Stage Loading

*Equal rise-fall gates, no overdrive*

<table>
<thead>
<tr>
<th>$C_{IN}/C_{REF}$</th>
<th>Equal Rise/Fall</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inverter</td>
<td>1</td>
</tr>
<tr>
<td>NOR</td>
<td>$3k+1/4$</td>
</tr>
<tr>
<td>NAND</td>
<td>$3+k/4$</td>
</tr>
<tr>
<td>Overdrive</td>
<td></td>
</tr>
<tr>
<td>Inverter</td>
<td></td>
</tr>
<tr>
<td>HL</td>
<td>1</td>
</tr>
<tr>
<td>LH</td>
<td>1</td>
</tr>
<tr>
<td>NOR</td>
<td>1</td>
</tr>
<tr>
<td>HL</td>
<td>1</td>
</tr>
<tr>
<td>LH</td>
<td>1</td>
</tr>
<tr>
<td>NAND</td>
<td>1</td>
</tr>
<tr>
<td>HL</td>
<td>1</td>
</tr>
<tr>
<td>LH</td>
<td>1</td>
</tr>
</tbody>
</table>

$t_{PROP}/t_{REF} = \sum_{k=1}^{n} F_{i(k+1)}$

$t_{PROP} = t_{REF} \sum_{k=1}^{5} F_{k+1}$
Equal rise-fall gates, no overdrive

In 0.5μm process, \( t_{REF} = 20 \text{ps} \), \( C_{REF} = 4fF \), \( R_{PDREF} = 2.5K \)

\[
\sum_{k=1}^{5} F_{k+1} = 10.25 + 4.25 + 4.25 + 1.25 + 12.5
\]

\[
t_{PROP} = t_{REF} \sum_{k=1}^{5} F_{k+1}
\]

\[
t_{PROP} = t_{REF} (10.25 + 4.25 + 4.25 + 1.25 + 12.5)
\]

\[
t_{PROP} = 32.5t_{REF}
\]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Equal rise-fall gates, with overdrive

\[ t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^{n} \frac{F_{k+1}}{\text{OD}_k} \]

In 0.5u proc \( t_{\text{REF}}=20\text{ps}, \) \( C_{\text{REF}}=4\text{fF}, R_{\text{PDREF}}=2.5\text{K} \)
### Propagation Delay in Multiple-Levels of Logic with Stage Loading

*Equal rise-fall gates, with overdrive*

<table>
<thead>
<tr>
<th>$C_{\text{IN}}/C_{\text{REF}}$</th>
<th>Equal Rise/Fall</th>
<th>Equal Rise/Fall (with OD)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inverter</td>
<td>1</td>
<td>OD</td>
</tr>
<tr>
<td>NOR</td>
<td>$\frac{3k+1}{4}$</td>
<td>$\frac{3k+1}{4} \cdot \text{OD}$</td>
</tr>
<tr>
<td>NAND</td>
<td>$\frac{3+k}{4}$</td>
<td>$\frac{3+k}{4} \cdot \text{OD}$</td>
</tr>
<tr>
<td>Overdrive</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Inverter</td>
<td></td>
<td></td>
</tr>
<tr>
<td>HL</td>
<td>1</td>
<td>OD</td>
</tr>
<tr>
<td>LH</td>
<td>1</td>
<td>OD</td>
</tr>
<tr>
<td>NOR</td>
<td>1</td>
<td>OD</td>
</tr>
<tr>
<td>HL</td>
<td>1</td>
<td>OD</td>
</tr>
<tr>
<td>NAND</td>
<td>1</td>
<td>OD</td>
</tr>
<tr>
<td>HL</td>
<td>1</td>
<td>OD</td>
</tr>
<tr>
<td>LH</td>
<td>1</td>
<td>OD</td>
</tr>
</tbody>
</table>

$\text{PROP} = t_{\text{REF}} \sum_{k=1}^{n} \frac{F_{k+1}}{\text{OD}_k}$

- $t_{\text{PROP}}$ represents the propagation delay.
- $t_{\text{REF}}$ is the reference delay.
- $F_{k+1}$ are the functions of the logic gates.
- $\text{OD}_k$ refers to the overdrive conditions.
Equal rise-fall gates, with overdrive

\[ t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^{n} \frac{F_{k+1}}{\text{OD}_k} \]

\[ t_{\text{PROP}} = t_{\text{REF}} \left( \frac{14.25}{8} + \frac{13}{1} + \frac{4.25}{6} + \frac{5}{1} + \frac{12.5}{4} \right) \]

\[ t_{\text{PROP}} = 23.6 \ t_{\text{REF}} \]

In 0.5u proc  \( t_{\text{REF}} = 20 \text{ps} \),
\( C_{\text{REF}} = 4fF \), \( R_{\text{PDREF}} = 2.5K \)

\( F_{I2} = 14.25 \)
\( F_{I3} = 13 \)
\( F_{I4} = 4.25 \)
\( F_{I5} = 5 \)
\( F_{I6} = 12.5 \)
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Minimum-sized gates

In 0.5u proc \( t_{\text{REF}}=20\text{ps}, \quad C_{\text{REF}}=4\text{fF}, R_{PDREF}=2.5\text{K} \)
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Minimum-sized gates

\[ t_{\text{PROP}} = t_{\text{REF}} \cdot \square \]
Propagation Delay with Minimum-Sized Gates

\[ t_{\text{PROP}} = t_{\text{REF}} \cdot ? \]

\[ t_{\text{PROP}} = R_{\text{PD}} C_L + R_{\text{PU}} C_L \]

\[ t_{\text{PROP}} = \left( \frac{R_{\text{PD REF}}}{OD_{\text{HL}}} + \frac{R_{\text{PD REF}}}{OD_{\text{LH}}} \right) C_L \]

\[ t_{\text{PROP}} = R_{\text{PD REF}} \left( \frac{1}{OD_{\text{HL}}} + \frac{1}{OD_{\text{LH}}} \right) (C_{\text{REF}} F_{\text{LOAD}}) \]

\[ t_{\text{PROP}} = \left( \frac{1}{OD_{\text{HL}}} + \frac{1}{OD_{\text{LH}}} \right) (R_{\text{PD REF}} C_{\text{REF}}) F_{\text{LOAD}} \]

But recall

\[ t_{\text{REF}} = 2 C_{\text{REF}} R_{\text{PD REF}} \]

Thus

\[ t_{\text{PROP}} = \left( \frac{1}{OD_{\text{HL}}} + \frac{1}{OD_{\text{LH}}} \right) \left( \frac{t_{\text{REF}}}{2} \right) F_{\text{LOAD}} \]

Now, for \( k \) levels of logic

\[ t_{\text{PROP}} = \frac{t_{\text{REF}}}{2} \sum_{k=1}^{n} F_{l(k+1)} \left( \frac{1}{OD_{\text{HL}}^k} + \frac{1}{OD_{\text{LH}}^k} \right) \]

\[ t_{\text{PROP}} = t_{\text{REF}} \left( \frac{1}{2} \sum_{k=1}^{n} F_{l(k+1)} \left( \frac{1}{OD_{\text{HL}}^k} + \frac{1}{OD_{\text{LH}}^k} \right) \right) \]
Propagation Delay with Minimum-Sized Gates

\[
t_{\text{PROP}} = t_{\text{REF}} \cdot \left( \frac{1}{2} \sum_{k=1}^{n} F_{i(k+1)} \left( \frac{1}{OD_{HL_k}} + \frac{1}{OD_{LH_k}} \right) \right)
\]

Still need OD\textsubscript{HL} and OD\textsubscript{LH}
Still need \( F_i \)
Propagation Delay with minimum-sized gates

\[ OD_{HL} = \frac{1}{3k} \]

\[ OD_{HL} = 1 \]

\[ OD_{LH} = 1/k \]

\[ OD_{LH} = \frac{1}{3} \]

\[ FI = 2C_{OX}W_{MIN}L_{MIN} \]

\[ C_{REF} = 4C_{OX}W_{MIN}L_{MIN} \]

\[ FI = \frac{C_{REF}}{2} \]
## Propagation Delay in Multiple-Levels of Logic with Stage Loading

**Minimum-sized gates**

<table>
<thead>
<tr>
<th>C(<em>{\text{IN}})/C(</em>{\text{REF}})</th>
<th>Equal Rise/Fall</th>
<th>Equal Rise/Fall (with OD)</th>
<th>Minimum Sized</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inverter</td>
<td>1</td>
<td>OD</td>
<td></td>
</tr>
<tr>
<td>NO(_R)</td>
<td>(\frac{3k+1}{4})</td>
<td>(\frac{3k+1}{4}) * OD</td>
<td></td>
</tr>
<tr>
<td>NAND</td>
<td>(\frac{3+k}{4})</td>
<td>(\frac{3+k}{4}) * OD</td>
<td></td>
</tr>
<tr>
<td>Overdrive</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Inverter</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HL</td>
<td>1</td>
<td>OD</td>
<td></td>
</tr>
<tr>
<td>LH</td>
<td>1</td>
<td>OD</td>
<td></td>
</tr>
<tr>
<td>NOR</td>
<td>1</td>
<td>OD</td>
<td></td>
</tr>
<tr>
<td>HL</td>
<td>1</td>
<td>OD</td>
<td></td>
</tr>
<tr>
<td>LH</td>
<td>1</td>
<td>OD</td>
<td></td>
</tr>
<tr>
<td>NAND</td>
<td>1</td>
<td>OD</td>
<td></td>
</tr>
<tr>
<td>HL</td>
<td>1</td>
<td>OD</td>
<td></td>
</tr>
<tr>
<td>LH</td>
<td>1</td>
<td>OD</td>
<td></td>
</tr>
</tbody>
</table>

\(t_{\text{PROP}}/t_{\text{REF}}\) = \(\sum_{k=1}^{n} F_{f(k+1)} / \sum_{k=1}^{n} F_{f(k+1)} * OD_k\)

\(OD_{HL} = 1\)

\(OD_{LH} = \frac{1}{3k}\)

\(OD_{HL} = 1/k\)

\(OD_{LH} = \frac{1}{3}\)

\(F_L = \frac{C_{\text{REF}}}{2}\)
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Minimum-sized gates

<table>
<thead>
<tr>
<th>CIN/CREF</th>
<th>Equal Rise/Fall</th>
<th>Equal Rise/Fall (with OD)</th>
<th>Minimum Sized</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inverter</td>
<td>1</td>
<td>OD</td>
<td>1/2</td>
</tr>
<tr>
<td>NOR</td>
<td>3k+1/4</td>
<td>3k+1/4•OD</td>
<td>1/2</td>
</tr>
<tr>
<td>NAND</td>
<td>3+k/4</td>
<td>3+k/4•OD</td>
<td>1/2</td>
</tr>
</tbody>
</table>

Overdrive

<table>
<thead>
<tr>
<th>Inverter</th>
<th>Equal Rise/Fall</th>
<th>Minimum Sized</th>
</tr>
</thead>
<tbody>
<tr>
<td>HL</td>
<td>1</td>
<td>OD</td>
</tr>
<tr>
<td>LH</td>
<td>1</td>
<td>OD</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>NOR</th>
<th>Equal Rise/Fall</th>
<th>Minimum Sized</th>
</tr>
</thead>
<tbody>
<tr>
<td>HL</td>
<td>1</td>
<td>OD</td>
</tr>
<tr>
<td>LH</td>
<td>1</td>
<td>OD</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>NAND</th>
<th>Equal Rise/Fall</th>
<th>Minimum Sized</th>
</tr>
</thead>
<tbody>
<tr>
<td>HL</td>
<td>1</td>
<td>OD</td>
</tr>
<tr>
<td>LH</td>
<td>1</td>
<td>OD</td>
</tr>
</tbody>
</table>

\[ t_{PROP} / t_{REF} = \sum_{k=1}^{n} F_{I(k+1)} / \sum_{k=1}^{n} F_{I(k+1)} / OD_k = \frac{1}{2} \sum_{k=1}^{n} F_{I(k+1)} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \]

\[ F_I = \frac{C_{REF}}{2} \]
Minimum-sized gates

\[ t_{\text{PROP}} = t_{\text{REF}} \cdot \left( \frac{1}{2} \sum_{k=1}^{5} F_{l(k+1)} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right) \]

\[ t_{\text{PROP}} = t_{\text{REF}} \cdot \frac{1}{2} \left( \frac{13}{2} (3+3) + 1(12+1) + 1(6+10) + \frac{1}{2}(9+1) + 12.5(2+3) \right) \]

\[ t_{\text{PROP}} = 63.25 \cdot t_{\text{REF}} \]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Asymmetric-sized gates

\[ t_{\text{PROP}} = t_{\text{REF}} \cdot ? \]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

**Asymmetric-sized gates**

<table>
<thead>
<tr>
<th></th>
<th>Equal Rise/Fall</th>
<th>Equal Rise/Fall (with OD)</th>
<th>Minimum Sized</th>
<th>Asymmetric OD (OD(<em>{HL}), OD(</em>{LH}))</th>
</tr>
</thead>
<tbody>
<tr>
<td>C(<em>{IN}/C</em>{REF})</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Inverter</td>
<td>1</td>
<td>OD</td>
<td>1/2</td>
<td>(\frac{OD_{HL}+3\cdot OD_{LH}}{4})</td>
</tr>
<tr>
<td>NOR</td>
<td>(\frac{3k+1}{4})</td>
<td>(\frac{3k+1}{4}\cdot OD)</td>
<td>1/2</td>
<td>(\frac{OD_{HL}+3k\cdot OD_{LH}}{4})</td>
</tr>
<tr>
<td>NAND</td>
<td>(\frac{3+k}{4})</td>
<td>(\frac{3+k}{4}\cdot OD)</td>
<td>1/2</td>
<td>(k\cdot OD_{HL}+3\cdot OD_{LH})</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Overdrive</th>
<th>Inverter</th>
<th>Equal Rise/Fall</th>
<th>Minimum Sized</th>
<th>Asymmetric OD (OD(<em>{HL}), OD(</em>{LH}))</th>
</tr>
</thead>
<tbody>
<tr>
<td>HL</td>
<td>1</td>
<td>OD</td>
<td>1</td>
<td>OD(_{HL})</td>
</tr>
<tr>
<td>LH</td>
<td>1</td>
<td>OD</td>
<td>1/3</td>
<td>OD(_{LH})</td>
</tr>
<tr>
<td>NOR</td>
<td>HL</td>
<td>1</td>
<td>1</td>
<td>OD(_{HL})</td>
</tr>
<tr>
<td></td>
<td>LH</td>
<td>1</td>
<td>1/(3k)</td>
<td>OD(_{LH})</td>
</tr>
<tr>
<td>NAND</td>
<td>HL</td>
<td>1</td>
<td>1/k</td>
<td>OD(_{HL})</td>
</tr>
<tr>
<td></td>
<td>LH</td>
<td>1</td>
<td>1/3</td>
<td>OD(_{LH})</td>
</tr>
</tbody>
</table>

\[t_{PROP}/t_{REF} = \sum_{k=1}^{n} F_{l(k+1)} \sum_{k=1}^{n} \frac{F_{l(k+1)}}{OD_{k}} + \frac{1}{2} \sum_{k=1}^{n} F_{l(k+1)} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) + \frac{1}{2} \sum_{k=1}^{n} F_{l(k+1)} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right)\]

\[t_{PROP} = t_{REF} \cdot \left( \frac{1}{2} \sum_{k=1}^{n} F_{l(k+1)} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right)\]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Asymmetric-sized gates

\[ t_{\text{PROP}} = t_{\text{REF}} \cdot \left( \frac{1}{2} \sum_{k=1}^{5} F_{k+1} \left( \frac{1}{\text{OD}_{\text{HLk}}} + \frac{1}{\text{OD}_{\text{LHk}}} \right) \right) \]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

*Mixture of Minimum-sized gates, equal rise/fall gates and OD*

\[ t_{PROP} = t_{REF} \cdot ? \]
Driving Notation

- Equal rise/fall (no overdrive)
- Equal rise/fall with overdrive
- Minimum Sized
- Asymmetric Overdrive
Propagation Delay in Multiple-Levels of Logic with Stage Loading

*Mixture of Minimum-sized gates, equal rise/fall gates and OD*

\[ t_{\text{PROP}} = t_{\text{REF}} \left( \frac{1}{2} \sum_{k=1}^{5} F_{i(k+1)} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right) \]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

*Mixture of Minimum-sized gates, equal rise/fall gates and OD*

\[
t_{\text{PROP}} = t_{\text{REF}} \cdot \left( \frac{1}{2} \sum_{k=1}^{5} F_{(k+1)} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right)
\]
Propagation Delay in Multiple-Levels of Logic with Stage Loading

- Equal rise/fall (no overdrive)
- Equal rise/fall with overdrive
- Minimum Sized
- Asymmetric overdrive
- Combination of equal rise/fall, minimum size and overdrive

\[ t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^{n} F_{l(k+1)} \]

\[ t_{\text{PROP}} = t_{\text{REF}} \sum_{k=1}^{n} \frac{F_{l(k+1)}}{OD_k} \]

\[ t_{\text{PROP}} = t_{\text{REF}} \left( \frac{1}{2} \sum_{k=1}^{n} F_{l(k+1)} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right) \]

\[ t_{\text{PROP}} = t_{\text{REF}} \left( \frac{1}{2} \sum_{k=1}^{n} F_{l(k+1)} \left( \frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right) \]
Recall

Propagation Delay in Multiple-Levels of Logic with Stage Loading

**Overdrive**

Define the Overdrive Factor of the stage to be the factor by which PU and PD resistors are scaled relative to those of the reference inverter.

\[
R_{PDEFF} = \frac{R_{PDREF}}{OD_{HL}} \quad R_{PUEFF} = \frac{R_{PUREF}}{OD_{LH}}
\]

If inverter sized for equal rise/fall, \( OD_{HL} = OD_{LH} = OD \)

\[
t_{HL} = t_{LH} = \frac{R_{PDREF}}{OD} C_L = R_{PDREF} C_{REF} \frac{F_{IL}}{OD}
\]

\[
t_{PROP} = t_{LH} + t_{HL} = t_{REF} \frac{F_{IL}}{OD}
\]

OD may be larger or smaller than 1
Recall

Propagation Delay in Multiple-Levels of Logic with Stage Loading

*Overdrive*

\[ V_{IN} \rightarrow \triangle \rightarrow V_{OUT} \]

\[ C_L \]

\[ t_{\text{PROP}} = t_{\text{HL}} + t_{\text{IL}} = t_{\text{REF}} \cdot \frac{F_{\text{IL}}}{OD} \]

If inverter is not equal rise/fall

\[ t_{\text{HL}} = \frac{R_{\text{PDREF}}}{O_{\text{DL}}} \cdot C_L = \frac{1}{2} t_{\text{REF}} \cdot \frac{F_{\text{IL}}}{O_{\text{DL}}} \]

\[ t_{\text{IL}} = \frac{R_{\text{PUREF}}}{O_{\text{DL}}} \cdot C_L = \frac{1}{2} t_{\text{REF}} \cdot \frac{F_{\text{IL}}}{O_{\text{DL}}} \]

\[ t_{\text{PROP}} = t_{\text{HL}} + t_{\text{IL}} = \frac{1}{2} t_{\text{REF}} \cdot F_{\text{IL}} \cdot \left( \frac{1}{O_{\text{DL}}} + \frac{1}{O_{\text{DL}}} \right) \]