Digital Circuits

- Elmore Delay
- Power Dissipation
- Other Logic Styles
- Dynamic Logic Circuits
Propagation Delay in “Logic Effort” approach

\[ t_{\text{PROP}} = \sum_{k=1}^{n} f_k = \sum_{k=1}^{n} g_k h_k = \sum_{k=1}^{n} \frac{F_{l(k+1)}}{\text{OD}_k} \]

- Note with the exception of the \( t_{\text{REF}} \) scaling factor, this expression is identical to what we have derived previously.

- Probably more tedious to use the “Logical Effort” approach.

- Extensions to asymmetric overdrive factors may not be trivial.

- Extensions to include parasitics may be tedious as well.

- Logical Effort is widely used throughout the industry.
Elmore Delay Calculations

For \( x_1 < x_2 < x_3 \)
Review from Last Time

Elmore Delay Calculations

A lumped element model of transmission line

Even this lumped model is 4-th order and a closed-form solution is very tedious!

Need a quick (and reasonably good) approximation to the delay of a delay line.
Elmore Delay Calculations

It can be shown that this is a reasonably good approximation to the actual delay.  
Numbering is critical (resistors and capacitors numbered from input to output).  
As stated, only applies to this specific structure.
Elmore Delay Calculations

Elmore delay:

\[ t_{PD} = \sum_{i=1}^{n} \left( C_i \sum_{j=1}^{i} R_j \right) \]

- Note error in text on Page 161 of first edition of WH

\[ t_{pd} = \sum_{i}^{N} R_{n-i} C_i = \sum_{i=1}^{N} C_i \sum_{j=i}^{i} R_j \]

- Not detailed definition on Page 150 of second edition of WH
Elmore delay\cite{1} is a simple approximation to the delay through an \textbf{RC network} in an electronic system. It is often used in applications such as \textbf{logic synthesis}, \textbf{delay calculation}, \textbf{static timing analysis}, \textbf{placement} and \textbf{routing}, since it is simple to compute (especially in tree structured networks, which are the vast majority of signal nets within ICs) and is reasonably accurate. Even where it is not accurate, it is usually faithful, in the sense that reducing the Elmore delay will almost always reduce the true delay, so it is still useful in optimization.

\begin{equation}
    t_{PD} = \sum_{i=1}^{n} \left( C_i \sum_{j=1}^{i} R_j \right)
\end{equation}

\cite{1} W.C. Elmore. \textit{The Transient Analysis of Damped Linear Networks with Particular Regard to Wideband Amplifiers}. J. Applied Physics, vol. 19(1), 1948.
Elmore Delay Calculations

Example:

Elmore delay:
\[ t_{PD} = \sum_{i=1}^{4} \left( C_i \sum_{j=1}^{n} R_j \right) \]

\[ t_{PD} = \sum_{i=1}^{4} (t_i) \]

What is really happening?

- Creating 4 first-order circuits
- Delay to \( V_1, V_2, V_3 \) and \( V_4 \) calculated separately by considering capacitors one at a time and assuming others are 0
Elmore Delay Calculations

Extensions:

Lumped Network Model:
Elmore Delay Calculations

Extensions:

1. Create a lumped element model

2. Identify a path from input to output
Elmore Delay Calculations

Extensions:

3. Renumber elements along path from input to output and neglect off-path elements.

4. Use Elmore Delay equation for elements on this RC network

\[ t_{PD} = \sum_{i=1}^{4} \left( C_i \sum_{j=1}^{i} R_j \right) \]
Elmore Delay Calculations

How is a resistive load handled?
Elmore Delay Calculations

Example with resistive load:

\[
t = C_i R_j
\]

Elmore delay:

\[
t_{PD} = \sum_{i=1}^{4} \left( C_i \sum_{j=1}^{i} R_j \right)
\]

where

\[
t_{PD} = \sum_{i=1}^{4} (t_i)
\]

\[
t_i = C_i \sum_{j=1}^{i} R_j \quad j = 1, 2, 3
\]

\[
t_4 = C_4 \left( \frac{\sum_{j=1}^{4} R_j}{R_5} \right)
\]

\[
t_4 = \left( \frac{(R_1 + R_2 + R_3)C_4}{R_5} \right)
\]
Elmore Delay Calculations

With resistive load:

\[ t_{PD} = \sum_{i=1}^{n-1} \left( C_i \sum_{j=1}^{i} R_j \right) + C_n \left( \frac{\sum_{j=1}^{n} R_j}{R_L} \right) \]

Actually, \( R_L \) affects all of the delays and a modestly better but modestly more complicated delay model is often used.
Elmore Delay Calculations

Example with resistive load (modestly better model):

\[ \begin{align*}
&\text{Elmore delay:} \\
&\quad t_1 = \left( R_1 \parallel \left[ R_2 + R_3 + R_4 + R_5 \right] \right) C_1 \\
&\quad t_2 = \left( \frac{R_1 + R_2}{R_3 + R_4 + R_5} \right) C_2 \\
&\quad t_3 = \left( \frac{R_1 + R_2 + R_3}{R_4 + R_5} \right) C_2 \\
&\quad t_4 = \left( \frac{R_1 + R_2 + R_3 + R_4}{R_5} \right) C_4 \\
&\text{where} \\
&\quad t_{PD} = \sum_{i=1}^{4} t_i \\
&\quad t_i = C_i \left( \sum_{j=1}^{i} R_j \right) \parallel \left( \sum_{j=i+1}^{5} R_j \right) \\
&\quad j = 1, 2, 3, 4
\end{align*} \]
Elmore Delay Calculations

With resistive load (modestly better model):

\[ t_{PD} = \sum_{i=1}^{n} C_i \left( \left[ \sum_{j=1}^{i} R_j \right] \parallel \left[ \sum_{j=i+1}^{n+1} R_j \right] \right) \]
Elmore Delay Calculations

How are the number of stages chosen?

- For hand analysis, keep number of stages small (maybe 3 or 4 for simple delay line) if possible.
- If “faithfulness” is important, should keep the number of stages per unit length constant.
Elmore Delay Calculations
Elmore Delay Calculations

\[ t_1 = R(C + C_{REF}) \]
\[ t_2 = 3RC \]
\[ t_3 = 5R \left( C + \frac{1}{2}C_{REF} \right) \]
\[ t_4 = \left[ \frac{6R}{R_L} \right]^{25/4} C_{REF} \]
\[ t_5 = t_{REF} \cdot \frac{20}{5} \]

\[ t_{PROP} = \sum_{i=1}^{5} t_i \]
Digital Circuit Design

- Hierarchical Design
- Basic Logic Gates
- Properties of Logic Families
- Characterization of CMOS Inverter
- Static CMOS Logic Gates
  - Ratio Logic
- Propagation Delay
  - Simple analytical models
    - FI/OD
    - Logical Effort
  - Elmore Delay
- Sizing of Gates

- Propagation Delay with Multiple Levels of Logic
- Optimal driving of Large Capacitive Loads
- Power Dissipation in Logic Circuits
  - Other Logic Styles
  - Array Logic
  - Ring Oscillators

- done
- partial
Assume current periodic with period $T_{CL}$

$$P_{AVG,T} = \frac{1}{T_{CL}} \int_{t_1}^{t_1+T_{CL}} V_{DD}I_{DD}(t)dt$$
Power Dissipation in Logic Circuits

Types of Power Dissipation

- Static
- Pipe
- Dynamic
- Leakage
  - Gate
  - Diffusion
  - Drain
If Boolean output averages H and L 50% of the time

\[ P_{\text{STAT, AVG}} = \frac{P_H + P_L}{2} \]

\[ P_{\text{STAT, AVG}} = \frac{V_{DD}(I_{DDH} + I_{DDL})}{2} \]

• Generally decreases with \( V_{DD} \)
• \( I_{DDH} = I_{DDL} = 0 \) for static CMOS gates so \( P_{\text{STAT}} = 0 \)
• A major source of power dissipation in ratio logic circuits and the major reason CMOS is so widely used
Pipe Power Dissipation

Due to conduction of both PUN and PDN during transitions

- Can be made small if transitions are fast
- Usually negligible in Static CMOS circuits
Dynamic Power Dissipation

Due to charging and discharging $C_L$ on logic transitions

$C_L$ dissipates no power but PUN and PDN dissipate power during charge and discharge of $C_L$

$C_L$ includes all gate input capacitances of loads and interconnect capacitances
Dynamic Power Dissipation

Energy supplied by $V_{DD}$ when $C_L$ charges:

\[
E = \int_{t_1}^{\infty} V_{DD} I_{DD}(t) dt
\]

\[
I_{DD} = C_L \frac{dV_C}{dt}
\]

\[
E = \int_{t_1}^{\infty} V_{DD} C_L \frac{dV_C}{dt} dt
\]

\[
E = \int_{V_C=0}^{V_{DD}} V_{DD} C_L dV_C = V_{DD} C_L \int_{V_C=0}^{V_{DD}} dV_C = V_{DD} C_L V_C \bigg|_{V_C=0}^{V_{DD}} = V_{DD}^2 C_L
\]

Energy stored in $C_L$ after $C_L$ is charged to $V_{DD}$:

\[
E = \frac{1}{2} C_L V_{DD}^2
\]
Dynamic Power Dissipation

Energy supplied by \( V_{dd} \) and dissipated in \( R_{PU} \) when \( C_L \) charges

\[
E_{DIS} = \frac{1}{2} C_L V_{DD}^2
\]

Energy stored on \( C_L \) after L-H transition

\[
E_{STORE} = \frac{1}{2} C_L V_{DD}^2
\]

Thus, energy from \( V_{dd} \) for one L-H: H-L output transition sequence is

\[
E = E_{DIS} + E_{STORE} = C_L V_{DD}^2
\]

When the output transitions from H to L, energy stored on \( C_L \) is dissipated in PDN.

If \( f \) is the average transition rate of the output, determine \( P_{AVG} \).
Dynamic Power Dissipation

Energy from $V_{DD}$ for one L-H: H-L output transition sequence is

$$E = C_L V_{DD}^2$$

If $f$ is the average transition rate of the output, determine $P_{AVG}$

$$P_{AVG} = \frac{E}{T} = Ef$$

$$P_{DYN} = fC_L V_{DD}^2$$

If a gate has a transition duty cycle of 50% with a clock frequency of $f_{CL}$

$$P_{DYN} = \frac{f_{CL} C_L V_{DD}^2}{2}$$

Note dependent on the square of $V_{DD}$! .... Want to make VDD small !!!

Major source of power dissipation in many static CMOS circuits for $L_{min}>0.1u$
All power is dissipated in pull-up and pull-down devices.

$C_L$ dissipates no power but PUN and PDN dissipate power when charging and discharging $C_L$.

Dynamic power dissipation reduced by more (often much more) than a factor of 2 if minimum sizing strategy is used.
Leakage Power Dissipation

- **Gate**
  - with very thin gate oxides, some gate leakage current flows
  - major concern in 60nm and smaller processes
  - actually a type of static power dissipation

- **Diffusion**
  - Leakage across a reverse-biased pn junction
  - Dependent upon total diffusion area
  - May actually be dominant power loss on longer-channel devices
  - Actually a type of static power dissipation

- **Drain**
  - channel current due to small $V_{GS} - V_T$
  - of significant concern only with low $V_{DD}$ processes
  - actually a type of static power dissipation
Example: Determine the dynamic power dissipation in the last stage of a 6-stage CMOS pad driver if used to drive a 10pF capacitive load if clocked at 500MHz. Assume pad driver with OD of $\theta=2.5$ and $V_{DD}=3.5V$

Solution: (assume output changes with 50% of clock transitions)

$$P_{DYN} = \frac{f_{CL}}{2} C_L V_{DD}^2 = 5E8 \cdot 10pF \cdot 3.5^2 = 61mW$$

Note this solution is independent of the OD and the process.
Example: Will the CMOS pad driver actually be able to drive the 10pF load at 500MHz in the previous example in the 0.5u process?

Solution:

\[ t_{CLK} = \frac{1}{500\text{MHz}} = 2\text{nsec} \]

\[ t_{PROP} = n\theta \cdot t_{REF} = 6 \cdot 2.5 \cdot 20\text{psec} = 0.3\text{nsec} \]

Since \( t_{CLK} > t_{PROP} \), this pad driver can drive the 10pF load at 500MHz.

In 0.5u proc \( t_{REF} = 20\text{ps} \), \( C_{REF} = 4\text{fF} \), \( R_{PDREF} = 2.5\text{K} \)
Example: Determine the dynamic power dissipation in the next to the last stage of a 6-stage CMOS pad driver if used to drive a 10pF capacitive load if clocked at 500MHz. Assume pad driver with OD of $\theta=2.5$ and $V_{DD}=3.5V$

Solution:

$$C_{IN} = \theta^5 C_{REF} = 2.5^5 \cdot 4fF = 390fF$$

$$P_{DYN} = f_{CL} C_L V_{DD}^2 = 5E8 \cdot 390fF \cdot 3.5^2 = 2.4mW$$
Example: Is the 6-stage CMOS pad driver adequate to drive the 10pF capacitive load as fast as possible? Assume pad driver with OD of $\theta=2.5$ and $V_{DD}=3.5V$.

Solution:

$$n_{OPT} = \ln \left( \frac{C_L}{C_{REF}} \right) = \ln \left( \frac{10pF}{4fF} \right) = 7.8$$

No – an 8-stage pad driver would drive the load much faster (but is not needed if clocked at only 500MHz).
Example: Determine the power that would be required in the last stage of a CMOS pad driver to drive a 32-bit data bus off-chip if the capacitive load on each line is 2pF. Assume the clock speed is 500MHz and that each bit has an average 50% toggle rate. Assume $V_{DD}=3.5V$

Solution:

$$P_{DYN} = 32 \cdot \frac{f_{CL} C_L V_{DD}^2}{2} = 32 \cdot \frac{5 \times 10^8}{2} \cdot 2pF \cdot 3.5^2 = 196mW$$

Note: A very large amount of power is required to take a large bus off-chip if bus has a high rate of activity.
End of Lecture 43