EE 330
Lecture 43

Digital Circuits

- Other Logic Styles
- Dynamic Logic Circuits
Elmore Delay Calculations

Review from Last Time

\[ t_1 = R(C + C_{REF}) \]
\[ t_2 = 3RC \]
\[ t_3 = 5R\left(C + \frac{1}{2}C_{REF}\right) \]
\[ t_4 = \left[6R // R_L\right]^{25/4}C_{REF} \]
\[ t_5 = t_{REF} \frac{20}{5} \]

\[ t_{PROP} = \sum_{i=1}^{5} t_i \]

\[ R = \frac{1}{6} R_w \frac{L}{W} \]
\[ C = \frac{1}{3} C_D \]
Power Dissipation in Logic Circuits

Types of Power Dissipation

- Static
- Pipe
- Dynamic
- Leakage
  - Gate
  - Diffusion
  - Drain

Review from Last Time
Dynamic Power Dissipation

Energy dissipated with clock signal itself

\[ P_{\text{DYN}} = f_{\text{CL}} V_{\text{DD}}^2 \]

The clock transitions on every clock cycle (i.e. it has a transition duty cycle of 100%)

Clock distribution can cause significant power dissipation

But if a gate has a transition duty cycle of 50% with a clock frequency of \( f_{\text{CL}} \)

\[ P_{\text{DYN}} = \frac{f_{\text{CL}}}{2} C_L V_{\text{DD}}^2 \]
Leakage Power Dissipation

- **Gate**
  - with very thin gate oxides, some gate leakage current flows
  - major concern in 60nm and smaller processes
  - actually a type of static power dissipation

- **Diffusion**
  - Leakage across a reverse-biased pn junction
  - Dependent upon total diffusion area
  - May actually be dominant power loss on longer-channel devices
  - Actually a type of static power dissipation

- **Drain**
  - channel current due to small $V_{GS} - V_T$
  - of significant concern only with low $V_{DD}$ processes
  - actually a type of static power dissipation
Example: Determine the dynamic power dissipation in the last stage of a 6-stage CMOS pad driver if used to drive a 10pF capacitive load if clocked at 500MHz. Assume pad driver with OD of $\theta=2.5$ and $V_{DD}=3.5V$.

Solution: (assume output changes with 50% of clock transitions)

\[ P_{DYN} = \frac{f_{CL}}{2} C_L V_{DD}^2 = 5E8 \cdot 10pF \cdot 3.5^2 = 61mW \]

Note this solution is independent of the OD and the process.
Example: Will the CMOS pad driver actually be able to drive the 10pF load at 500MHz in the previous example in the 0.5u process?

Solution:

\[ t_{CLK} = \frac{1}{500\text{MHz}} = 2\text{nsec} \]

\[ t_{PROP} = 5\theta \cdot t_{REF} + \frac{F_{I_{load}}}{O_{D_{6}}} \cdot t_{REF} \]

\[ F_{I_{load}} = \frac{10\text{pF}}{4\text{fF}} = 2500 \]

\[ OD_{6} = \theta^{5} = 98 \]

\[ \frac{F_{I_{load}}}{OD_{6}} = \frac{2500}{98} \approx 25 \]

\[ t_{prop} = 5 \cdot 2.5 \cdot 20\text{psec} + 25 \cdot 20\text{psec} = (12.5 + 25) \cdot 20\text{psec} = 0.75\text{nsec} \]

since \( t_{CLK} > t_{PROP} \), this pad driver can drive the 10pF load at 500MHz
Example: Determine the dynamic power dissipation in the next to the last stage of a 6-stage CMOS pad driver if used to drive a 10pF capacitive load if clocked at 500MHz. Assume pad driver with OD of $\theta=2.5$ and $V_{DD}=3.5V$

Solution:

$C_{IN}=\theta^5C_{REF}=2.5^5 \cdot 4fF=390fF$

$$P_{DYN}=f_{CL}C_LV_{DD}^2 = 5 \times 10^8 \cdot 390fF \cdot 3.5^2 = 2.4mW$$
Example: Is the 6-stage CMOS pad driver adequate to drive the 10pF capacitive load as fast as possible? Assume pad driver with OD of $\theta=2.5$ and $V_{DD}=3.5\text{V}$

Solution:

$$n_{OPT} = \ln\left(\frac{C_L}{C_{REF}}\right) = \ln\left(\frac{10\text{pF}}{4\text{fF}}\right) = 7.8$$

No – an 8-stage pad driver would drive the load much faster (but is not needed if clocked at only 500MHz)
Example: Determine the power that would be required in the last stage of a CMOS pad driver to drive a 32-bit data bus off-chip if the capacitive load on each line is 2pF. Assume the clock speed is 500MHz and that each bit has an average 50% toggle rate. Assume $V_{DD}=3.5V$

Solution:

\[ P_{DYN} = 32 \cdot \frac{f_{CL} \cdot C_L \cdot V_{DD}^2}{2} = 32 \cdot \frac{5 \times 10^8}{2} \cdot 2pF \cdot 3.5^2 = 196mW \]

Note: A very large amount of power is required to take a large bus off-chip if bus has a high rate of activity.
Digital Circuit Design

- Hierarchical Design
- Basic Logic Gates
- Properties of Logic Families
- Characterization of CMOS Inverter
- Static CMOS Logic Gates
  - Ratio Logic
- Propagation Delay
  - Simple analytical models
    - FI/OD
    - Logical Effort
  - Elmore Delay
- Sizing of Gates

- Propagation Delay with Multiple Levels of Logic
- Optimal driving of Large Capacitive Loads
- Power Dissipation in Logic Circuits
- Other Logic Styles
  - Array Logic
  - Ring Oscillators

- done
- partial
Logic Styles

- Static CMOS
- Complex Logic Gates
- Pass Transistor Logic (PTL)
- Pseudo NMOS
- Dynamic Logic
  - Domino
  - Zipper
Complex Logic Gates

- Implement B in PDN
- Implement B in PUN with complimented input variables
- Zero static power dissipation
- $V_H = V_{DD}$, $V_L = 0V$ (or $V_{SS}$)
- Complimented input variables often required

Have implemented the logical function twice (once in PU, again in PD) and this is a major contributor to increased area and dynamic power dissipation.
Pass Transistor Logic

Observations about PTL

- Low device count implementation of non inverting function (can be dramatic)
- Logic Swing not rail to rail 😞
- Static power dissipation not 0 when F high 😞
- $R_{LG}$ may be unacceptably large 😞
- Slow $t_{LH}$ 😞
- Signal degradation can occur when multiple levels of logic are used 😞
- Widely used in some applications
- Implements basic logic function only once!
Pseudo NMOS Logic

n could be several hundred or even several thousand
Dynamic Logic

- PTL reduced complexity of either PUN or PDN to single “resistor”
- PTL relaxed requirement of all n-channel or all p-channel devices in PUN/PDN

What is the biggest contributor to area? PUN (3X active area for inverter, more for NOR gates, and Well)

What is biggest contributor to dynamic power dissipation? PUN and is responsible for approximately 75% of the dynamic power dissipation in inverter, more in NOR gates!

Can the PUN be eliminated W/O compromising signal levels and power dissipation?
Can the PUN be eliminated W/O compromising signal levels and power dissipation?

Benefits could be most significant!
Consider:

Precharges $F$ to “1” when $\phi$ is low
$F$ either stays high if output is to be high or changes to low on evaluation.
Consider:

- Termed Dynamic Logic Gates
- Parasitic capacitors actually replace $C_D$
- If Logic Block is n-channel, will have rail to rail swings
- Logic Block is simply a PDN that implements $\overline{F}$
Dynamic Logic

Basic Dynamic Logic Gate

Any of the PDNs used in complex logic gates would work here!

- Have eliminate the PUN!
- Ideally will have a factor of 4 or more reduction in $C_{IN}$
- Ideally will have a factor of 4 or more reduction in dynamic power dissipation relative to that of equal rise/fall!
- Ideally will have a factor of 2 reduction in dynamic power dissipation relative to that of minimum size!
Dynamic logic (digital electronics)

From Wikipedia, the free encyclopedia

For the subject in theoretical computer science, see dynamic logic (modal logic).

In integrated circuit design, dynamic logic (or sometimes clocked logic) is a design methodology in combinatory logic circuits, particularly those implemented in MOS technology. It is distinguished from the so-called static logic by exploiting temporary storage of information in stray and gate capacitances.[1] It was popular in the 1970s and has seen a recent resurgence in the design of high speed digital electronics, particularly computer CPUs. Dynamic logic circuits are usually faster than static counterparts, and require less surface area, but are more difficult to design. Dynamic logic has a higher toggle rate than static logic[2] but the capacitative loads being toggled are smaller[3] so the overall power consumption of dynamic logic may be higher or lower depending on various tradeoffs. When referring to a particular logic family, the dynamic adjective usually suffices to distinguish the design methodology, e.g. dynamic CMOS[4] or dynamic SOI design.[2]

Dynamic logic is distinguished from so-called static logic in that dynamics logic uses a clock signal in its implementation of combinational logic circuits. The usual use of a clock signal is to synchronize transitions in sequential logic circuits. For most implementations of combinational logic, a clock signal is not even needed.

The static/dynamic terminology used to refer to combinatorial circuits should not be confused with how the same adjectives are used to distinguish memory devices, e.g. static RAM from dynamic RAM.[5]
Dynamic Logic

Basic Dynamic Logic Gate

Advantages:

- Lower dynamic power dissipation (Ideally 4X)
- Improved speed (ideally 4X)

Limitations:

- Output only valid during evaluate state
- Need to route a clock
  (and this dissipates some power)
- Premature Discharge!
- More complicated
- Charge storage on internal nodes of PDN
- No Static hold if output H
Dynamic Logic

Premature Discharge Problem

If $A$ is high, then $F$ may go low at the start of the evaluate cycle and there is no way to recover a high output later in the evaluate phase - i.e. there may be a boolean error!

Can not reliably cascade dynamic logic gates!
Premature Discharge Problem

This problem occurs when any inputs to an arbitrary dynamic logic gate create an $R_{PD}$ path in the PDN during at the start of the evaluate phase that is not to pull down later in that evaluate phase.

How can this problem be fixed?

Precharging to the low level all inputs to a PDN that may change to the high state later in the evaluate cycle (called domino)

Alternating gates with n-channel and p-channel pull networks (Zipper Logic)
Dynamic Logic

Premature Discharge Problem

Adding an inverter at the output will cause $F$ to precharge low so it can serve as input to subsequent gate w/o causing premature discharge

Implement $F$ instead of $\overline{F}$ in the PDN

Termed **Domino Logic**

Some additional dynamic power dissipation in the inverter

Some additional delay during the evaluate state in inverter
Domino Logic

- A
- PDN
- $V_{DD}$
- F
- $\phi$
- $n$

Diagram of a domino logic circuit with inputs A, PDN, and outputs $V_{DD}$, F, and $\phi$.
Dynamic Logic

- p-channel logic gate will pre-charge low
- Phasing of PUN and PDN networks is reversed
- Some performance loss with p-channel logic devices
- Direct coupling between alternate type dynamic gates is possible without causing a premature discharge problem
Dynamic Logic

Direct coupling between alternate type dynamic gates
Zipper Logic

Map gates to appropriate precharge type
Zipper Logic

Acceptable Implementation in Zipper
Unacceptable Implementation in Zipper
- Premature discharge at output of 2-input NAND
Zipper Logic

Another acceptable Implementation in Zipper
Static Hold Option

If not clocked, charge on upper node of PDN will drain off causing H output to degrade
Static Hold Option

- Weak p will hold charge
- Size may be big (long L)
- Some static power dissipation
- Can use small current source
- Sometimes termed “keeper”

- Weak p will hold charge
- Size may be big (long L)
- Can eliminate static power with domino
- Sometimes termed “keeper”
Charge stored on internal nodes of PDN

If voltage on $C_{P1}$ and $C_{P2}$ was 0V on last evaluation, these may drain charge (charge redistribution) on $C_P$ if output is to evaluate high (e.g. On last evaluation $A_1=A_2=A_3=H$, on next evaluation $A_3=L$, $A_1=A_2=H$.)
Charge stored on internal nodes of PDN

Can precharge internal nodes to eliminate undesired charge redistribution
Dynamic Logic

Many variants of dynamic logic are around

- Domino
- Zipper
- Ratio-less 2-phase
- Ratio-less 4-phase
- Output Prediction Logic
- Fully differential

Benefits disappear, however, when interconnect (and diffusion) capacitances dominate gate capacitances
Future of Dynamic Logic

Dynamic logic will likely disappear in deep sub-micron processes because interconnect parasitics will dominate gate parasitics.
From Wikipedia:

B
BiCMOS

C
CMOS
Cascode Voltage Switch Logic
Clocked logic
Complementary Pass-transistor Logic
Current mode logic
Current steering logic

D
Differential TTL
Diode logic
Diode–transistor logic
Domino logic
Dynamic logic (digital logic)

E
Emitter-coupled logic

F
Four-phase logic

G
Gunning Transceiver Logic

H
HMOS
HVDS
High-voltage differential signaling

I
Integrated injection logic

L
LVDS
Low-voltage differential signaling
Low-voltage positive emitter-coupled logic

M
Multi-threshold CMOS

N
NMOS logic

P
PMOS logic
Philips NORbits
Positive emitter-coupled logic

R
Resistor-transistor logic

S
Static logic (digital logic)

T
Transistor–transistor logic
End of Lecture 43
Digital Building Blocks

• Shift Registers
• Sequential Logic
• Shift Registers (stack)
• Array Logic
• Memory Arrays
Ring Oscillators

- Odd number of stages will oscillate (even will not oscillate)
- Waveform nearly a square wave if \( n \) (number of stages) is large
- Output will slightly imbalance ring and device sizes can be compensated if desired
- Usually use a prime number (e.g. 31)
- Number of stages usually less than 50 (follow by dividers)
- Frequency highly sensitive to process variations and temperature

\[
f_{\text{OSC}} \approx \frac{1}{nt_{\text{PROP}}}
\]

- \( n \) is the number of stages
- \( t_{\text{PROP}} \) is the propagation delay of a single stage (all assumed identical)