EE 330
Lecture 5

Digital Systems – A preview
Quiz 4

Determine $V_H$ and $V_L$ at the C output for the Static CMOS NOR gate shown. Use the switch-level model for the transistors introduced in the last lecture.
And the number is ....
And the number is ....
Quiz 4

Determine $V_H$ and $V_L$ at the C output for the Static CMOS NOR gate shown. Use the switch-level model for the transistors introduced in the last lecture.

Solution:

$V_H = V_{DD}$, $V_L = 0V$
Review from Last Time

MOS Transistor

Qualitative Discussion of n-channel Operation

Source  Gate  Drain

Bulk  

n-channel MOSFET

Source  Drain

Gate  

n-type
n+-type
p-type
p+-type
SiO₂ (insulator)
POLY (conductor)
Review from Last Time

MOS Transistor
Comparison of Operation

D = 1
S = 0

D = 0
S = 1
Logic Circuits

Review from Last Time

Inverter

Truth Table

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
</tr>
</thead>
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<tr>
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</table>
Review from Last Time

Logic Circuits

Truth Table

<table>
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<th>C</th>
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NOR Gate
Logic Circuits

Review from Last Time

Truth Table

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<tr>
<th>A</th>
<th>B</th>
<th>C</th>
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<td>1</td>
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</table>
Review from Last Time

Pull-up and Pull-down Networks

For these circuits, the PUN and PDN satisfy the 3 properties

1. PU network comprised of p-channel device
2. PD network comprised of n-channel device
3. One and only one of these networks is conducting at the same time

\[ V_H = V_{DD} \quad V_L = 0 \quad (\text{too good to be true?}) \]

\[ P_H = P_L = 0 \quad (\text{too good to be true?}) \]

\[ t_{HL} = t_{LH} = 0 \quad (\text{too good to be true?}) \]

These characteristics are inherent in Boolean circuits with these 3 properties
Example 1:
How many transistors are required to realize the function

\[ F = \overline{A \cdot B} + \overline{A \cdot C} \]

in a basic CMOS process if static NAND and NOR gates are used? Assume A, B and C are available.

**Solution:**

20 transistors and 5 levels of logic
Example: XOR Function

\[ Y = A \oplus B \]

A widely-used 2-input Gate

Static CMOS implementation

\[ Y = A \overline{B} + \overline{A}B \]

22 transistors  5 levels of logic

Delays unacceptable and device count is too large!
Example

\[ Y = (A \cdot B) + (C \cdot D) \]

Standard Static CMOS Implementation

3 levels of Logic

16 Transistors if Basic CMOS Gates are Used
Observe:

\[ Y = (A \cdot B) + (C \cdot D) \]

Significant reduction in transistor count and levels of logic for realizing same Boolean function

Termed a “Complex Logic Gate” implementation
Complex Logic Gates

\[ Y = \overline{(A \cdot B)} + (C \cdot D) \]
Complex Gates

Pull up and pull down network never both conducting

One of the two networks is always conducting
Complex Gates

Nomenclature:

When the logic gate shown is not a multiple-input NAND or NOR gate but satisfies Properties 1, 2, and 3 above, the gate will be referred to as a Complex Logic Gate.

Complex Logic Gates also implement static logic functions and some authors would refer to this as Static CMOS Logic as well but we will make the distinction and refer to this as “Complex Logic Gates”
Complex Gates

Complex Gate Design Strategy:

1. Implement $\overline{Y}$ in the PDN

2. Implement $Y$ in the PUN (must complement the input variables since p-channel devices are used)
XOR in Complex Logic Gates

A \rightarrow Y
B

Y = A \oplus B
XOR in Complex Logic Gates

\[ Y = A \oplus B \]

\[ Y = AB + \overline{AB} \]

\[ \overline{Y} = (AB + \overline{AB}) \]

\[ \overline{Y} = AB \cdot \overline{AB} \]

\[ Y = (\overline{A} + B) \cdot (A + B) \]
XOR in Complex Logic Gates

\[ Y = A \overline{B} + \overline{A}B \]

\[ \overline{Y} = (\overline{A}+B) \cdot (A+\overline{B}) \]
XOR in Complex Logic Gates

\[ Y = \overline{AB} + \overline{A}B \]

\[ \overline{Y} = (\overline{A} + B) \cdot (A + \overline{B}) \]

12 transistors and 2 levels of logic

Notice a significant reduction in the number of transistors required
XOR in Complex Logic Gates

\[ Y = A \overline{B} + \overline{A}B \]

\[ \overline{Y} = (A + \overline{B}) \cdot (A + \overline{B}) \]

\[ \overline{Y} = (A \cdot (A + \overline{B})) + (B \cdot (A + \overline{B})) \]

\[ = (A \cdot B) + (A \cdot B) \]

Multiple PU and PD networks can be used.
Complex Logic Gate Summary:

1. PU network comprised of p-channel device
2. PD network comprised of n-channel device
3. One and only one of these networks is conducting at the same time

If PUN and PDN satisfy the properties:

1. PU network comprised of p-channel device
2. PD network comprised of n-channel device
3. One and only one of these networks is conducting at the same time

Characteristics of PU/PD logic of this type:

- Rail to rail logic swings
- Zero static power dissipation in both Y=1 and Y=0 states
- Arbitrarily fast (too good to be true? will consider again with better model)
Consider \[ Y = A \cdot B \]

Standard CMOS Implementation

2 levels of Logic

6 Transistors if Basic CMOS Gates are Used

Basic noninverting functions generally require more complexity if basic CMOS gates are used for implementation
Pass Transistor Logic

\[ Y = A \cdot B \]

Requires only 2 transistors rather than 6 for a standard CMOS gate (and a resistor).
Pass Transistor Logic

\[ Y = A \cdot B \]

Even simpler pass transistor logic implementations are possible.

Requires only 1 transistor (and a resistor).
Pass Transistor Logic

Requires only 1 transistor (and a resistor)

- Pass transistor logic can offer significant reductions in complexity for some functions (particularly noninverting)
- Resistor may require more area than several hundred or even several thousand transistors
- Signal levels may not go to $V_{DD}$ or to $0\,\text{V}$
- Static power dissipation may not be zero
- Signals may degrade unacceptably if multiple gates are cascaded
- “resistor” often implemented with a transistor to reduce area but signal swing and power dissipation problems still persist
- Pass transistor logic is widely used
Logic Design Styles

• Several different logic design styles are often used throughout a given design (3 considered thus far)
  – Static CMOS
  – Complex Logic Gates
  – Pass Transistor Logic

• The designer has complete control over what is placed on silicon and governed only by cost and performance

• New logic design strategies have been proposed recently and others will likely emerge in the future

• The digital designer needs to be familiar with the benefits and limitations of varying logic styles to come up with a good solution for given system requirements
MOSFET Modeling

- Simple model of MOSFET was developed
- Simple gates designed in CMOS Process were introduced
  - Some have zero power dissipation
  - Some have or appeared to have rail to rail logic voltage swings
  - All appeared to be Infinitely fast
  - Logic levels of some can not be predicted with simple model
  - Simple model is not sufficiently accurate to provide insight relating to some of these properties

- MOSFET modeling strategy
  - hierarchical model structure will be developed
  - generally use simplest model that can be justified
MOS Transistor Models

1. Switch-Level model

Advantages:
Simple, does not require understanding of semiconductor properties, does not depend upon process, adequate for understanding basic operation of many digital circuits

Limitations:
Does not provide timing information (surfaced when looking at static CMOS circuits, and several others that have not yet become apparent from the applications that have been considered) and can not support design of “resistor” used in Pass Transistor Logic
Recall

MOS Transistor
Qualitative Discussion of n-channel Operation
Recall

MOS Transistor
Qualitative Discussion of n-channel Operation

For $V_{GS}$ small

For $V_{GS}$ large
MOS Transistor
Qualitative Discussion of n-channel Operation

For $V_{GS}$ small

For $V_{GS}$ large
Improved Switch-Level Model

Switch-level model including gate capacitance and drain resistance

Switch closed for $V_{GS} = \text{“1”}$

Still neglect bulk connection and connect the bulk capacitance to the source
Improved Switch-Level Model

Switch-level model including gate capacitance and drain resistance

Switch closed for $V_{GS} = \text{"1"}$
Improved Switch-Level Model

Switch-level model including gate capacitance and drain resistance

Switch closed for $V_{GS} = 0$

Switch-level model including gate capacitance and drain resistance
Improved Switch-Level Model

Switch-level model including gate capacitance and drain resistance

$C_{GS}$ and $R_{SW}$ dependent upon device sizes and process

For minimum-sized devices in a 0.5μ process

$C_{GS} \approx 1.5fF \quad R_{SW} \approx \begin{cases} 2K\Omega & \text{n–channel} \\ 6K\Omega & \text{p–channel} \end{cases}$

Considerable emphasis will be placed upon device sizing to manage $C_{GS}$ and $R_{SW}$
Is a capacitor of 1.5fF small enough to be neglected?
Is a capacitor of 1.5fF small enough to be neglected?
Model Summary

1, Switch-Level model

Switch closed for $V_{GS} = \text{large}$

Switch open for $V_{GS} = \text{small}$

2, Improves switch-level model

Other models will be developed later
Example

What are $t_{HL}$ and $t_{LH}$?

With switch level model
Example (cont)

With improved model

Inverter
Example (cont)

With improved model

$t_{HL} = ?$

Inverter
Example (cont)

With improved model

\[ t_{HL} = ? \]

Recognize as a first-order RC network

Recall: Step response of any first-order network with LHP pole can be written as

\[ y(t) = F + (I - F)e^{-\frac{t}{\tau}} \]

where \( F \) is the final value, \( I \) is the initial value and \( \tau \) is the time constant of the circuit

For the circuit above, \( F=0, I=5 \) and \( \tau = R_{SWn} C_L \)
Example (cont)

With improved model

\[
V_{OUT}(t) = F + (1 - F)e^{-\frac{t}{\tau}}
\]

\[
\tau = R_{SWn} C_L
\]
Example (cont)

With improved model

\[ t_{HL} = \]?

\[ I = 5V, \quad F = 0V \]

\[ \tau = R_{SWn} C_L \]

\[ V_{OUT}(t) = F + (1 - F) e^{-\frac{t}{\tau}} \]

\[ \frac{I}{e} = F + (1 - F) e^{-\frac{t_{HL}}{\tau}} \]

\( t_{HL} \) as defined has proved useful at analytically predicting response time of circuits.
Example (cont)

With improved model

\[ I = F + (I - F)e^{-\frac{t_{HL}}{\tau}} \]

\[ I = 0 + (I - 0)e^{-\frac{t_{HL}}{\tau}} \]

\[ 1 = e^{-\frac{t_{HL}}{\tau}} \]

\[ t_{HL} = \tau \]

\[ t_{HL} = R_{SWn}C_L \]

\[ I = 5V, \ F = 0V \]

\[ \tau = R_{SWn}C_L \]
Example (cont)

With improved model \[ t_{LH} = ? \]

\[
y(t) = F + (1 - F) e^{-\frac{t}{\tau}}
\]

For this circuit, \( F = 5 \), \( I = 0 \) and \( \tau = R_{SWP} C_L \)
Example (cont)

With improved model

$t_{LH} = ?$

$t_{HL}$ as defined has proved useful at analytically predicting response time of circuits

\[
V_{\text{OUT}}(t) = F + (1 - F) e^{-\frac{t}{\tau}}
\]

\[
F \left( 1 - \frac{1}{e} \right) = F + (1 - F) e^{-\frac{t_{LH}}{\tau}}
\]
Example (cont)

With improved model

\[ V_{\text{OUT}}(t) = F + (1 - F)e^{-\frac{t}{\tau}} \]

\[ \tau = R_{\text{SWp}} C_L \]
Example (cont)

With improved model

\[ t_{LH} = ? \]

\[
F \left( 1 - \frac{1}{e} \right) = F + (1 - F) e^{-\frac{t_{LH}}{\tau}}
\]

\[
F \left( 1 - \frac{1}{e} \right) = F + (F) e^{-\frac{t_{LH}}{\tau}}
\]

\[
1 - \frac{1}{e} = 1 + e^{-\frac{t_{LH}}{\tau}}
\]

\[ t_{LH} = \tau \]

\[ t_{LH} = R_{SWp} C_L \]
Example (cont)

With improved model

\[
\begin{align*}
  t_{\text{HL}} & \approx R_{\text{SWn}} C_L \\
  t_{\text{LH}} & \approx R_{\text{SWp}} C_L
\end{align*}
\]

\[
2K \cdot 1pF = 2n \text{sec}
\]

\[
6K \cdot 1pF = 6n \text{sec}
\]

Note this circuit is quite fast!

Note that \( t_{\text{HL}} \) is much shorter than \( t_{\text{LH}} \)

Often \( C_L \) will be even smaller and the circuit will be much faster!!
End of Lecture 5
One gate often drives one or more other gates!

What are $t_{HL}$ and $t_{LH}$?
Example: What is the delay of a minimum-sized inverter driving another identical device?

Loading effects same whether $C_{GSp}$ connected to $V_{DD}$ or GND
Example: What is the delay of a minimum-sized inverter driving another identical device?
Example: What is the delay of a minimum-sized inverter driving another identical device?

\[ t_{HL} \approx R_{SWn} C_L = 2K \cdot 3fF = 6p\text{sec} \]

\[ t_{LH} \approx R_{SWp} C_L = 6K \cdot 1pF = 18p\text{sec} \]

Note this is very fast but even the small 1.5fF capacitors are not negligible!
Stick Diagrams

• It is often necessary to obtain information about placement, interconnect and physical-layer structure
• Stick diagrams are often used for small component-count blocks
• Approximate placement, routing, and area information can be obtained rather quickly with the use of stick diagrams
Stick Diagrams

Metal 1
poly
n-diffusion
p-diffusion
Metal 2
Contact

Additional layers can be added and color conventions are personal
A stick diagram is not a layout but gives the basic structure that will be instantiated in the actual layout itself.

Modifications can be made much more quickly on a stick diagram than on a layout.

Iteration may be needed to come up with a good layout structure.
Stick Diagram

Alternate Representation
Technology Files

• Provide Information About Process
  – Process Flow (Fabrication Technology)
  – Model Parameters
  – Design Rules

• Serve as Interface Between Design Engineer and Process Engineer

• Insist on getting information that is deemed important for a design
  – Limited information available in academia
  – Foundries often sensitive to who gets access to information
  – Customer success and satisfaction is critical to foundries
Technology Files

• Design Rules

• Process Flow (Fabrication Technology) (will discuss next)

• Model Parameters (will discuss in substantially more detail after device operation and more advanced models are introduced)
**TABLE 2B.2**  
Design rules for a typical p-well CMOS process  
(See Table 2B.3 in color plates for graphical interpretation)

<table>
<thead>
<tr>
<th>Dimensions</th>
<th>Microns</th>
<th>Scalable</th>
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</thead>
<tbody>
<tr>
<td>1. p-well (CIF Brown, Mask #1a)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.1 Width</td>
<td>5</td>
<td>4(\lambda)</td>
</tr>
<tr>
<td>1.2 Spacing (different potential)</td>
<td>15</td>
<td>10(\lambda)</td>
</tr>
<tr>
<td>1.3 Spacing (same potential)</td>
<td>9</td>
<td>6(\lambda)</td>
</tr>
<tr>
<td>2. Active (CIF Green, Mask #2)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2.1 Width</td>
<td>4</td>
<td>2(\lambda)</td>
</tr>
<tr>
<td>2.2 Spacing</td>
<td>4</td>
<td>2(\lambda)</td>
</tr>
<tr>
<td>2.3 p(^+) active in n-sub to p-well edge</td>
<td>8</td>
<td>6(\lambda)</td>
</tr>
<tr>
<td>2.4 n(^+) active in n-sub to p-well edge</td>
<td>7</td>
<td>5(\lambda)</td>
</tr>
<tr>
<td>2.5 n(^+) active in p-well to p-well edge</td>
<td>4</td>
<td>2(\lambda)</td>
</tr>
<tr>
<td>2.6 p(^+) active in p-well to p-well edge</td>
<td>1</td>
<td>(\lambda)</td>
</tr>
<tr>
<td>3. Poly (POLY I) (CIF Red, Mask #3)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3.1 Width</td>
<td>3</td>
<td>2(\lambda)</td>
</tr>
<tr>
<td>3.2 Spacing</td>
<td>3</td>
<td>2(\lambda)</td>
</tr>
<tr>
<td>3.3 Field poly to active</td>
<td>2</td>
<td>(\lambda)</td>
</tr>
<tr>
<td>3.4 Poly overlap of active</td>
<td>3</td>
<td>2(\lambda)</td>
</tr>
<tr>
<td>3.5 Active overlap of poly</td>
<td>4</td>
<td>2(\lambda)</td>
</tr>
<tr>
<td>4. p(^+) select (CIF Orange, Mask #4)</td>
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</tr>
<tr>
<td>4.1 Overlap of active</td>
<td>2</td>
<td>(\lambda)</td>
</tr>
<tr>
<td>4.2 Space to n(^+) active</td>
<td>2</td>
<td>(\lambda)</td>
</tr>
<tr>
<td>4.3 Overlap of channel(^b)</td>
<td>3.5</td>
<td>2(\lambda)</td>
</tr>
<tr>
<td>4.4 Space to channel(^b)</td>
<td>3.5</td>
<td>2(\lambda)</td>
</tr>
<tr>
<td>4.5 Space to p(^+) select</td>
<td>3</td>
<td>2(\lambda)</td>
</tr>
<tr>
<td>4.6 Width</td>
<td>3</td>
<td>2(\lambda)</td>
</tr>
</tbody>
</table>
Typical Design Rules (cont)

5. Contact\textsuperscript{c} (CIF Purple, Mask #6)
   
   5.1 Square contact, exactly \hspace{2cm} 3 \times 3 \hspace{1cm} 2\lambda \times 2\lambda
   5.2 Rectangular contact, exactly \hspace{2cm} 3 \times 8 \hspace{1cm} 2\lambda \times 6\lambda
   5.3 Space to different contact \hspace{2cm} 3 \hspace{1cm} 2\lambda
   5.4 Poly overlap of contact \hspace{2cm} 2 \hspace{1cm} \lambda
   5.5 Poly overlap in direction of metal 1 \hspace{2cm} 2.5 \hspace{1cm} 2\lambda
   5.6 Space to channel \hspace{2cm} 3 \hspace{1cm} 2\lambda
   5.7 Metal 1 overlap of contact \hspace{2cm} 2 \hspace{1cm} \lambda
   5.8 Active overlap of contact \hspace{2cm} 2 \hspace{1cm} \lambda
   5.9 \text{p}^+ \text{ select overlap of contact} \hspace{2cm} 3 \hspace{1cm} 2\lambda
   5.10 Subs./well shorting contact, exactly \hspace{2cm} 3 \times 8 \hspace{1cm} 2\lambda \times 6\lambda

6. Metal 1\textsuperscript{d} (CIF Blue, Mask #7)
   
   6.1 Width \hspace{2cm} 3 \hspace{1cm} 2\lambda
   6.2 Spacing \hspace{2cm} 4 \hspace{1cm} 3\lambda
   6.3 Maximum current density \hspace{2cm} 0.8 \text{mA}/\mu \hspace{1cm} 0.8 \text{mA}/\mu
**Typical Design Rules (cont)**

<table>
<thead>
<tr>
<th>Rule</th>
<th>Description</th>
<th>Width</th>
<th>Spacing</th>
<th>Bonding pad size</th>
<th>Probe pad size</th>
<th>Bonding pad separation</th>
<th>Bonding to probe pad</th>
<th>Probe pad separation</th>
<th>Pad to circuitry</th>
<th>Maximum current density</th>
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</thead>
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<tr>
<td>7.1</td>
<td>Size, exactly</td>
<td>3 x 3</td>
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<td>2λ x 2λ</td>
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<td></td>
</tr>
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<td>Separation</td>
<td>3</td>
<td></td>
<td>2λ</td>
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<td>Space to poly edge</td>
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<td>Space to contact</td>
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<td></td>
<td>2λ</td>
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<td>Overlap by metal 1</td>
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<td></td>
<td>λ</td>
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<td></td>
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<td></td>
<td></td>
</tr>
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<td></td>
<td>λ</td>
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</tr>
<tr>
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<td>Width</td>
<td>5</td>
<td></td>
<td>3λ</td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8.2</td>
<td>Spacing</td>
<td>5</td>
<td></td>
<td>3λ</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8.3</td>
<td>Bonding pad size</td>
<td>100 x 100</td>
<td>100 μ x 100 μ</td>
<td></td>
<td>75 x 75</td>
<td>75 μ x 75 μ</td>
<td></td>
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<td></td>
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</tr>
<tr>
<td>8.4</td>
<td>Probe pad size</td>
<td>75 x 75</td>
<td></td>
<td>75 μ x 75 μ</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>8.5</td>
<td>Bonding pad separation</td>
<td>50</td>
<td></td>
<td>50 μ</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8.6</td>
<td>Bonding to probe pad</td>
<td>30</td>
<td></td>
<td>30 μ</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>8.7</td>
<td>Probe pad separation</td>
<td>30</td>
<td></td>
<td>30 μ</td>
<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>8.8</td>
<td>Pad to circuitry</td>
<td>40</td>
<td></td>
<td>40 μ</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>8.9</td>
<td>Maximum current density</td>
<td>0.8 mA/μ</td>
<td>0.8 mA/μ</td>
<td></td>
<td></td>
<td></td>
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<td></td>
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<tr>
<td>9.1</td>
<td>Bonding pad opening</td>
<td>90 x 90</td>
<td>90 μ x 90 μ</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>9.2</td>
<td>Probe pad opening</td>
<td>65 x 65</td>
<td></td>
<td>65 μ x 65 μ</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
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<tr>
<td>10.1</td>
<td>Metal 1 to poly edge spacing when crossing metal 2</td>
<td>2</td>
<td></td>
<td>λ</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>10.2</td>
<td>Rule domain</td>
<td>2</td>
<td></td>
<td>λ</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>11.1</td>
<td>Width</td>
<td>3</td>
<td></td>
<td>2λ</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>11.2</td>
<td>Spacing</td>
<td>3</td>
<td></td>
<td>2λ</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>11.3</td>
<td>POLY I overlap of POLY II</td>
<td>2</td>
<td></td>
<td>λ</td>
<td>3</td>
<td>2λ</td>
<td>3</td>
<td>2λ</td>
<td>3</td>
<td>2λ</td>
</tr>
</tbody>
</table>
Typical Process Description

Process scenario of major process steps in typical p-well CMOS process

1. Clean wafer
2. GROW THIN OXIDE
3. Apply photoresist
4. PATTERN P-WELL
5. Develop photoresist
6. Deposit and diffuse p-type impurities
7. Strip photoresist
8. Strip thin oxide
9. Grow thin oxide
10. Apply layer of Si₃N₄
11. Apply photoresist
12. PATTERN Si₃N₄ (active area definition)
13. Develop photoresist
14. Etch Si₃N₄
15. Strip photoresist
   *Optional field threshold voltage adjust*
   A.1 Apply photoresist
   A.2 PATTERN ANTIMOAT IN SUBSTRATE
   A.3 Develop photoresist
   A.4 FIELD IMPLANT (n-type)
   A.5 Strip photoresist
16. GROW FIELD OXIDE
17. Strip Si₃N₄
18. Strip thin oxide
19. GROW GATE OXIDE
20. POLYSILICON DEPOSITION (POLY I)
21. Apply photoresist
22. PATTERN POLYSILICON
23. Develop photoresist
24. ETCH POLYSILICON
### Typical Process Description (cont)

<table>
<thead>
<tr>
<th>Step</th>
<th>Description</th>
</tr>
</thead>
</table>
| 25.  | Strip photoresist  
      | *Optional steps for double polysilicon process*  
      | B.1 Strip thin oxide  
      | B.2 GROW THIN OXIDE  
      | B.3 POLYSILICON DEPOSITION (POLY II)  
      | B.4 Apply photoresist  
      | B.5 PATTERN POLYSILICON (MASK #B1)  
      | B.6 Develop photoresist  
      | B.7 ETCH POLYSILICON  
      | B.8 Strip photoresist  
      | B.9 Strip thin oxide |
| 26.  | Apply photoresist |
| 27.  | PATTERN P-CHANNEL DRAINS AND SOURCES AND  
      | P+ GUARD RINGS (p-well ohmic contacts) (MASK #4)  
| 28.  | Develop photoresist |
| 29.  | p+ IMPLANT |
| 30.  | Strip photoresist |
| 31.  | Apply photoresist |
| 32.  | PATTERN N-CHANNEL DRAINS AND SOURCES AND  
      | N+ GUARD RINGS (top ohmic contact to substrate) (MASK #5) |
| 33.  | Develop photoresist |
| 34.  | n+ IMPLANT |
| 35.  | Strip photoresist |
| 36.  | Strip thin oxide |
| 37.  | Grow oxide |
| 38.  | Apply photoresist |
| 39.  | PATTERN CONTACT OPENINGS (MASK #6) |
| 40.  | Develop photoresist |
| 41.  | Etch oxide |
| 42.  | Strip photoresist |
| 43.  | APPLY METAL |
| 44.  | Apply photoresist |
| 45.  | PATTERN METAL (MASK #7) |
| 46.  | Develop photoresist |
| 47.  | Etch metal |
Typical Process Description (cont)

48. Strip photoresist
   *Optional steps for double metal process*
   C.1 Strip thin oxide
   C.2 DEPOSIT INTERMETAL OXIDE
   C.3 Apply photoresist
   C.4 PATTERN VIAS
   C.5 Develop photoresist
   C.6 Etch oxide
   C.7 Strip photoresist
   C.8 APPLY METAL (Metal 2)
   C.9 Apply photoresist
   C.10 PATTERN METAL
   C.11 Develop photoresist
   C.12 Etch metal
   C.13 Strip photoresist

49. APPLY PASSIVATION
50. Apply photoresist
51. PATTERN PAD OPENINGS
52. Develop photoresist
53. Etch passivation
54. Strip photoresist
55. ASSEMBLE, PACKAGE AND TEST
### Typical Model Parameters

#### Process parameters for a typical p-well CMOS process

<table>
<thead>
<tr>
<th>Square law model parameters</th>
<th>Typical</th>
<th>Tolerance</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{T0}$ (threshold voltage)</td>
<td>0.75</td>
<td>± 0.25</td>
<td>V</td>
</tr>
<tr>
<td>n-channel ($V_{TNO}$)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>p-channel ($V_{TP0}$)</td>
<td>−0.75</td>
<td>± 0.25</td>
<td>V</td>
</tr>
<tr>
<td>$K'$ (conduction factor)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>n-channel</td>
<td>24</td>
<td>± 6</td>
<td>$\mu$A/V^2</td>
</tr>
<tr>
<td>p-channel</td>
<td>8</td>
<td>± 1.5</td>
<td>$\mu$A/V^2</td>
</tr>
<tr>
<td>$\gamma$ (body effect)</td>
<td>0.8</td>
<td>± 0.4</td>
<td>$V^{1/2}$</td>
</tr>
<tr>
<td>n-channel</td>
<td>0.4</td>
<td>± 0.2</td>
<td>$V^{1/2}$</td>
</tr>
<tr>
<td>p-channel</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\lambda$ (channel length modulation)</td>
<td>0.01</td>
<td>± 50%</td>
<td>$V^{-1}$</td>
</tr>
<tr>
<td>n-channel</td>
<td>0.02</td>
<td>± 50%</td>
<td>$V^{-1}$</td>
</tr>
<tr>
<td>p-channel</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\phi$ (surface potential)</td>
<td>0.6</td>
<td>± 0.1</td>
<td>V</td>
</tr>
<tr>
<td>n- and p-channel</td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

#### Process parameters

<table>
<thead>
<tr>
<th>$\mu$ (channel mobility)</th>
<th>Typical</th>
<th>Tolerance</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>n-channel</td>
<td>710</td>
<td></td>
<td>cm^2/(V · s)</td>
</tr>
<tr>
<td>p-channel</td>
<td>230</td>
<td></td>
<td>cm^2/(V · s)</td>
</tr>
</tbody>
</table>

#### Doping

<table>
<thead>
<tr>
<th>Doping</th>
<th>Typical</th>
<th>Tolerance</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>n^+ active</td>
<td>5</td>
<td>±4</td>
<td>$10^{18}$/cm^3</td>
</tr>
<tr>
<td>p^+ active</td>
<td>5</td>
<td>±4</td>
<td>$10^{17}$/cm^3</td>
</tr>
<tr>
<td>p-well</td>
<td>5</td>
<td>±2</td>
<td>$10^{16}$/cm^3</td>
</tr>
<tr>
<td>n-substrate</td>
<td>1</td>
<td>±0.1</td>
<td>$10^{16}$/cm^3</td>
</tr>
</tbody>
</table>
Typical Model Parameters (cont)

<table>
<thead>
<tr>
<th>Physical feature sizes</th>
<th></th>
<th>±</th>
<th>Å</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>$T_{OX}$ (gate oxide thickness)</strong></td>
<td>500</td>
<td>100</td>
<td></td>
</tr>
<tr>
<td>Total lateral diffusion</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>n-channel</td>
<td>0.45</td>
<td>0.15</td>
<td>μ</td>
</tr>
<tr>
<td>p-channel</td>
<td>0.6</td>
<td>0.3</td>
<td>μ</td>
</tr>
<tr>
<td>Diffusion depth</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$n^+$ diffusion</td>
<td>0.45</td>
<td>0.15</td>
<td>μ</td>
</tr>
<tr>
<td>$p^+$ diffusion</td>
<td>0.6</td>
<td>0.3</td>
<td>μ</td>
</tr>
<tr>
<td>p-well</td>
<td>3.0</td>
<td>30%</td>
<td>μ</td>
</tr>
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</table>

<table>
<thead>
<tr>
<th>Insulating layer separation</th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>POLY I to POLY II</td>
<td>800</td>
<td>100</td>
<td>Å</td>
</tr>
<tr>
<td>Metal 1 to Substrate</td>
<td>1.55</td>
<td>0.15</td>
<td>μ</td>
</tr>
<tr>
<td>Metal 1 to Diffusion</td>
<td>0.925</td>
<td>0.25</td>
<td>μ</td>
</tr>
<tr>
<td>POLY I to Substrate (POLY I on field oxide)</td>
<td>0.75</td>
<td>0.1</td>
<td>μ</td>
</tr>
<tr>
<td>Metal 1 to POLY I</td>
<td>0.87</td>
<td>0.7</td>
<td>μ</td>
</tr>
<tr>
<td>Metal 2 to Substrate</td>
<td>2.7</td>
<td>0.25</td>
<td>μ</td>
</tr>
<tr>
<td>Metal 2 to Metal I</td>
<td>1.2</td>
<td>0.1</td>
<td>μ</td>
</tr>
<tr>
<td>Metal 2 to POLY I</td>
<td>2.0</td>
<td>0.07</td>
<td>μ</td>
</tr>
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</table>
### Capacitances

<table>
<thead>
<tr>
<th>Capacitance</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{OX}$ (gate oxide capacitance, n- and p-channel)</td>
<td>0.7</td>
<td>fF/μm$^2$</td>
</tr>
<tr>
<td>POLY I to substrate, poly in field</td>
<td>0.045</td>
<td>fF/μm$^2$</td>
</tr>
<tr>
<td>POLY II to substrate, poly in field</td>
<td>0.045</td>
<td>fF/μm$^2$</td>
</tr>
<tr>
<td>Metal 1 to substrate, metal in field</td>
<td>0.025</td>
<td>fF/μm$^2$</td>
</tr>
<tr>
<td>Metal 2 to substrate, metal in field</td>
<td>0.014</td>
<td>fF/μm$^2$</td>
</tr>
<tr>
<td>POLY I to POLY II</td>
<td>0.44</td>
<td>fF/μm$^2$</td>
</tr>
<tr>
<td>POLY I to Metal 1</td>
<td>0.04</td>
<td>fF/μm$^2$</td>
</tr>
<tr>
<td>POLY I to Metal 2</td>
<td>0.039</td>
<td>fF/μm$^2$</td>
</tr>
<tr>
<td>Metal 1 to Metal 2</td>
<td>0.035</td>
<td>fF/μm$^2$</td>
</tr>
<tr>
<td>Metal 1 to diffusion</td>
<td>0.04</td>
<td>fF/μm$^2$</td>
</tr>
<tr>
<td>Metal 2 to diffusion</td>
<td>0.02</td>
<td>fF/μm$^2$</td>
</tr>
<tr>
<td>n$^+$ diffusion to p-well (junction, bottom)</td>
<td>0.33</td>
<td>fF/μm$^2$</td>
</tr>
<tr>
<td>n$^+$ diffusion sidewall (junction, sidewall)</td>
<td>2.6</td>
<td>fF/μm</td>
</tr>
<tr>
<td>p$^+$ diffusion to substrate (junction, bottom)</td>
<td>0.38</td>
<td>fF/μm$^2$</td>
</tr>
<tr>
<td>p$^+$ diffusion sidewall (junction, sidewall)</td>
<td>3.5</td>
<td>fF/μm</td>
</tr>
<tr>
<td>p-well to substrate (junction, bottom)</td>
<td>0.2</td>
<td>fF/μm$^2$</td>
</tr>
<tr>
<td>p-well sidewall (junction, sidewall)</td>
<td>1.6</td>
<td>fF/μm</td>
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</table>

### Resistances

<table>
<thead>
<tr>
<th>Resistance</th>
<th>Value</th>
<th>Unit</th>
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<tr>
<td>Substrate</td>
<td>25</td>
<td>Ω-cm</td>
</tr>
<tr>
<td>p-well</td>
<td>5000</td>
<td>Ω</td>
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<tr>
<td>n$^+$ diffusion</td>
<td>35</td>
<td>Ω</td>
</tr>
<tr>
<td>p$^+$ diffusion</td>
<td>80</td>
<td>Ω</td>
</tr>
<tr>
<td>Metal</td>
<td>0.003</td>
<td>Ω</td>
</tr>
<tr>
<td>Poly</td>
<td>25</td>
<td>Ω</td>
</tr>
<tr>
<td>Metal 1–Metal 2 via (3 μ × 3 μ contact)</td>
<td>&lt;0.1</td>
<td>Ω</td>
</tr>
<tr>
<td>Metal 1 contact to POLY I (3 μ × 3 μ contact)</td>
<td>&lt;10</td>
<td>Ω</td>
</tr>
<tr>
<td>Metal 1 contact to n$^+$ or p$^+$ diffusion (3 μ × 3 μ contact)</td>
<td>&lt;5</td>
<td>Ω</td>
</tr>
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</table>
Typical Model Parameters (cont)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Punchthrough voltages (Gate oxide, POLY I to POLY II)</td>
<td>&gt;10 V</td>
</tr>
<tr>
<td>Diffusion reverse breakdown voltage</td>
<td>&gt;10 V</td>
</tr>
<tr>
<td>p-well to substrate reverse breakdown voltage</td>
<td>&gt;20 V</td>
</tr>
<tr>
<td>Metal 1 in field threshold voltage</td>
<td>&gt;10 V</td>
</tr>
<tr>
<td>Metal 2 in field threshold voltage</td>
<td>&gt;10 V</td>
</tr>
<tr>
<td>Poly-field threshold voltage</td>
<td>&gt;10 V</td>
</tr>
<tr>
<td>Maximum operating voltage</td>
<td>7.0 V</td>
</tr>
<tr>
<td>n⁺ diffusion to p-well leakage current</td>
<td>0.25 fA/μ²</td>
</tr>
<tr>
<td>p⁺ diffusion to substrate leakage current</td>
<td>0.25 fA/μ²</td>
</tr>
<tr>
<td>p-well leakage current</td>
<td>0.25 fA/μ²</td>
</tr>
<tr>
<td>Maximum metal current density</td>
<td>0.8 mA/μ width</td>
</tr>
<tr>
<td>Maximum device operating temperature</td>
<td>200 °C</td>
</tr>
<tr>
<td>Parameter (Level 2 model)</td>
<td>n-channel</td>
</tr>
<tr>
<td>--------------------------</td>
<td>-----------</td>
</tr>
<tr>
<td>VTO</td>
<td>0.827</td>
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<tr>
<td>KP</td>
<td>32.87</td>
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<tr>
<td>GAMMA</td>
<td>1.36</td>
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<tr>
<td>PHI</td>
<td>0.6</td>
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<tr>
<td>LAMBDA</td>
<td>1.605E−2</td>
</tr>
<tr>
<td>CGSO</td>
<td>5.2E−4</td>
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<tr>
<td>CGDO</td>
<td>5.2E−4</td>
</tr>
<tr>
<td>RSH</td>
<td>25</td>
</tr>
<tr>
<td>CJ</td>
<td>3.2E−4</td>
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<tr>
<td>MJ</td>
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<tr>
<td>CJSW</td>
<td>9.0E−4</td>
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<tr>
<td>MJSW</td>
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<td>TOX</td>
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<td>NSUB</td>
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<td>NSS</td>
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<td>NFS</td>
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<td>TPG</td>
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<td>XJ</td>
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<td>LD</td>
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<td>UO</td>
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<td>UEXP</td>
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<td>VMAX</td>
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<tr>
<td>DELTA</td>
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</table>
Typical Model Parameters (cont)

```
.MOS M = CMOSN NMOS (LEVEL = 49
+VERSION = 3.1
+NAME = CMOSN NMOS
+XJ = 1.0E+7
+NCH = 1.7E17
+K1 = 0.875093
+K2 = -0.0543223
+K3B = -3.615287E-3
+KETA = -3.615287E-3
+RDSW = 1.380341E3
+WINT = 2.594349E-7
+XL = 1E-7
+DWB = 3.537786E-8
+MOS = 0
+CDSC = 0
+CDSCB = 0
+DSUB = 0.076309
+PDIBLC2 = 2.23242E-3
+PSCBE1 = 6.619472E8
+DELTA = 0.01
+PR = 0
+KT1L = 0
+UB1 = -7.61E-18
+WLN = 0
+LWN = 1
+LNL = 1
+LWL = 0
+CGDO = 2.34E-10
+CGSO = 2.34E-10
+CJ = 4.240724E-4
+PB = 0.9148626
+MJSW = 0.2025106
+CF = 0
+PK2 = -0.0283027
```
Typical Model Parameters (cont)

```
.MODEL CMOS P MOS (cont)
+VERSION = 3.1
+XJ = 1.5E-7
+K1 = 0.5600277
+K3B = -1.0103515
+DVTDW = 0
+DVTDU = 2.2199372
+VTO = 220.5172252
+UC = -5.76090E-11
+AGS = 0.157354
+RDSW = 3E3
+MR = 1
+XL = 1E-7
+DWB = 1.629532E-8
+CIT = 0
+CDSCB = 0
+DSUB = 1
+PDIBLC2 = 3.172604E-3
+PSCBE1 = 1.851867E10
+DELTA = 0.01
+PR = 0
+HT = 0
+UB1 = -7.61E-18
+WL = 0
+MNW = 1
+MNW = 1
+MLN = 1
+MLW = 0
+LW = 0
+LW = 0
+LW = 0
+CAPMD = 2
+CGDO = 3.09E-10
+CJ = 7.4100006E-4
+CJSW = 2.487127E-10
+CJSWG = 6.4E-11
+CF = 0
+PK = 3.73981E-3
+KETA = 2.873507E-3
```

LEVEL = 49
TOX = 1.4E-8
VTHO = -0.9633249
K3 = 7.2192028
NLY = 5.826683E-8
DVT1W = 0
DVT2W = 0
DVT1U = 0.5378964
DVT2U = -0.1158128
UA = 3.141811E-9
UB = 1.085892E-21
VSA = 1.342779E5
AO = 0.9333022
BO = 9.735259E-7
B1 = 5E-6
AI = 3.447612E-4
A2 = 0.3701317
PRWG = -0.0418464
PRWB = -0.0212357
NINT = 3.097872E-7
LINT = 1.040378E-7
XW = 0
VOFF = -0.0323738
CDSC = 2.4E-4
ETA = 0.4935496
ETAB = -0.0653358
PCLM = 2.1142057
PDIBLC1 = 0.0256688
PSCE = 1.697939E-9
PVAG = 0
RSH = 103.6
MOEMOD = 1
UTE = -1.5
XT = -0.11
UX = 4.31E-9
UC = -5.6E-11
AT = 3.3E4
UL = 0
LL = 0
LW = 0
LWN = 1
XPART = 0.5
XPAR = 0.5
CB = 0.3877813
MJSW = 0.3877813
PDSW = 14.859842
## Typical Design Rules (cont)

### SCMOS Layout Rules - Poly

<table>
<thead>
<tr>
<th>Rule</th>
<th>Description</th>
<th>Lambda</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.1</td>
<td>Minimum width</td>
<td>2</td>
</tr>
<tr>
<td>3.2</td>
<td>Minimum spacing over field</td>
<td>2</td>
</tr>
<tr>
<td>3.2.a</td>
<td>Minimum spacing over active</td>
<td>2</td>
</tr>
<tr>
<td>3.3</td>
<td>Minimum gate extension of active</td>
<td>2</td>
</tr>
<tr>
<td>3.4</td>
<td>Minimum active extension of poly</td>
<td>3</td>
</tr>
<tr>
<td>3.5</td>
<td>Minimum field poly to active</td>
<td>1</td>
</tr>
</tbody>
</table>

![Diagram showing Poly and Active regions with design rules 3.1, 3.2, 3.3, 3.4, 3.5 marked]
Design Rules

• Give minimum feature sizes, spacing, and other constraints that are acceptable in a process

• Very large number of devices can be reliably made with the design rules of a process

• Yield and performance unpredictable and often low if rules are violated

• Compatible with design rule checker in integrated toolsets
Design Rules and Layout — consider transistors

Layer Map
- p-active
- n-active
- Poly 1
- Metal 1
- n-well
- contact

Layout always represented in a top view in two dimensions
Design rules give minimum feature sizes and spacings

Designers generally do layouts to minimize size of circuit subject to design rule constraints (because yield, cost, and performance usually improve)
Design Rules and Layout – consider transistors

Layer Map
- p-active
- n-active
- Poly 1
- Metal 1
- n-well
- contact

- Bulk connection needed
- Single bulk connection can often be used for several (many) transistors
Design Rules and Layout – consider transistors

Layer Map

- p-active
- n-active
- Poly 1
- Metal 1
- n-well
- contact

- Bulk connection needed
- Single bulk connection can often be used for several (many) transistors if they share the same well
Design Rules and Layout (example)

Logic Circuit

Circuit Schematic (Including Device Sizing)

Stick Diagram
Design Rules (example)
Design Rules (example)

• Polygons merged in Geometric Description File (GDF)
• Separate rectangles generally more convenient to represent
Design Rules (example)

- Design rules must be satisfied throughout the design
- DRC runs incrementally during layout in most existing tools to flag most problems
- DRC can catch layout errors but not circuit design errors
Design Rules  (example)

What is wrong with this layout?

_Bulk connections missing!_
Design Rules (example)

- Note diffusions needed for bulk connections
- Note p-well connections increase area a significant amount
- Note p-wells are both connected to $V_{DD}$ in this circuit
Design Rules (example)

Layout with shared p-well reduces area
Shared p-active can be combined to reduce area

Shared n-active can be combined to reduce area
Design Rules

• Design rules can be given in absolute dimensions for every rule

• Design rules can be parameterized and given relative to a parameter
  – Makes movement from one process to another more convenient
  – Easier for designer to remember
  – Some penalty in area efficiency
  – Often termed $\lambda$-based design rules
  – Typically $\lambda$ is $\frac{1}{2}$ the minimum feature size in a process
Design Rules

• See www.MOSIS.org for design rules
Welcome to MOSIS

MOSIS is an integrated circuit fabrication service where you can purchase prototype and small-volume production quantities of integrated circuits and related products. MOSIS lowers the cost of fabrication by combining designs from many customers onto multi-project wafers, thereby significantly decreasing the cost of each design.

MOSIS in the News

<table>
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<tr>
<th>New MOSIS Users</th>
<th>Experienced MOSIS Users</th>
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</thead>
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<td>Purchasing Agents</td>
<td>Design and Test</td>
</tr>
<tr>
<td>Academic Institutions</td>
<td>Export Program</td>
</tr>
</tbody>
</table>

Fabrication Processes
AMIR - austrimicrosystems - IBM - TSMC
All Fabricators

Looking for something special? Check our Site Map or Search MOSIS.
Design Rules

• See [www.MOSIS.org](http://www.MOSIS.org) for design rules

• Some of these files are on class WEB site
  – Mosis Rules Pictorial.pdf
<table>
<thead>
<tr>
<th>Technology code with link to layer map</th>
<th>Layers</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCNE</td>
<td>N_well, Active, N_select, P_select, Poly, Poly2, Contact, Metal1, Via, Metal2, Glass</td>
</tr>
<tr>
<td>SCNA</td>
<td>N_well, Active, N_select, P_select, Poly, Poly2, Contact, Pbase, Metal1, Via, Metal2, Glass</td>
</tr>
<tr>
<td>SCNPC</td>
<td>N_well, Active, N_select, P_select, Poly_cap, Poly, Contact, Metal1, Via, Metal2, Glass</td>
</tr>
<tr>
<td>SCN3M</td>
<td>N_well, Active, N_select, P_select, Poly, Silicide block (Agilent/HP only), Hi_Res_Implant, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass</td>
</tr>
<tr>
<td>SCN3ME</td>
<td>N_well, Active, N_select, P_select, Poly, Poly2, Hi_Res_Implant, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass</td>
</tr>
<tr>
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<td>Layers</td>
</tr>
<tr>
<td>--------------------------------------</td>
<td>---------------------------------------------</td>
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</table>
SCMOS Layout Rules - Well

<table>
<thead>
<tr>
<th>Rule</th>
<th>Description</th>
<th>Lambda</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>SCMOS</td>
</tr>
<tr>
<td>1.1</td>
<td>Minimum width</td>
<td>10</td>
</tr>
<tr>
<td>1.2</td>
<td>Minimum spacing between wells at different potential</td>
<td>12</td>
</tr>
<tr>
<td>1.3</td>
<td>Minimum spacing between wells at same potential</td>
<td>12</td>
</tr>
<tr>
<td>1.4</td>
<td>Minimum spacing between wells of different type (if both are drawn)</td>
<td>0</td>
</tr>
</tbody>
</table>

|      |                                                       | SUBM    |
| 1.2  |                                                       | 18      |
| 1.3  |                                                       | 18      |
|      |                                                       | DEEP    |

Exceptions for AMIS C30 0.35 micron process:

1 Use lambda=16 for rule 1.2 only when using SCN4M or SCN4ME
2 Use lambda=21 for rule 1.2 only when using SCN4M_SUBM or SCN4ME_SUBM
3 Use lambda=8 for rule 1.3 only when using SCN4M or SCN4ME
4 Use lambda=11 for rule 1.3 only when using SCN4M_SUBM or SCN4ME_SUBM
<table>
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<tr>
<td>SCN3ME</td>
<td>N_well, Active, N_select, P_select, Poly, Poly2, Hi_Res_Implant, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass</td>
</tr>
</tbody>
</table>
### SCMOS Layout Rules - Active

<table>
<thead>
<tr>
<th>Rule</th>
<th>Description</th>
<th>Lambda SCMOS</th>
<th>Lambda SUBM</th>
<th>Lambda DEEP</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.1</td>
<td>Minimum width</td>
<td>3 *</td>
<td>3 *</td>
<td>3</td>
</tr>
<tr>
<td>2.2</td>
<td>Minimum spacing</td>
<td>3</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>2.3</td>
<td>Source/drain active to well edge</td>
<td>5</td>
<td>6</td>
<td>6</td>
</tr>
<tr>
<td>2.4</td>
<td>Substrate/well contact active to well edge</td>
<td>3</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>2.5</td>
<td>Minimum spacing between non-abutting active of different implant. Abutting active (&quot;split-active&quot;) is illustrated under Select Layout Rules.</td>
<td>4</td>
<td>4</td>
<td>4</td>
</tr>
</tbody>
</table>

*Note: For analog and critical digital designs, MOSIS recommends the following minimum MOS channel widths (active under poly) for AMIS designs. Narrower devices, down to design rule minimum, will be functional, but their electrical characteristics will not scale, and their performance is not predictable from MOSIS SPICE parameters.*

<table>
<thead>
<tr>
<th>Process</th>
<th>Design Technology</th>
<th>Design Lambda (micrometers)</th>
<th>Minimum Width (lambda)</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMI_ABN</td>
<td>SCNA, SCNE</td>
<td>0.80</td>
<td>5</td>
</tr>
<tr>
<td>AMI_C5F/N</td>
<td>SCN3M, SCN3ME</td>
<td>0.35</td>
<td>9</td>
</tr>
<tr>
<td>AMI_C5F/N</td>
<td>SCN3M_SUBM, SCN3ME_SUBM</td>
<td>0.30</td>
<td>10</td>
</tr>
</tbody>
</table>

![Diagram of SCMOS Layout Rules - Active](image)
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<tr>
<td>SCN3ME</td>
<td>N_well, Active, N_select, P_select, Poly, Poly2, Hi_Res_Implant, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass</td>
</tr>
</tbody>
</table>
SCMOS Layout Rules - Poly

<table>
<thead>
<tr>
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<th>Description</th>
<th>Lambda</th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>3.1</td>
<td>Minimum width</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>3.2</td>
<td>Minimum spacing over field</td>
<td>2</td>
<td>3</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>3.2.a</td>
<td>Minimum spacing over active</td>
<td>2</td>
<td>3</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>3.3</td>
<td>Minimum gate extension of active</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2.5</td>
</tr>
<tr>
<td>3.4</td>
<td>Minimum active extension of poly</td>
<td>3</td>
<td>3</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>3.5</td>
<td>Minimum field poly to active</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Diagram:
- Rule 3.1: Minimum width
- Rule 3.2: Minimum spacing over field
- Rule 3.2.a: Minimum spacing over active
- Rule 3.3: Minimum gate extension of active
- Rule 3.4: Minimum active extension of poly
- Rule 3.5: Minimum field poly to active