Improved Device Models
Propagation Delay in Logic Circuits
Review from Last Time

MOS Transistor
Qualitative Discussion of n-channel Operation

Cross-Sectional View

Top View

Designer always works with top view

Complete Symmetry in construction between Drain and Source
Review from Last Time

MOS Transistor
Comparison of Operation

Source assumed connected to (or close to) ground

Source assumed connected to (or close to) $V_{DD}$ and Boolean $G$ at gate is relative to ground
Pull-up and Pull-down Networks

Three key characteristics of Static CMOS Gates
1. PU network comprised of p-channel devices
2. PD network comprised of n-channel devices
3. One and only one of these networks is conducting at the same time

Three properties of Static CMOS Gates (based upon simple switch-level model)

1. $V_H = V_{DD}$, $V_L = 0$ (too good to be true?)
2. $P_H = P_L = 0$ (too good to be true?)
3. $t_{HL} = t_{LH} = 0$ (too good to be true?)

These 3 properties are inherent in Boolean circuits with these 3 characteristics
Example 1:

How many transistors are required to realize the function

\[ F = A \cdot \overline{B} + \overline{A} \cdot C \]

in a basic CMOS process if static NAND and NOR gates are used? Assume A, B and C are available.
Example 1:

How many transistors are required to realize the function

\[ F = \overline{A \cdot B} + \overline{A} \cdot \overline{C} \]

in a basic CMOS process if static NAND and NOR gates are used? Assume A, B and C are available.

Solution:

20 transistors and 5 levels of logic
Example 1:

How many transistors are required to realize the function

\[ F = \overline{A \cdot B} + \overline{A} \cdot \overline{C} \]

in a basic CMOS process if static NAND and NOR gates are used? Assume A, B and C are available.

Solution (alternative): From basic Boolean Manipulations

\[ F = \overline{A} + \overline{B} + \overline{A} \cdot C = \overline{A} + B + \overline{A} \cdot C \]

\[ F = \overline{A} \cdot (1 + C) + B = \overline{A} + B \]

8 transistors and 3 levels of logic
Example 1:

How many transistors are required to realize the function

\[ F = \overline{A \cdot B} + \overline{A} \cdot C \]

in a basic CMOS process if static NAND and NOR gates are used? Assume A, B and C are available.

Solution (alternative): From basic Boolean Manipulations

\[ F = \overline{A \cdot (1+C)} + B = \overline{A} + B \]

\[ F = \overline{A} + B = A \cdot \overline{B} \]

6 transistors and 2 levels of logic
Example 2: XOR Function

\[ Y = A \oplus B \]

A widely-used 2-input Gate

Static CMOS implementation

\[ Y = AB + \overline{AB} \]

22 transistors  5 levels of logic

Delays unacceptable (will show later) and device count is too large!
Example 3: \[ Y = (A \cdot B) + (C \cdot D) \]

Standard Static CMOS Implementation

3 levels of Logic

16 Transistors if Basic CMOS Gates are Used

Can the same Boolean functionality be obtained with less transistors?
Observe:

\[ Y = (A \cdot B) + (C \cdot D) \]

Significant reduction in transistor count and levels of logic for realizing same Boolean function

Termed a “Complex Logic Gate” implementation

Some authors term this a “compound gate”
Complex Logic Gates

\[ Y = (A \cdot B) + (C \cdot D) \]
Complex Gates

Pull up and pull down network never both conducting

One of the two networks is always conducting
When the logic gate shown is not a multiple-input NAND or NOR gate but has Characteristics 1, 2, and 3 above, the gate will be referred to as a Complex Logic Gate.

Complex Logic Gates also implement static logic functions and some authors would refer to this as Static CMOS Logic as well but we will make the distinction and refer to this as “Complex Logic Gates”
Complex Gates

Complex Gate Design Strategy:

1. Implement $\overline{Y}$ in the PDN

2. Implement $Y$ in the PUN (must complement the input variables since p-channel devices are used)

($Y$ and $\overline{Y}$ often expressed in either SOP or POS form)
XOR in Complex Logic Gates

\[ Y = A \oplus B \]

Will express \( \overline{Y} \) and \( Y \) in standard SOP or POS form
XOR in Complex Logic Gates

\[ Y = A \oplus B \]

\[ Y = A\overline{B} + \overline{A}B \]

\[ \overline{Y} = (A\overline{B} + \overline{A}B) \]

\[ \overline{Y} = A\overline{B} \land \overline{A}B \]

\[ \overline{Y} = (\overline{A}+B) \land (A+\overline{B}) \]
XOR in Complex Logic Gates

\[ Y = A\overline{B} + \overline{A}B \]
\[ \overline{Y} = (\overline{A} + B) \cdot (A + \overline{B}) \]
XOR in Complex Logic Gates

\[ Y = A\overline{B} + \overline{A}B \]

\[ \overline{Y} = (\overline{A} + B)(A + \overline{B}) \]

12 transistors and 2 levels of logic

Notice a significant reduction in the number of transistors required
XOR in Complex Logic Gates

\[ Y = A \bar{B} + \bar{A}B \]
\[ \bar{Y} = (\bar{A} + B) \cdot (A + \bar{B}) \]

Multiple PU and PD networks can be used

\[
\bar{Y} = (\bar{A} + B) \cdot (A + \bar{B}) \\
= (\bar{A} \cdot (A + \bar{B})) + (B \cdot (A + \bar{B})) \\
= (\bar{A} \cdot \bar{B}) + (A \cdot B)
\]
Complex Logic Gate Summary:

1. PU network comprised of p-channel device
2. PD network comprised of n-channel device
3. One and only one of these networks is conducting at the same time

If PUN and PDN satisfy the characteristics:

1. PU network comprised of p-channel device
2. PD network comprised of n-channel device
3. One and only one of these networks is conducting at the same time

Properties of PU/PD logic of this type (with simple switch-level model):

- Rail to rail logic swings
- Zero static power dissipation in both Y=1 and Y=0 states
- Arbitrarily fast (too good to be true? will consider again with better model)
Consider $Y = A \cdot B$

Standard CMOS Implementation

2 levels of Logic

6 Transistors if Basic CMOS Gates are Used

Basic noninverting functions generally require more complexity if basic CMOS gates are used for implementation
Pass Transistor Logic

$Y = A \cdot B$

Requires only 2 transistors rather than 6 for a standard CMOS gate (and a resistor).
Pass Transistor Logic

\[ Y = A \cdot B \]

Even simpler pass transistor logic implementations are possible.

Requires only 1 transistor (and a resistor).

Will see later that the area of a single practical resistor for this circuit may be comparable to that needed for hundreds or even thousands of transistors.
Pass Transistor Logic

May be able to replace resistor with transistor

But high logic level can not be determined with existing device model (or even low logic level for circuit on right)
Pass Transistor Logic

\[ Y = A \oplus B \]

6 transistors, 1 resistor, two levels of logic

(the 4 transistors in the two inverters are not shown)
Pass Transistor Logic

\[ Y = A \oplus B \]

2 transistors, 1 resistor, one level of logic
Pass Transistor Logic

- Requires only 1 transistor (and a resistor)
- Pass transistor logic can offer significant reductions in complexity for some functions (particularly noninverting)
- Resistor may require more area than several hundred or even several thousand transistors
- Signal levels may not go to $V_{DD}$ or to 0V
- Static power dissipation may not be zero
- Signals may degrade unacceptably if multiple gates are cascaded
- “resistor” often implemented with a transistor to reduce area but signal swing and power dissipation problems still persist
- Pass transistor logic is widely used
Logic Design Styles

• Several different logic design styles are often used throughout a given design (3 considered thus far)
  – Static CMOS
  – Complex Logic Gates
  – Pass Transistor Logic

• The designer has complete control over what is placed on silicon and governed only by cost and performance

• New logic design strategies have been proposed recently and others will likely emerge in the future

• The digital designer needs to be familiar with the benefits and limitations of varying logic styles to come up with a good solution for given system requirements
Simple model of MOSFET was developed \(\text{(termed switch-level model)}\)

Simple gates designed in CMOS Process were introduced
- Some have zero power dissipation
- Some have or appeared to have rail to rail logic voltage swings
- All appeared to be Infinitely fast
- Logic levels of some can not be predicted with simple model
- Simple model is not sufficiently accurate to provide insight relating to some of these properties

MOSFET modeling strategy
- hierarchical model structure will be developed
- generally use simplest model that can be justified
MOS Transistor Models

1. Switch-Level model

Advantages:
Simple, does not require understanding of semiconductor properties, does not depend upon process, adequate for understanding basic operation of many digital circuits

Limitations:
Does not provide timing information (surfaced when looking at static CMOS circuits, and several others that have not yet become apparent from the applications that have been considered) and can not support design of “resistor” used in Pass Transistor Logic
Improved Device Models

With the simple switch-level model, it was observed that basic static CMOS logic gates have the following three properties:

- Rail to rail logic swings
- Zero static power dissipation in both $Y=1$ and $Y=0$ states
- Arbitrarily fast (too good to be true? will consider again with better model)

It can be shown that the first two properties are nearly satisfied in actual fabricated circuits but though the circuits are fast, they are observably not arbitrarily fast.

Will now extend switch-level model to predict speed of basic gates
Recall

MOS Transistor
Qualitative Discussion of n-channel Operation

n-channel MOSFET

\[ D \quad S \quad G = 0 \]
\[ D \quad S \quad G = 1 \]
MOS Transistor
Qualitative Discussion of n-channel Operation

n-channel MOSFET

Bulk
Source
Gate
Drain

n-channel MOSFET

G = 0
D = S

G = 1
D = S

Gate
Source
Drain
MOS Transistor
Qualitative Discussion of n-channel Operation

For $V_{GS}$ small

For $V_{GS}$ large
MOS Transistor
Qualitative Discussion of n-channel Operation

For $V_{GS}$ small

For $V_{GS}$ large

- Capacitance from gate to channel region is distributed
- Lumped capacitance much easier to work with
Improved Switch-Level Model

Switch-level model including gate capacitance and channel resistance

Still neglect bulk connection and connect the gate capacitance to the source
Improved Switch-Level Model

n-channel

Switch-Level model

Switch closed for $V_{GS} = \text{"1"}$

Switch-level model including gate capacitance and channel resistance
Improved Switch-Level Model

Switch-level model including gate capacitance and channel resistance

Switch closed for \( V_{GS} = 0 \)

Switch-level model including gate capacitance and channel resistance

Switch-level model

Drain
Gate
Source

\( p \)-channel
Improved Switch-Level Model

Switch-level model including gate capacitance and channel resistance

Switch closed for \( V_{GS} = \text{"1"} \)

\( C_{GS} \) and \( R_{SW} \) dependent upon device sizes and process

For minimum-sized devices in a 0.5\( \mu \) process

\[
C_{GS} \approx 1.5\text{fF} \\
R_{sw} \approx \begin{cases} 2\text{K}\Omega & \text{n-channel} \\ 6\text{K}\Omega & \text{p-channel} \end{cases}
\]

Considerable emphasis will be placed upon device sizing to manage \( C_{GS} \) and \( R_{SW} \)
Is a capacitor of 1.5fF small enough to be neglected?

Area allocations shown to relative scale:
Is a capacitor of 1.5fF small enough to be neglected?

Area allocations shown to relative scale:

- Not enough information at this point to determine whether this very small capacitance can be neglected
- Will answer this important question later
Model Summary

1, Switch-Level model

2, Improved switch-level model

Switch closed for $V_{GS} = \text{large}$

Switch open for $V_{GS} = \text{small}$

Other models will be developed later
End of Lecture 5