EE 330
Lecture 6

Propagation Delay
Stick Diagrams
Technology Files
- Design Rules
MOS Transistor
Qualitative Discussion of n-channel Operation

Review from Last Time

For $V_{GS}$ small

For $V_{GS}$ large
MOS Transistor

Qualitative Discussion of n-channel Operation

For $V_{GS}$ small
- Thin “film” resistor is electrically created
- Capacitance from gate to channel region is distributed
- Lumped capacitance much easier to work with

For $V_{GS}$ large

Review from Last Time
Review from Last Time

**Improved Switch-Level Model**

Switch-level model including gate capacitance and channel resistance

Still neglect bulk connection and connect the gate capacitance to the source
Review from Last Time

Improved Switch-Level Model

Switch-level model

Switch closed for $V_{GS}$ = large

Alt: switch closed for “$G = 1$”

Switch-level model including gate capacitance and channel resistance
Review from Last Time

Improved Switch-Level Model

Switch-level model including gate capacitance and channel resistance

Switch closed for $V_{GS}$ large and negative

Alt: If $S$ near $V_{DD}$, closed for $G=0$
**Improved Switch-Level Model**

Switch-level model including gate capacitance and channel resistance

**S**witch closed for $G = 1$

$C_{GS}$ and $R_{SW}$ dependent upon device sizes and process

For minimum-sized devices in a 0.5u process

$C_{GS} \approx 1.5fF$

$R_{SW} \approx \begin{cases} 
2K\Omega & \text{n-channel} \\
6K\Omega & \text{p-channel} 
\end{cases}$

Considerable emphasis will be placed upon device sizing to manage $C_{GS}$ and $R_{SW}$
Is a capacitor of 1.5fF small enough to be neglected?

Area allocations shown to relative scale:
Is a capacitor of 1.5fF small enough to be neglected?

Area allocations shown to relative scale:

- Not enough information at this point to determine whether this very small capacitance can be neglected
- Will answer this important question later
Model Summary (for n-channel)

1, Switch-Level model

Switch closed for \( V_{GS} = \text{large} \)
Switch open for \( V_{GS} = \text{small} \)

2, Improved switch-level model

Other models will be developed later
Example

**What are** $t_{HL}$ **and** $t_{LH}$? 

**Assume** $V_{DD}=5V$

**With basic switch level model?**

**With improved switch level model?**
Example

Inverter with basic switch-level model

- p-channel Model
  - G
  - A
  - VDD
  - Y

- n-channel Model
  - G
  - A
  - VDD
  - Y
Example

What are $t_{HL}$ and $t_{LH}$?

With basic switch level model

$t_{HL}=t_{LH}=0$
Example (cont)

*With simple switch-level model* \( t_{HL} = t_{LH} = 0 \)

\[ \text{Inverter} \]

*With improved model?*
Example (cont)

*Inverter with improved model*

**Inverter**

**Inverter with Improved Model**

\[ A \]

\[ A \]

\[ Y \]

\[ Y \]

\[ V_{DD} \]

\[ R_{SWp} \]

\[ C_{GSp} \]

\[ R_{SWn} \]

\[ C_{GSn} \]
Example (cont)

*With improved model* \( t_{HL} = ? \)

To initiate a HL output transition, assume \( Y \) has been in the high state for a long time and lower switch closes at time \( t=0 \).
Example (cont)

With improved model

$t_{HL}=?$

Recall: Step response of any first-order network with LHP pole can be written as

$$y(t) = F + (I - F)e^{-\frac{t}{\tau}}$$

where $F$ is the final value, $I$ is the initial value and $\tau$ is the time constant of the circuit

For the circuit above, $F=0$, $I=5$ and $\tau = R_{Swn}C_L$
Example (cont)

With improved model

$$V_{\text{OUT}}(t) = F + (1-F)e^{-\frac{t}{\tau}}$$

$$V_{\text{OUT}}(t) = 5e^{-\frac{t}{\tau}}$$

$$\tau = R_{\text{SWn}}C_L$$

how is $t_{HL}$ defined?
Example (cont)

\[ t_{HL} = ? \]

Define \( t_{HL} \) to be the time taken for output to drop to \( I/e \)

\[ V_{OUT}(t) = F + (I - F)e^{-\frac{t}{\tau}} \]

\[ \frac{I}{e} = F + (I - F)e^{-\frac{t_{HL}}{\tau}} \]

\( t_{HL} \) as defined has proved useful at analytically predicting response time of circuits
Example (cont)

With improved model

\[ I = F + (I - F) e^{-\frac{t_{HL}}{\tau}} \]

\[ I = I e^{-\frac{t_{HL}}{\tau}} \]

\[ \frac{1}{e} = e^{-\frac{t_{HL}}{\tau}} \]

\[ t_{HL} = \tau \]

\[ I=5V, \ F=0V \]

\[ \tau = R_{SWn} C_L \]
Example (cont)

With improved model $t_{LH} = ?$

Assume output in low state for a long time and upper switch closes at time $t=0$

$V_{OUT}$

$V_{DD}=5V$

$R_{SWp}=6K$

$1pf$

$5V$

$C_{GSp}$

$C_{GSn}$

$V_{OUT}$

$0V$

$C_{L}$

$0V$ is the initial condition on $C_{L}$
Example (cont)

*With improved model* $t_{LH} = ?$

\[ y(t) = F + (I - F)e^{-\frac{t}{\tau}} \]

*For this circuit, $F=5$, $I=0$ and $R_{SWP}C_L = R_{SWP}C_L$*
Example (cont)

With improved model

$$V_{OUT}(t) = F + (I - F)e^{\frac{t}{\tau}}$$

$$\tau = R_{SWp}C_L$$

How is $t_{LH}$ defined?
Example (cont)

*With improved model*
\[ t_{LH} = ? \]

Define \( t_{LH} \) as shown on figure

\[ V_{\text{OUT}}(t) = F + (I - F)e^{-\frac{t}{\tau}} \]

\[ F\left(1 - \frac{1}{e}\right) = F + (I - F)e^{-\frac{t_{LH}}{\tau}} \]

\( t_{LH} \) as defined has proven useful for analytically predicting response time of circuits
Example (cont)

*With improved model*  

\[ t_{LH} =? \]

\[
F \left(1 - \frac{1}{e}\right) = F + (I - F) e^{-\frac{t_{LH}}{\tau}}
\]

\[
F \left(1 - \frac{1}{e}\right) = F + (F) e^{-\frac{t_{LH}}{\tau}}
\]

\[
1 - \frac{1}{e} = 1 + e^{-\frac{t_{LH}}{\tau}}
\]

\[ t_{LH} = \tau \]

**Diagram:**

\[ I=0V, \ F=5V \]

\[ \tau = R_{SWp} C_L \]
With improved model

Example (cont)

\[
\begin{align*}
    t_{HL} & \approx R_{SWn} C_L \\
    t_{LH} & \approx R_{SWp} C_L
\end{align*}
\]

In the ON 0.5u process

\[
\begin{align*}
    t_{HL} & = 2K \cdot 1pF = 2n\text{sec} \\
    t_{LH} & = 6K \cdot 1pF = 6n\text{sec}
\end{align*}
\]

Note this circuit is quite fast!

Note that \( t_{HL} \) is much shorter than \( t_{LH} \)

Often \( C_L \) will be even smaller and the circuit will be much faster!!
Summary: What is the delay of a minimum-sized inverter driving a 1pF load?

In the ON 0.5μ process

\[ t_{HL} \approx R_{SWn} C_L = 2K \cdot 1pF = 2n\text{sec} \]

\[ t_{LH} \approx R_{SWp} C_L = 6K \cdot 1pF = 6n\text{sec} \]
Improved switch-level model

Switch closed for $V_{GS} =$ large
Switch open for $V_{GS} =$ small

• Previous example showed why $R_{SW}$ in the model was important
• But of what use is the $C_{GS}$ which did not enter the previous calculations?

For minimum-sized devices in a 0.5u process

$C_{GS} \approx 1.5fF \quad R_{SW} \approx \begin{cases} 2K\Omega & \text{n-channel} \\ 6K\Omega & \text{p-channel} \end{cases}$
One gate often drives one or more other gates!

What are $t_{HL}$ and $t_{LH}$?
Example: What is the delay of a minimum-sized inverter driving another identical device?

\[ X \rightarrow Y \rightarrow \text{inverter} \]

\[ \text{Load on first inverter} \]

\[ C_{GSn} \text{ and } C_{GSp} \text{ both } 1.5 \text{fF} \]

\[ C_{GSn} \approx C_{GSn} \approx 1.5 \text{fF} \]

\[ \text{Loading effects same whether } C_{GSp} \text{ and/or } C_{GSn} \text{ connected to } V_{DD} \text{ or GND} \]

\[ 3fF \]

For convenience, will reference both to ground
Is a capacitor of 1.5fF small enough to be neglected?

Area allocations shown to relative scale:

- This example will provide insight into the answer of the question
Example: What is the delay of a minimum-sized inverter driving another identical device? Assume $V_{DD}=5V$
Generalizing the Previous Analysis to Arbitrary Load

\[ t_{HL} \approx R_{SWn} C_L \]
\[ t_{LH} \approx R_{SWp} C_L \]
Example: What is the delay of a minimum-sized inverter driving another identical device?

\[ t_{HL} \approx R_{SWn} C_L = 2K \cdot 3\, fF = 6\, p\, sec \]

\[ t_{LH} \approx R_{SWp} C_L = 6K \cdot 3\, fF = 18\, p\, sec \]

Do gates really operate this fast?

What would be the maximum clock rate for acceptable operation?
Example: What is the delay of a minimum-sized inverter driving another identical device?

\[ t_{\text{HL}} \approx R_{\text{SWn}} C_L = 6\, \text{psec} \]

\[ t_{\text{LH}} \approx R_{\text{SWp}} C_L = 18\, \text{psec} \]

What would be the maximum clock rate for acceptable operation?

\[ f_{\text{CLK-max}} = \frac{1}{T_{\text{CLK-min}}} = \frac{1}{24\, \text{psec}} = 40\, \text{GHz} \]

And much faster in a finer feature process!!

What would be the implications of allowing for 10 levels of logic and 10 loads (FO=10)?
Example: What is the delay of a minimum-sized inverter driving another identical device? SUMMARY

\[ t_{HL} \approx R_{SWn} C_L = 2K \cdot 3fF = 6p\text{sec} \]

\[ t_{LH} \approx R_{SWp} C_L = 6K \cdot 3fF = 18p\text{sec} \]

*Note this is very fast but even the small 1.5fF capacitors are not negligible!*
Response time of logic gates

\[ t_{HL} \approx R_{SWn} C_L \]
\[ t_{LH} \approx R_{SWp} C_L \]

- Logic Circuits can operate very fast
- Extremely small parasitic capacitances play key role in speed of a circuit
Stick Diagrams

- It is often necessary to obtain information about placement, interconnect and physical-layer structure
- Stick diagrams are often used for small component-count blocks
- Approximate placement, routing, and area information can be obtained rather quickly with the use of stick diagrams
Stick Diagrams

Metal 1
poly
n-diffusion
p-diffusion
Metal 2
Contact

Additional layers can be added and color conventions are personal.
A stick diagram is not a layout but gives the basic structure (including location, orientation and interconnects) that will be instantiated in the actual layout itself.

Modifications can be made much more quickly on a stick diagram than on a layout.

Iteration may be needed to come up with a good layout structure.
Stick Diagram

Alternate Representations
Technology Files

- Provide Information About Process
  - Process Flow (Fabrication Technology)
  - Model Parameters
  - Design Rules
- Serve as Interface Between Design Engineer and Process Engineer
- Insist on getting information that is deemed important for a design
  - Limited information available in academia
  - Foundries often sensitive to who gets access to information
  - Customer success and satisfaction is critical to foundries
End of Lecture 6