Design Rules

IC Fabrication Technology Part 1
Technology Files

- Provide Information About Process
  - Process Flow (Fabrication Technology)
  - Model Parameters
  - Design Rules

- Serve as Interface Between Design Engineer and Process Engineer

- Insist on getting information that is deemed important for a design
  - Limited information available in academia
  - Foundries often sensitive to who gets access to information
  - Customer success and satisfaction is critical to foundries
Technology Files

• Design Rules

• Process Flow (Fabrication Technology) (will discuss next)

• Model Parameters (will discuss in substantially more detail after device operation and more advanced models are introduced)

First – A preview of what the technology files look like!
### TABLE 2B.2

Design rules for a typical p-well CMOS process

(See Table 2B.3 in color plates for graphical interpretation)

<table>
<thead>
<tr>
<th>Design Rule</th>
<th>Dimensions</th>
<th>Microns</th>
<th>Scalable</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. p-well (CIF Brown, Mask #1&lt;sup&gt;a&lt;/sup&gt;)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.1 Width</td>
<td></td>
<td>5</td>
<td>4λ</td>
</tr>
<tr>
<td>1.2 Spacing (different potential)</td>
<td></td>
<td>15</td>
<td>10λ</td>
</tr>
<tr>
<td>1.3 Spacing (same potential)</td>
<td></td>
<td>9</td>
<td>6λ</td>
</tr>
<tr>
<td>2. Active (CIF Green, Mask #2)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2.1 Width</td>
<td></td>
<td>4</td>
<td>2λ</td>
</tr>
<tr>
<td>2.2 Spacing</td>
<td></td>
<td>4</td>
<td>2λ</td>
</tr>
<tr>
<td>2.3 p&lt;sup&gt;+&lt;/sup&gt; active in n-sub to p-well edge</td>
<td></td>
<td>8</td>
<td>6λ</td>
</tr>
<tr>
<td>2.4 n&lt;sup&gt;+&lt;/sup&gt; active in n-sub to p-well edge</td>
<td></td>
<td>7</td>
<td>5λ</td>
</tr>
<tr>
<td>2.5 n&lt;sup&gt;+&lt;/sup&gt; active in p-well to p-well edge</td>
<td></td>
<td>4</td>
<td>2λ</td>
</tr>
<tr>
<td>2.6 p&lt;sup&gt;+&lt;/sup&gt; active in p-well to p-well edge</td>
<td></td>
<td>1</td>
<td>λ</td>
</tr>
<tr>
<td>3. Poly (POLY I) (CIF Red, Mask #3)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3.1 Width</td>
<td></td>
<td>3</td>
<td>2λ</td>
</tr>
<tr>
<td>3.2 Spacing</td>
<td></td>
<td>3</td>
<td>2λ</td>
</tr>
<tr>
<td>3.3 Field poly to active</td>
<td></td>
<td>2</td>
<td>λ</td>
</tr>
<tr>
<td>3.4 Poly overlap of active</td>
<td></td>
<td>3</td>
<td>2λ</td>
</tr>
<tr>
<td>3.5 Active overlap of poly</td>
<td></td>
<td>4</td>
<td>2λ</td>
</tr>
<tr>
<td>4. p&lt;sup&gt;+&lt;/sup&gt; select (CIF Orange, Mask #4)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4.1 Overlap of active</td>
<td></td>
<td>2</td>
<td>λ</td>
</tr>
<tr>
<td>4.2 Space to n&lt;sup&gt;+&lt;/sup&gt; active</td>
<td></td>
<td>2</td>
<td>λ</td>
</tr>
<tr>
<td>4.3 Overlap of channel&lt;sup&gt;b&lt;/sup&gt;</td>
<td></td>
<td>3.5</td>
<td>2λ</td>
</tr>
<tr>
<td>4.4 Space to channel&lt;sup&gt;b&lt;/sup&gt;</td>
<td></td>
<td>3.5</td>
<td>2λ</td>
</tr>
<tr>
<td>4.5 Space to p&lt;sup&gt;+&lt;/sup&gt; select</td>
<td></td>
<td>3</td>
<td>2λ</td>
</tr>
<tr>
<td>4.6 Width</td>
<td></td>
<td>3</td>
<td>2λ</td>
</tr>
</tbody>
</table>
Typical Design Rules (cont)

<table>
<thead>
<tr>
<th></th>
<th>Contact&lt;sup&gt;c&lt;/sup&gt; (CIF Purple, Mask #6)</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>5.1</td>
<td>Square contact, exactly</td>
<td>$3 \times 3$</td>
<td>$2\lambda \times 2\lambda$</td>
</tr>
<tr>
<td>5.2</td>
<td>Rectangular contact, exactly</td>
<td>$3 \times 8$</td>
<td>$2\lambda \times 6\lambda$</td>
</tr>
<tr>
<td>5.3</td>
<td>Space to different contact</td>
<td>3</td>
<td>$2\lambda$</td>
</tr>
<tr>
<td>5.4</td>
<td>Poly overlap of contact</td>
<td>2</td>
<td>$\lambda$</td>
</tr>
<tr>
<td>5.5</td>
<td>Poly overlap in direction of metal 1</td>
<td>2.5</td>
<td>$2\lambda$</td>
</tr>
<tr>
<td>5.6</td>
<td>Space to channel</td>
<td>3</td>
<td>$2\lambda$</td>
</tr>
<tr>
<td>5.7</td>
<td>Metal 1 overlap of contact</td>
<td>2</td>
<td>$\lambda$</td>
</tr>
<tr>
<td>5.8</td>
<td>Active overlap of contact</td>
<td>2</td>
<td>$\lambda$</td>
</tr>
<tr>
<td>5.9</td>
<td>$p^+$ select overlap of contact</td>
<td>3</td>
<td>$2\lambda$</td>
</tr>
<tr>
<td>5.10</td>
<td>Subs./well shorting contact, exactly</td>
<td>$3 \times 8$</td>
<td>$2\lambda \times 6\lambda$</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>Metal 1&lt;sup&gt;d&lt;/sup&gt; (CIF Blue, Mask #7)</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>6.1</td>
<td>Width</td>
<td>3</td>
<td>$2\lambda$</td>
</tr>
<tr>
<td>6.2</td>
<td>Spacing</td>
<td>4</td>
<td>$3\lambda$</td>
</tr>
<tr>
<td>6.3</td>
<td>Maximum current density</td>
<td>0.8 mA/µm</td>
<td>0.8 mA/µm</td>
</tr>
</tbody>
</table>
7. Via *(CIF Purple Hatched, Mask #C1)*
   7.1 Size, exactly  \(3 \times 3\)  \(2\lambda \times 2\lambda\)
   7.2 Separation  \(3\)  \(2\lambda\)
   7.3 Space to poly edge  \(4\)  \(2\lambda\)
   7.4 Space to contact  \(3\)  \(2\lambda\)
   7.5 Overlap by metal 1  \(2\)  \(\lambda\)
   7.6 Overlap by metal 2  \(2\)  \(\lambda\)
   7.7 Space to active edge  \(3\)  \(2\lambda\)

8. Metal 2 *(CIF Orange Hatched, Mask #C2)*
   8.1 Width  \(5\)  \(3\lambda\)
   8.2 Spacing  \(5\)  \(3\lambda\)
   8.3 Bonding pad size  \(100 \times 100\)  \(100 \mu \times 100 \mu\)
   8.4 Probe pad size  \(75 \times 75\)  \(75 \mu \times 75 \mu\)
   8.5 Bonding pad separation  \(50\)  \(50 \mu\)
   8.6 Bonding to probe pad  \(30\)  \(30 \mu\)
   8.7 Probe pad separation  \(30\)  \(30 \mu\)
   8.8 Pad to circuitry  \(40\)  \(40 \mu\)
   8.9 Maximum current density  \(0.8 \text{ mA/}\mu\)  \(0.8 \text{ mA/}\mu\)

9. Passivation *(CIF Purple Dashed, Mask #8)*
   9.1 Bonding pad opening  \(90 \times 90\)  \(90 \mu \times 90 \mu\)
   9.2 Probe pad opening  \(65 \times 65\)  \(65 \mu \times 65 \mu\)

10. Metal 2 crossing coincident metal 1 and poly *(CIF Purple Hatched, Mask #A1)*
    10.1 Metal 1 to poly edge spacing when crossing metal 2  \(2\)  \(\lambda\)
    10.2 Rule domain  \(2\)  \(\lambda\)

11. Electrode (POLY II) *(CIF Purple Hatched, Mask #A1)*
    11.1 Width  \(3\)  \(2\lambda\)
    11.2 Spacing  \(3\)  \(2\lambda\)
    11.3 POLY I overlap of POLY II  \(2\)  \(\lambda\)
    11.4 Space to contact  \(3\)  \(2\lambda\)
### Typical Design Rules (cont)

#### SCMOS Layout Rules - Poly

<table>
<thead>
<tr>
<th>Rule</th>
<th>Description</th>
<th>Lambda</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>SCMOS</td>
</tr>
<tr>
<td>3.1</td>
<td>Minimum width</td>
<td>2</td>
</tr>
<tr>
<td>3.2</td>
<td>Minimum spacing over field</td>
<td>2</td>
</tr>
<tr>
<td>3.2.a</td>
<td>Minimum spacing over active</td>
<td>2</td>
</tr>
<tr>
<td>3.3</td>
<td>Minimum gate extension of active</td>
<td>2</td>
</tr>
<tr>
<td>3.4</td>
<td>Minimum active extension of poly</td>
<td>3</td>
</tr>
<tr>
<td>3.5</td>
<td>Minimum field poly to active</td>
<td>1</td>
</tr>
</tbody>
</table>

![Diagram of design rules](image.png)
### Typical Process Description

Process scenario of major process steps in typical p-well CMOS process

<table>
<thead>
<tr>
<th>Step</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Clean wafer</td>
</tr>
<tr>
<td>2.</td>
<td>GROW THIN OXIDE</td>
</tr>
<tr>
<td>3.</td>
<td>Apply photoresist</td>
</tr>
<tr>
<td>4.</td>
<td>PATTERN P-WELL <strong>(MASK #1)</strong></td>
</tr>
<tr>
<td>5.</td>
<td>Develop photoresist</td>
</tr>
<tr>
<td>6.</td>
<td>Deposit and diffuse p-type impurities</td>
</tr>
<tr>
<td>7.</td>
<td>Strip photoresist</td>
</tr>
<tr>
<td>8.</td>
<td>Strip thin oxide</td>
</tr>
<tr>
<td>9.</td>
<td>Grow thin oxide</td>
</tr>
<tr>
<td>10.</td>
<td>Apply layer of Si$_3$N$_4$</td>
</tr>
<tr>
<td>11.</td>
<td>Apply photoresist</td>
</tr>
<tr>
<td>12.</td>
<td>PATTERN Si$_3$N$_4$ (active area definition) <strong>(MASK #2)</strong></td>
</tr>
<tr>
<td>13.</td>
<td>Develop photoresist</td>
</tr>
<tr>
<td>14.</td>
<td>Etch Si$_3$N$_4$</td>
</tr>
</tbody>
</table>
| 15.  | Strip photoresist  
   *Optional field threshold voltage adjust*  
   A.1 Apply photoresist  
   A.2 PATTERN ANTIMOAT IN SUBSTRATE **(MASK #A1)**  
   A.3 Develop photoresist  
   A.4 FIELD IMPLANT (n-type)  
   A.5 Strip photoresist |
| 16.  | GROW FIELD OXIDE |
| 17.  | Strip Si$_3$N$_4$ |
| 18.  | Strip thin oxide |
| 19.  | GROW GATE OXIDE |
| 20.  | POLYSILICON DEPOSITION (POLY I) |
| 21.  | Apply photoresist |
| 22.  | PATTERN POLYSILICON **(MASK #3)** |
| 23.  | Develop photoresist |
| 24.  | ETCH POLYSILICON |
Typical Process Description (cont)

25. Strip photoresist
    *Optional steps for double polysilicon process*
    B.1 Strip thin oxide
    B.2 GROW THIN OXIDE
    B.3 POLYSILICON DEPOSITION (POLY II)
    B.4 Apply photoresist
    B.5 PATTERN POLYSILICON
        (MASK #B1)
    B.6 Develop photoresist
    B.7 ETCH POLYSILICON
    B.8 Strip photoresist
    B.9 Strip thin oxide

26. Apply photoresist
27. PATTERN P-CHANNEL DRAINS AND SOURCES AND
    P⁺ GUARD RINGS (p-well ohmic contacts)
        (MASK #4)
28. Develop photoresist
29. p⁺ IMPLANT
30. Strip photoresist
31. Apply photoresist
32. PATTERN N-CHANNEL DRAINS AND SOURCES AND
    N⁺ GUARD RINGS (top ohmic contact to substrate)
        (MASK #5)
33. Develop photoresist
34. n⁺ IMPLANT
35. Strip photoresist
36. Strip thin oxide
37. Grow oxide
38. Apply photoresist
39. PATTERN CONTACT OPENINGS
        (MASK #6)
40. Develop photoresist
41. Etch oxide
42. Strip photoresist
43. APPLY METAL
44. Apply photoresist
45. PATTERN METAL
        (MASK #7)
46. Develop photoresist
47. Etch metal
48. Strip photoresist

*Optional steps for double metal process*

C.1 Strip thin oxide
C.2 DEPOSIT INTERMETAL OXIDE
C.3 Apply photoresist
C.4 PATTERN VIAS
C.5 Develop photoresist
C.6 Etch oxide
C.7 Strip photoresist
C.8 APPLY METAL (Metal 2)
C.9 Apply photoresist
C.10 PATTERN METAL
C.11 Develop photoresist
C.12 Etch metal
C.13 Strip photoresist

(MASK #C1)

49. APPLY PASSIVATION

50. Apply photoresist

51. PATTERN PAD OPENINGS

(MASK #8)

52. Develop photoresist
53. Etch passivation
54. Strip photoresist
55. ASSEMBLE, PACKAGE AND TEST
### Process parameters for a typical p-well CMOS process

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Typical</th>
<th>Tolerance $^b$</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Square law model parameters</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{T0}$ (threshold voltage)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>n-channel ($V_{TNO}$)</td>
<td>0.75</td>
<td>$\pm 0.25$</td>
<td>V</td>
</tr>
<tr>
<td>p-channel ($V_{TPO}$)</td>
<td>-0.75</td>
<td>$\pm 0.25$</td>
<td>V</td>
</tr>
<tr>
<td>$K$ (conduction factor)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>n-channel</td>
<td>24</td>
<td>$\pm 6$</td>
<td>$\mu A/V^2$</td>
</tr>
<tr>
<td>p-channel</td>
<td>8</td>
<td>$\pm 1.5$</td>
<td>$\mu A/V^2$</td>
</tr>
<tr>
<td>$\gamma$ (body effect)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>n-channel</td>
<td>0.8</td>
<td>$\pm 0.4$</td>
<td>$V^{1/2}$</td>
</tr>
<tr>
<td>p-channel</td>
<td>0.4</td>
<td>$\pm 0.2$</td>
<td>$V^{1/2}$</td>
</tr>
<tr>
<td>$\lambda$ (channel length modulation)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>n-channel</td>
<td>0.01</td>
<td>$\pm 50%$</td>
<td>$V^{-1}$</td>
</tr>
<tr>
<td>p-channel</td>
<td>0.02</td>
<td>$\pm 50%$</td>
<td>$V^{-1}$</td>
</tr>
<tr>
<td>$\phi$ (surface potential)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>n- and p-channel</td>
<td>0.6</td>
<td>$\pm 0.1$</td>
<td>V</td>
</tr>
<tr>
<td><strong>Process parameters</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\mu$ (channel mobility)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>n-channel</td>
<td>710</td>
<td></td>
<td>$cm^2/(V \cdot s)$</td>
</tr>
<tr>
<td>p-channel</td>
<td>230</td>
<td></td>
<td>$cm^2/(V \cdot s)$</td>
</tr>
<tr>
<td><strong>Doping</strong> $^c$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>n$^+$ active</td>
<td>5</td>
<td>$\pm 4$</td>
<td>$10^{18}/cm^3$</td>
</tr>
<tr>
<td>p$^+$ active</td>
<td>5</td>
<td>$\pm 4$</td>
<td>$10^{17}/cm^3$</td>
</tr>
<tr>
<td>p-well</td>
<td>5</td>
<td>$\pm 2$</td>
<td>$10^{16}/cm^3$</td>
</tr>
<tr>
<td>n-substrate</td>
<td>1</td>
<td>$\pm 0.1$</td>
<td>$10^{16}/cm^3$</td>
</tr>
</tbody>
</table>
### Typical Model Parameters (cont)

#### Physical feature sizes

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Uncertainty</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_{\text{OX}}$ (gate oxide thickness)</td>
<td>500</td>
<td>± 100</td>
<td>Å</td>
</tr>
<tr>
<td>Total lateral diffusion</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>n-channel</td>
<td>0.45</td>
<td>± 0.15</td>
<td>µ</td>
</tr>
<tr>
<td>p-channel</td>
<td>0.6</td>
<td>± 0.3</td>
<td>µ</td>
</tr>
<tr>
<td>Diffusion depth</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$n^+$ diffusion</td>
<td>0.45</td>
<td>± 0.15</td>
<td>µ</td>
</tr>
<tr>
<td>$p^+$ diffusion</td>
<td>0.6</td>
<td>± 0.3</td>
<td>µ</td>
</tr>
<tr>
<td>p-well</td>
<td>3.0</td>
<td>± 30%</td>
<td>µ</td>
</tr>
</tbody>
</table>

#### Insulating layer separation

<table>
<thead>
<tr>
<th>Layer Separation</th>
<th>Value</th>
<th>Uncertainty</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>POLY I to POLY II</td>
<td>800</td>
<td>± 100</td>
<td>Å</td>
</tr>
<tr>
<td>Metal 1 to Substrate</td>
<td>1.55</td>
<td>± 0.15</td>
<td>µ</td>
</tr>
<tr>
<td>Metal 1 to Diffusion</td>
<td>0.925</td>
<td>± 0.25</td>
<td>µ</td>
</tr>
<tr>
<td>POLY I to Substrate (POLY I on field oxide)</td>
<td>0.75</td>
<td>± 0.1</td>
<td>µ</td>
</tr>
<tr>
<td>Metal 1 to POLY I</td>
<td>0.87</td>
<td>± 0.7</td>
<td>µ</td>
</tr>
<tr>
<td>Metal 2 to Substrate</td>
<td>2.7</td>
<td>± 0.25</td>
<td>µ</td>
</tr>
<tr>
<td>Metal 2 to Metal I</td>
<td>1.2</td>
<td>± 0.1</td>
<td>µ</td>
</tr>
<tr>
<td>Metal 2 to POLY I</td>
<td>2.0</td>
<td>± 0.07</td>
<td>µ</td>
</tr>
</tbody>
</table>
### Capacitances

<table>
<thead>
<tr>
<th>Capacitance</th>
<th>Value</th>
<th>Uncertainty</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{OX}$ (gate oxide capacitance, n- and p-channel)</td>
<td>0.7</td>
<td>±0.1</td>
<td>fF/μm²</td>
</tr>
<tr>
<td>POLY I to substrate, poly in field</td>
<td>0.045</td>
<td>±0.01</td>
<td>fF/μm²</td>
</tr>
<tr>
<td>POLY II to substrate, poly in field</td>
<td>0.045</td>
<td>±0.01</td>
<td>fF/μm²</td>
</tr>
<tr>
<td>Metal 1 to substrate, metal in field</td>
<td>0.025</td>
<td>±0.005</td>
<td>fF/μm²</td>
</tr>
<tr>
<td>Metal 2 to substrate, metal in field</td>
<td>0.014</td>
<td>±0.002</td>
<td>fF/μm²</td>
</tr>
<tr>
<td>POLY I to POLY II</td>
<td>0.44</td>
<td>±0.05</td>
<td>fF/μm²</td>
</tr>
<tr>
<td>POLY I to Metal 1</td>
<td>0.04</td>
<td>±0.01</td>
<td>fF/μm²</td>
</tr>
<tr>
<td>POLY I to Metal 2</td>
<td>0.039</td>
<td>±0.003</td>
<td>fF/μm²</td>
</tr>
<tr>
<td>Metal 1 to Metal 2</td>
<td>0.035</td>
<td>±0.01</td>
<td>fF/μm²</td>
</tr>
<tr>
<td>Metal 1 to diffusion</td>
<td>0.04</td>
<td>±0.01</td>
<td>fF/μm²</td>
</tr>
<tr>
<td>Metal 2 to diffusion</td>
<td>0.02</td>
<td>±0.005</td>
<td>fF/μm²</td>
</tr>
<tr>
<td>n⁺ diffusion to p-well (junction, bottom)</td>
<td>0.33</td>
<td>±0.17</td>
<td>fF/μm²</td>
</tr>
<tr>
<td>n⁺ diffusion sidewall (junction, sidewall)</td>
<td>2.6</td>
<td>±0.6</td>
<td>fF/μ</td>
</tr>
<tr>
<td>p⁺ diffusion to substrate (junction, bottom)</td>
<td>0.38</td>
<td>±0.12</td>
<td>fF/μm²</td>
</tr>
<tr>
<td>p⁺ diffusion sidewall (junction, sidewall)</td>
<td>3.5</td>
<td>±2.0</td>
<td>fF/μ</td>
</tr>
<tr>
<td>p-well to substrate (junction, bottom)</td>
<td>0.2</td>
<td>±0.1</td>
<td>fF/μm²</td>
</tr>
<tr>
<td>p-well sidewall (junction, sidewall)</td>
<td>1.6</td>
<td>±1.0</td>
<td>fF/μ</td>
</tr>
</tbody>
</table>

### Resistances

<table>
<thead>
<tr>
<th>Resistance</th>
<th>Value</th>
<th>Uncertainty</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Substrate</td>
<td>25</td>
<td>±20%</td>
<td>Ω-cm</td>
</tr>
<tr>
<td>p-well</td>
<td>5000</td>
<td>±2500</td>
<td>Ω/□</td>
</tr>
<tr>
<td>n⁺ diffusion</td>
<td>35</td>
<td>±25</td>
<td>Ω/□</td>
</tr>
<tr>
<td>p⁺ diffusion</td>
<td>80</td>
<td>±55</td>
<td>Ω/□</td>
</tr>
<tr>
<td>Metal</td>
<td>0.003</td>
<td>±25%</td>
<td>Ω/□</td>
</tr>
<tr>
<td>Poly</td>
<td>25</td>
<td>±25%</td>
<td>Ω/□</td>
</tr>
<tr>
<td>Metal 1–Metal 2 via (3 μ × 3 μ contact)</td>
<td>&lt;0.1</td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>Metal 1 contact to POLY I (3 μ × 3 μ contact)</td>
<td>&lt;10</td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>Metal 1 contact to n⁺ or p⁺ diffusion</td>
<td>&lt;5</td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>(3 μ × 3 μ contact)</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
## Breakdown voltages, leakage currents, migration currents and operating conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Punchthrough voltages (Gate oxide, POLY I to POLY II)</td>
<td>&gt;10</td>
<td>V</td>
</tr>
<tr>
<td>Diffusion reverse breakdown voltage</td>
<td>&gt;10</td>
<td>V</td>
</tr>
<tr>
<td>p-well to substrate reverse breakdown voltage</td>
<td>&gt;20</td>
<td>V</td>
</tr>
<tr>
<td>Metal 1 in field threshold voltage</td>
<td>&gt;10</td>
<td>V</td>
</tr>
<tr>
<td>Metal 2 in field threshold voltage</td>
<td>&gt;10</td>
<td>V</td>
</tr>
<tr>
<td>Poly-field threshold voltage</td>
<td>&gt;10</td>
<td>V</td>
</tr>
<tr>
<td>Maximum operating voltage</td>
<td>7.0</td>
<td>V</td>
</tr>
<tr>
<td>n⁺ diffusion to p-well leakage current</td>
<td>0.25</td>
<td>fA/μ²</td>
</tr>
<tr>
<td>p⁺ diffusion to substrate leakage current</td>
<td>0.25</td>
<td>fA/μ²</td>
</tr>
<tr>
<td>p-well leakage current</td>
<td>0.25</td>
<td>fA/μ²</td>
</tr>
<tr>
<td>Maximum metal current density</td>
<td>0.8</td>
<td>mA/μ width</td>
</tr>
<tr>
<td>Maximum device operating temperature</td>
<td>200</td>
<td>°C</td>
</tr>
<tr>
<td>Parameter (Level 2 model)</td>
<td>n-channel</td>
<td>p-channel</td>
</tr>
<tr>
<td>---------------------------</td>
<td>-----------</td>
<td>-----------</td>
</tr>
<tr>
<td>VTO</td>
<td>0.827</td>
<td>-0.895</td>
</tr>
<tr>
<td>KP</td>
<td>32.87</td>
<td>15.26</td>
</tr>
<tr>
<td>GAMMA</td>
<td>1.36</td>
<td>0.879</td>
</tr>
<tr>
<td>PHI</td>
<td>0.6</td>
<td>0.6</td>
</tr>
<tr>
<td>LAMBDA</td>
<td>1.605E-2</td>
<td>4.709E-2</td>
</tr>
<tr>
<td>CGSO</td>
<td>5.2E-4</td>
<td>4.0E-4</td>
</tr>
<tr>
<td>CGDO</td>
<td>5.2E-4</td>
<td>4.0E-4</td>
</tr>
<tr>
<td>RSH</td>
<td>25</td>
<td>95</td>
</tr>
<tr>
<td>CJ</td>
<td>3.2E-4</td>
<td>2.0E-4</td>
</tr>
<tr>
<td>MJ</td>
<td>0.5</td>
<td>0.5</td>
</tr>
<tr>
<td>CJSW</td>
<td>9.0E-4</td>
<td>4.5E-4</td>
</tr>
<tr>
<td>MJSW</td>
<td>0.33</td>
<td>0.33</td>
</tr>
<tr>
<td>TOX</td>
<td>500</td>
<td>500</td>
</tr>
<tr>
<td>NSUB</td>
<td>1.0E16</td>
<td>1.12E14</td>
</tr>
<tr>
<td>NSS</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>NFS</td>
<td>1.235E12</td>
<td>8.79E11</td>
</tr>
<tr>
<td>TPG</td>
<td>1</td>
<td>-1</td>
</tr>
<tr>
<td>XJ</td>
<td>0.4</td>
<td>0.4</td>
</tr>
<tr>
<td>LD</td>
<td>0.28</td>
<td>0.28</td>
</tr>
<tr>
<td>UO</td>
<td>200</td>
<td>100</td>
</tr>
<tr>
<td>UCRIT</td>
<td>9.99E5</td>
<td>1.64E4</td>
</tr>
<tr>
<td>UE XP</td>
<td>1.001E-3</td>
<td>0.1534</td>
</tr>
<tr>
<td>VMAX</td>
<td>1.0E5</td>
<td>1.0E5</td>
</tr>
<tr>
<td>NEFF</td>
<td>1.001E-2</td>
<td>1.001E-2</td>
</tr>
<tr>
<td>DELTA</td>
<td>1.2405</td>
<td>1.938</td>
</tr>
</tbody>
</table>
98 parameters in this BSIM Model!
Typical Model Parameters (cont)

```
.MODEL CMOSP PMOS
+VERSION = 3.1
+XJ    = 1.5E-7
+K1    = 0.5600277
+K3B   = -1.0103515
+DVTOW = 0
+DVTOW = 2.2199372
+UO    = 220.5729225
+UC    = -5.76898E-11
+AGS   = 0.157364
+KETA  = -2.42686E-3
+RDSW  = 3E3
+WR    = 1
+XL    = 1E-7
+DVBT  = 1.629532E-8
+DVBW  = 1.629532E-8
+CIT   = 0
+CDSCB = 0
+DSUB  = 1
+PDIBLC2 = 3.172604E-3
+PSCBE1 = 1.851867E10
+DELTA = 0.01
+PRT   = 0
+KTI1  = 0
+UB1   = -7.61E-18
+WLN   = 0
+WLN   = 1
+LLN   = 1
+LWL   = 0
+CGDO  = 3.09E-10
+CGDO  = 3.09E-10
+CJ    = 7.410008E-4
+CJ    = 7.410008E-4
+CJSW  = 2.487127E-10
+CJSW  = 2.487127E-10
+CJSWG = 6.4E-11
+CJSWG = 6.4E-11
+CF    = 0
+CF    = 0
+PK2   = 3.73981E-3
+PK2   = 3.73981E-3

LEVEL = 49
TOX   = 1.4E-8
VTHO  = -0.9633249
K3    = 7.2192028
NLX   = 5.626683E-8
DVT1W = 0
DVT2W = 0
DVT1  = 0.5378964
DVT2  = -0.1158128
UA    = 3.141611E-9
UB    = 1.085892E-21
VSAT  = 1.342779E5
AO    = 0.9333822
BO    = 9.735259E-7
B1    = 5E-6
A1    = 3.447019E-4
A2    = 0.3701317
PRWG  = -0.0418484
PRWB  = -0.0212357
WINT  = 3.097872E-7
LINT  = 1.040878E-7
XW    = 0
DVG   = -1.983686E-8
VOFF  = -0.0823738
NFACCTOR = 0.969384
CDSC  = 2.4E-4
ETAO  = 0.4985496
ETAB  = -0.0653358
PCLM  = 2.1142057
PDIBLC1 = 0.0256688
PDIBLC2 = -0.0511673
PVAG  = 0
RSH   = 103.6
MOBMOD = 1
UTE   = -1.5
KT2   = 0.022
UA1   = 4.31E-9
UC1   = -5.6E-11
AT    = 3.3E4
WL    = 0
WL    = 1
WW    = 0
LL    = 0
LW    = 0
LLN   = 1
CAPMOD = 2
XPART = 0.5
CGSO  = 3.09E-10
CGBO  = 1E-9
PB    = 0.9665307
MJ    = 0.4978642
PWSW  = 0.99
MJSW  = 0.3877813
PWSWG = 0.99
MJSWG = 0.3877813
PVTHO = 5.98016E-3
PRDSW = 14.8598424
WKETA = 2.870507E-3
LKETA = -4.823171E-3
-```
Technology Files

• Design Rules

• Process Flow (Fabrication Technology) (will discuss next)

• Model Parameters (will discuss in substantially more detail after device operation and more advanced models are introduced)
Design Rules

- Give minimum feature sizes, spacing, and other constraints that are acceptable in a process

- Very large number of devices can be reliably made with the design rules of a process

- Yield and performance unpredictable and often low if rules are violated

- Compatible with design rule checker in integrated toolsets
Design Rules and **Layout** — consider transistors

![Diagram of transistor layout with labels for Drain (D), Gate (G), and Source (S)]

---

Layer Map

- **p-active**
- **n-active**
- **Poly 1**
- **Metal 1**
- **n-well**
- **contact**

---

Layout always represented in a top view in two dimensions
Design Rules and **Layout** — consider transistors

Layer Map

- p-active
- n-active
- Poly 1
- Metal 1
- n-well
- contact

Everything useful in channel region. **All other features just overhead that degrades performance**
Design rules give minimum feature sizes and spacings

Designers generally do layouts to minimize size of circuit subject to design rule constraints (because yield, cost, and performance usually improve)
Design Rules and Layout — consider transistors

- Bulk connection needed
- Single bulk connection can often be used for several (many) transistors
Design Rules and Layout – consider transistors

- Bulk connection needed
- Single bulk connection can often be used for several (many) transistors if they share the same well
Design Rules and Layout (example)

Logic Circuit

Circuit Schematic (Including Device Sizing)

Stick Diagram
Design Rules (example)

Layer Map

- Yellow: p-active
- Green: n-active
- Red: Poly 1
- Blue: Metal 1
- Brown: n-well
- Black: contact

A

V_{DD}

V_{SS} (GND)

A

Y

Y

Layout
Design Rules (example)

- Polygons merged in Geometric Description File (GDF)
- Separate rectangles generally more convenient to represent
Design Rules  (example)

• Design rules must be satisfied throughout the design
• DRC runs incrementally during layout in most existing tools to flag most problems
• DRC can catch layout errors but not circuit design errors
What is wrong with this layout?

Bulk connections missing!
Design Rules (example)

- Note diffusions needed for bulk connections
- Note p-well connections increase area a significant amount
- Note p-wells are both connected to $V_{DD}$ in this circuit

Actually 4-terminal device
Design Rules (example)

Layout with shared p-well reduces area
Design Rules (example)

Shared p-active can be combined to reduce area

Shared n-active can be combined to reduce area
Design Rules

• Design rules can be given in absolute dimensions for every rule

• Design rules can be parameterized and given relative to a parameter
  – Makes movement from one process to another more convenient
  – Easier for designer to remember
  – Some penalty in area efficiency
  – Often termed $\lambda$-based design rules
  – Typically $\lambda$ is $\frac{1}{2}$ the minimum feature size in a process
Design Rules

• See www.MOSIS.com for design rules
Fabrication

Design


Fabrication Schedule

Multi-Project Wafer Fabrication Schedule

Fabrication Processes

Fabrication Processes Available through MOSIS
Design
A variety of design flows (digital, analog, mixed-signal) can be used with a number of different CAD tools, technology files, design kits, libraries and IP to create designs for processes accessed by MOSIS.

Design Kits
Design kits (PKCs), technology files, etc. (see design kit summary) that support a variety of CAD tools, e.g. Cadence, Mentor, Synopsys and Tanner. Except where noted, these are distributed free of charge and are made available (other than austriamicrosystems) through our document server after signature of the MOSIS customer agreement and the vendor required agreements.

Design Rules
Vendor design rules, SPICE models, etc. are available for each process. MOSIS provides electrical test data and SPICE parameters from MOSIS measurements on most MPW (multiproject wafer) runs. Projects submitted to MOSIS for fabrication can be designed using either the vendor’s native design rules (specific to a process) or (for some processes) the SCMOS vendor-independent, scalable rules. These rule sets cannot be mixed within a design. SCMOS kits, cells and technology files are available.
Vendor and MOSIS SCMOS Design Rules
Projects submitted to MOSIS for fabrication can be designed using either vendor-independent, scalable rules (MOSIS SCMOS Rules), or design rules specific to a process.

Projects submitted to MOSIS for fabrication can be designed using either layout design rules specific to a process (vendor native rules) or (for some processes) vendor-independent, scalable rules (SCMOS rules). These rule sets cannot be mixed within a design.

Use SCMOS rules for portability and simplicity. Use vendor specific rules for fine-tuned layout.

Vendor Rules
Vendors consider their rules, process specifications, and SPICE parameters proprietary and make them available to MOSIS commercial account holders in different ways.

SCMOS Rules
MOSIS Scalable CMOS (SCMOS) is a set of logical layers together with their design rules, which provide a nearly process- and metric-independent interface to many CMOS fabrication processes available through MOSIS.
Design Rules

• See www.MOSIS.com for design rules

• Some of these files are on class WEB site
  – Mosis Rules Pictorial.pdf
### Table 2a: MOSIS SCMOS-Compatible Mappings

<table>
<thead>
<tr>
<th>Foundry</th>
<th>Process</th>
<th>Lambda (micro-meters)</th>
<th>Options</th>
</tr>
</thead>
<tbody>
<tr>
<td>ON Semi</td>
<td>C5F/N (0.5 micron n-well)</td>
<td>0.35</td>
<td>SCN3M, SCN3ME</td>
</tr>
<tr>
<td>TSMC</td>
<td>0.35 micron 2P4M (4 Metal Poly, 3.3 V/5 V)</td>
<td>0.25</td>
<td>SCN4ME</td>
</tr>
<tr>
<td>TSMC</td>
<td>0.35 micron 1P4M (4 Metal Silicided, 3.3 V/5 V)</td>
<td>0.25</td>
<td>SCN4M</td>
</tr>
</tbody>
</table>

### Table 2b: MOSIS SCMOS_SUBM-Compatible Mappings

<table>
<thead>
<tr>
<th>Foundry</th>
<th>Process</th>
<th>Lambda (micro-meters)</th>
<th>Options</th>
</tr>
</thead>
<tbody>
<tr>
<td>ON Semi</td>
<td>C5F/N (0.5 micron n-well)</td>
<td>0.30</td>
<td>SCN3M_SUBM, SCN3ME_SUBM</td>
</tr>
<tr>
<td>TSMC</td>
<td>0.35 micron 2P4M (4 Metal Poly, 3.3 V/5 V)</td>
<td>0.20</td>
<td>SCN4ME_SUBM</td>
</tr>
<tr>
<td>TSMC</td>
<td>0.35 micron 1P4M (4 Metal Silicided, 3.3 V/5 V)</td>
<td>0.20</td>
<td>SCN4M_SUBM</td>
</tr>
<tr>
<td>TSMC</td>
<td>0.25 micron 5 Metal 1 Poly (2.5 V/3.3 V)</td>
<td>0.15</td>
<td>SCN5M_SUBM</td>
</tr>
<tr>
<td>TSMC</td>
<td>0.18 micron 6 Metal 1 Poly (1.8 V/3.3 V)</td>
<td>0.10</td>
<td>SCN6M_SUBM</td>
</tr>
</tbody>
</table>

### Table 2c: MOSIS SCMOS_DEEP-Compatible Mappings

<table>
<thead>
<tr>
<th>Foundry</th>
<th>Process</th>
<th>Lambda (micro-meters)</th>
<th>Options</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSMC</td>
<td>0.25 micron 5 Metal 1 Poly (2.5 V/3.3 V)</td>
<td>0.12</td>
<td>SCN5M_DEEP</td>
</tr>
<tr>
<td>TSMC</td>
<td>0.18 micron 6 Metal 1 Poly (1.8 V/3.3 V)</td>
<td>0.09</td>
<td>SCN6M_DEEP</td>
</tr>
</tbody>
</table>
2.1. Well Type

The Scalable CMOS (SC) rules support both $n$-well and $p$-well processes. MOSIS recognizes three base technology codes that let the designer specify the well type of the process selected. SCN specifies an $n$-well process, SCP specifies a $p$-well process, and SCE indicates that the designer is willing to utilize a process of either $n$-well or $p$-well.

An SCE design must provide both a drawn $n$-well and a drawn $p$-well; MOSIS will use the well that corresponds to the selected process and ignore the other well. As a convenience, SCN and SCP designs may also include the other well ($p$-well in an SCN design or $n$-well in an SCP design), but it will always be ignored.

MOSIS currently offers only $n$-well processes or foundry-designated twin-well processes that from the design and process flow standpoints are equivalent to $n$-well processes. These twin-well processes may have options (deep $n$-well) that provide independently isolated $p$-wells. For all of these processes at this time use the technology code SCN. SCP is currently not supported, and SCE is treated exactly as SCN.
2.2. SCMOS Options

SCMOS options are used to designate projects that use additional layers beyond the standard single-poly, double metal CMOS. Each option is called out with a designator that is appended to the basic technology-code. Please note that not all possible combinations are available. The current list is shown in Table 1.

MOSIS has not issued SCMOS design rules for some vendor-supported options. For example, any designer using the SCMOS rules who wants the TSMC Thick_Top_Metal must draw the top metal to comply with the TSMC rules for that layer. Questions about other non-SCMOS layers should be directed to support@moss.com.

<table>
<thead>
<tr>
<th>Designation</th>
<th>Long Form</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>E</td>
<td>Electrode</td>
<td>Adds a second polysilicon layer (poly2) that can serve either as the upper electrode of a poly capacitor or (1.5 micron only) as a gate for transistors</td>
</tr>
<tr>
<td>A</td>
<td>Analog</td>
<td>Adds electrode (as in E option), plus layers for vertical NPN transistor pbase</td>
</tr>
<tr>
<td>3M</td>
<td>3 Metal</td>
<td>Adds second via (via2) and third metal (metal3) layers</td>
</tr>
<tr>
<td>4M</td>
<td>4 Metal</td>
<td>Adds 3M plus third via (via3) and fourth metal (metal4) layers</td>
</tr>
<tr>
<td>5M</td>
<td>5 Metal</td>
<td>Adds 4M plus fourth via (via4) and fifth metal (metal5) layers</td>
</tr>
<tr>
<td>6M</td>
<td>6 Metal</td>
<td>Adds 5M plus fifth via (via5) and sixth metal (metal6) layers</td>
</tr>
<tr>
<td>LC</td>
<td>Linear Capacitor</td>
<td>Adds a cap_well layer for linear capacitors</td>
</tr>
<tr>
<td>PC</td>
<td>Poly Cap</td>
<td>Adds poly_cap, a different layer for linear capacitors</td>
</tr>
<tr>
<td>SUBM</td>
<td>Sub-Micron</td>
<td>Uses revised layout rules for better fit to sub-micron processes (see section 2.4)</td>
</tr>
<tr>
<td>DEEP</td>
<td>Deep</td>
<td>Uses revised layout rules for better fit to deep sub-micron processes (see section 2.4)</td>
</tr>
<tr>
<td>Technology code with link to layer map</td>
<td>Layers</td>
<td></td>
</tr>
<tr>
<td>--------------------------------------</td>
<td>---------------------------------------------</td>
<td></td>
</tr>
<tr>
<td>SCNE</td>
<td>N_well, Active, N_select, P_select, Poly, Poly2, Contact, Metal1, Via, Metal2, Glass</td>
<td></td>
</tr>
<tr>
<td>SCNA</td>
<td>N_well, Active, N_select, P_select, Poly, Poly2, Contact, Pbase, Metal1, Via, Metal2, Glass</td>
<td></td>
</tr>
<tr>
<td>SCNPC</td>
<td>N_well, Active, N_select, P_select, Poly_cap, Poly, Contact, Metal1, Via, Metal2, Glass</td>
<td></td>
</tr>
<tr>
<td>SCN3M</td>
<td>N_well, Active, N_select, P_select, Poly, Silicde block (Agilent/HP only), Hi_Res_Implant, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass</td>
<td></td>
</tr>
<tr>
<td>SCN3ME</td>
<td>N_well, Active, N_select, P_select, Poly, Poly2, Hi_Res_Implant, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass</td>
<td></td>
</tr>
<tr>
<td>Technology code with link to layer map</td>
<td>Layers</td>
<td></td>
</tr>
<tr>
<td>--------------------------------------</td>
<td>--------</td>
<td></td>
</tr>
<tr>
<td>SCNE</td>
<td>N_well, Active, N_select, P_select, Poly, Poly2, Contact, Metal1, Via, Metal2, Glass</td>
<td></td>
</tr>
<tr>
<td>SCNA</td>
<td>N_well, Active, N_select, P_select, Poly, Poly2, Contact, Pbase, Metal1, Via, Metal2, Glass</td>
<td></td>
</tr>
<tr>
<td>SCNPC</td>
<td>N_well, Active, N_select, P_select, Poly_cap, Poly, Contact, Metal1, Via, Metal2, Glass</td>
<td></td>
</tr>
<tr>
<td>SCN3M</td>
<td>N_well, Active, N_select, P_select, Poly, Silicide block (Agilent/HP only), Hi_Res_Implant, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass</td>
<td></td>
</tr>
<tr>
<td>SCN3ME</td>
<td>N_well, Active, N_select, P_select, Poly, Poly2, Hi_Res_Implant, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass</td>
<td></td>
</tr>
</tbody>
</table>
### SCMOS Layout Rules - Well

<table>
<thead>
<tr>
<th>Rule</th>
<th>Description</th>
<th>Lambda</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.1</td>
<td>Minimum width</td>
<td>10</td>
</tr>
<tr>
<td>1.2</td>
<td>Minimum spacing between wells at different potential</td>
<td>9</td>
</tr>
<tr>
<td></td>
<td></td>
<td>18</td>
</tr>
<tr>
<td></td>
<td></td>
<td>18</td>
</tr>
<tr>
<td>1.3</td>
<td>Minimum spacing between wells at same potential</td>
<td>6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>6</td>
</tr>
<tr>
<td>1.4</td>
<td>Minimum spacing between wells of different type (if both are drawn)</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0</td>
</tr>
</tbody>
</table>

**Lambda Values:**
- SCMOS: 10, 9, 6, 0
- SUBM: 12, 18, 6, 0
- DEEP: 12, 18, 6, 0

**Exceptions for AMIS C30 0.35 micron process:**

1. Use \( \lambda = 16 \) for rule 1.2 only when using SCN4M or SCN4ME
2. Use \( \lambda = 21 \) for rule 1.2 only when using SCN4M_SUBM or SCN4ME_SUBM
3. Use \( \lambda = 8 \) for rule 1.3 only when using SCN4M or SCN4ME
4. Use \( \lambda = 11 \) for rule 1.3 only when using SCN4M_SUBM or SCN4ME_SUBM

![Diagram showing well spacing rules](image-url)
<table>
<thead>
<tr>
<th>Technology code with link to layer map</th>
<th>Layers</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCNE</td>
<td>N_well, Active, N_select, P_select, Poly, Poly2, Contact, Metal1, Via, Metal2, Glass</td>
</tr>
<tr>
<td>SCNA</td>
<td>N_well, Active, N_select, P_select, Poly, Poly2, Contact, Pbase, Metal1, Via, Metal2, Glass</td>
</tr>
<tr>
<td>SCNPC</td>
<td>N_well, Active, N_select, P_select, Poly_cap, Poly, Contact, Metal1, Via, Metal2, Glass</td>
</tr>
<tr>
<td>SCN3M</td>
<td>N_well, Active, N_select, P_select, Poly, Silicide block (Agilent/HP only), Hi_Res_Impant, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass</td>
</tr>
<tr>
<td>SCN3ME</td>
<td>N_well, Active, N_select, P_select, Poly, Poly2, Hi_Res_Impant, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass</td>
</tr>
</tbody>
</table>
2.1 Minimum width
2.2 Minimum spacing
2.3 Source/drain active to well edge
2.4 Substrate/well contact active to well edge
2.5 Minimum spacing between non-abutting active of different implant. Abutting active ("split-active") is illustrated under Select Layout Rules.

* Note: For analog and critical digital designs, MOSIS recommends the following minimum MOS channel widths (active under poly) for AMIS designs. Narrower devices, down to design rule minimum, will be functional, but their electrical characteristics will not scale, and their performance is not predictable from MOSIS SPICE parameters.

<table>
<thead>
<tr>
<th>Process</th>
<th>Design Technology</th>
<th>Design Lambda (micrometers)</th>
<th>Minimum Width (lambda)</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMI_AB</td>
<td>SCNA, SCNE</td>
<td>0.80</td>
<td>5</td>
</tr>
<tr>
<td>AMI_C5F/N</td>
<td>SCN3M, SCN3ME</td>
<td>0.35</td>
<td>9</td>
</tr>
<tr>
<td>AMI_C5F/N</td>
<td>SCN3M_SUBM, SCN3ME_SUBM</td>
<td>0.30</td>
<td>10</td>
</tr>
<tr>
<td>Technology code with link to layer map</td>
<td>Layers</td>
<td></td>
<td></td>
</tr>
<tr>
<td>--------------------------------------</td>
<td>------------------------------------------------------------------------</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SCNE</td>
<td>N_well, Active, N_select, P_select, Poly, Poly2, Contact, Metal1, Via, Metal2, Glass</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SCNA</td>
<td>N_well, Active, N_select, P_select, Poly, Poly2, Contact, Pbase, Metal1, Via, Metal2, Glass</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SCNPC</td>
<td>N_well, Active, N_select, P_select, Poly_cap, Poly, Contact, Metal1, Via, Metal2, Glass</td>
<td></td>
<td></td>
</tr>
<tr>
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<td></td>
</tr>
<tr>
<td>SCN3ME</td>
<td>N_well, Active, N_select, P_select, Poly, Poly2, Hi_Res_Implant, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
## SCMOS Layout Rules - Poly

<table>
<thead>
<tr>
<th>Rule</th>
<th>Description</th>
<th>Lambda</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>SCMOS</td>
</tr>
<tr>
<td>3.1</td>
<td>Minimum width</td>
<td>2</td>
</tr>
<tr>
<td>3.2</td>
<td>Minimum spacing over field</td>
<td>2</td>
</tr>
<tr>
<td>3.2.a</td>
<td>Minimum spacing over active</td>
<td>2</td>
</tr>
<tr>
<td>3.3</td>
<td>Minimum gate extension of active</td>
<td>2</td>
</tr>
<tr>
<td>3.4</td>
<td>Minimum active extension of poly</td>
<td>3</td>
</tr>
<tr>
<td>3.5</td>
<td>Minimum field poly to active</td>
<td>1</td>
</tr>
</tbody>
</table>

[Diagram showing Poly and Active layers with rule annotations 3.1, 3.2, 3.3, 3.4, and 3.5.]
<table>
<thead>
<tr>
<th>Technology code with link to layer map</th>
<th>Layers</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCNE</td>
<td>N_well, Active, N_select, P_select, Poly, Poly2, Contact, Metal1, Via, Metal2, Glass</td>
</tr>
<tr>
<td>SCNA</td>
<td>N_well, Active, N_select, P_select, Poly, Poly2, Contact, Pbase, Metal1, Via, Metal2, Glass</td>
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<td>SCNPC</td>
<td>N_well, Active, N_select, P_select, Poly_cap, Poly, Contact, Metal1, Via, Metal2, Glass</td>
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<td>SCN3ME</td>
<td>N_well, Active, N_select, P_select, Poly, Poly2, Hi_Res_Implant, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass</td>
</tr>
<tr>
<td>Rule</td>
<td>Description</td>
</tr>
<tr>
<td>------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>4.1</td>
<td>Minimum select spacing to channel of transistor to ensure adequate source/drain width</td>
</tr>
<tr>
<td>4.2</td>
<td>Minimum select overlap of active</td>
</tr>
<tr>
<td>4.3</td>
<td>Minimum select overlap of contact</td>
</tr>
<tr>
<td>4.4</td>
<td>Minimum select width and spacing (Note: P-select and N-select may be coincident, but must not overlap) (not illustrated)</td>
</tr>
</tbody>
</table>

*The same rules apply with N+ Select and P+ Select reversed.*
Technology Files

• Design Rules

Process Flow (Fabrication Technology)

• Model Parameters (will discuss in substantially more detail after device operation and more advanced models are introduced)
IC Fabrication Technology

See Chapter 3 and a little of Chapter 1 of WH
or Chapter 2 GAS for details
IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Etching
- Diffusion
- Oxidation
- Epitaxy
- Polysilicon
- Contacts, Interconnect and Metalization
- Planarization
MOS Transistor

n-type
n+-type
p-type
p+-type
SiO2 (insulator)
POLY (conductor)

Review

A' A

Gate
Source
Drain

Bulk

n-channel MOSFET
MOS Transistor

A
Source
Gate
Drain
A'
Bulk

n-type
n+-type
p-type
p+-type
SiO2 (insulator)
POLY (conductor)

n-type
n+-type
p-type
p+-type
SiO2 (insulator)
POLY (conductor)

p-channel MOSFET

Review
n-channel MOS transistor in Bulk CMOS n-well process with bulk contact

p-substrate serves as the BULK for n-channel devices
MOS Transistor

p-channel MOS transistor in Bulk CMOS n-well process with bulk contact and well (tub)

Serves as the BULK for p-channel device
MOS Transistor

• Single-crystalline silicon
  - Serves as physical support member
  - Lightly doped
  - Vertical dimensions are not linearly depicted
  - Often termed the Bulk

n-channel MOSFET
MOS Transistor

- **Single-crystalline silicon**
  - Serves as physical support member
  - Lightly doped
  - Vertical dimensions are not linearly depicted
  - Often termed the BULK
MOS Transistor

- **Single-crystalline silicon**
  - Serves as physical support member
  - Lightly doped (p-doping in the $10^{15}/\text{cm}^3$ range, silicon in the $2.2\times10^{22}/\text{cm}^3$ range)
  - Vertical dimensions are not linearly depicted
  - Often termed the BULK

- **Conductor (usually polysilicon)**
  - More heavily doped ($10^{17}/\text{cm}^3$ range)

- **Thin insulator**
  - (10A to 50A range)
p-channel MOSFET

Lightly-doped n-type (5x10^{16}/cm^3 range)

More heavily-doped p-type (10^{18}/cm^3 range)

Lightly doped p-type (10^{15}/cm^3 range)

Bulk
Crystal Preparation

• Large crystal is grown (pulled)
  – 12 inches (300mm) in diameter and 1 to 2 m long
  – Sliced to 250μm to 500μm thick
    • Prefer to be much thinner but thickness needed for mechanical integrity
  – 4 to 8 cm/hr pull rate
  – T=1430 °C

• Crystal is sliced to form wafers
• Cost for 12” wafer around $200
• 5 companies provide 90% of worlds wafers
• Somewhere around 400,000 12in wafers/month
Crystal Preparation

Some predict newer FABs to be at 450mm (18in) by 2020 but uncertain whether it will happen.

Lightly-doped silicon
Excellent crystalline structure
Crystal Preparation
Crystal Preparation
Crystal Preparation

Source: WEB
Crystal Preparation

Source: WEB
Crystal Preparation

A section of 300mm ingot is loaded into a wiresaw

Source: WEB
Crystal Preparation
End of Lecture 7
Masking

- Use masks or reticles to define features on a wafer
  - Masks same size as wafer
  - Reticles used for projection
  - Reticle much smaller (but often termed mask)
  - Reticles often of quartz with chrome
  - Quality of reticle throughout life of use is critical
  - Single IC may require 20 or more reticles
  - Cost of “mask set” now exceeds $1million for state of the art processes
  - Average usage 500 to 1500 times
  - Mask costs exceeding 50% of total fabrication costs in sub 100nm processes
  - Serve same purpose as a negative (or positive) in a photographic process
  - Usually use 4X optical reduction - exposure area approx. 860mm²
    (now through 2022 ITRS 2007 litho, Table LITH3a)
Step and Repeat (stepper) used to image across wafer
Masking

Exposure through reticle
Masking

Mask Features Intentionally Distorted to Compensated For Wavelength Limitations in Small Features
IC Fabrication Technology

- Crystal Preparation
- Masking

*Photolithographic Process*
- Deposition
- Etching
- Diffusion
- Oxidation
- Epitaxy
- Polysilicon
- Contacts, Interconnect and Metalization
- Planarization
Photolithographic Process

• Photoresist
  – Viscous Liquid
  – Uniform Application Critical (spinner)
  – Baked to harden
  – Approx 1μ thick
  – Non-Selective
  – Types
    • Negative – unexposed material removed when developed
    • Positive-exposed material removed when developed
    • Thickness about 450nm in 90nm process (ITRS 2007 Litho)

• Exposure
  – Projection through reticle with stepper (scanners becoming popular)
  – Alignment is critical !!
  – E-Bean Exposures
    • Eliminate need from reticle
    • Capacity very small

Stepper: Optics fixed, wafer steps in fixed increments
Scanner: Wafer steps in fixed increments and during exposure both optics and wafer are moved to increase effective reticle size
Steppers

Stepper costs in the $10M range with thru-put of around 100 wafers/hour.
Steppers
Mask Alignment

Correctly Aligned
Mask Alignment

Alignment Errors

\[ \Delta X \quad \Delta Y \]
Mask Alignment

Other alignment marks  (http://www.mems-exchange.org/users/masks/intro-equipment.html)
IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Implantation
- Etching
- Diffusion
- Oxidation
- Epitaxy
- Polysilicon
- Contacts, Interconnect and Metalization
- Planarization
Deposition

• Application of something to the surface of the silicon wafer or substrate
  – Layers 15A to 20u thick

• Methods
  – Physical Vapor Deposition (nonselective)
    • Evaporation/Condensation
    • Sputtering (better host integrity)
  – Chemical Vapor Deposition (nonselective)
    • Reaction of 2 or more gases with solid precipitate
    • Reduction by heating creates solid precipitate (pyrolytic)
  – Screening (selective)
    • For thick films
    • Low Tech, not widely used today
Deposition

Example: Chemical Vapor Deposition

Silane (SiH₄) is a gas (toxic and spontaneously combustible in air) at room temperature but breaks down into Si and H₂ above 400°C so can be used to deposit Si.

\[
\text{SiH}_4 \rightarrow \text{Si} + 2\text{H}_2
\]
IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Implantation
- Etching
- Diffusion
- Oxidation
- Epitaxy
- Polysilicon
- Contacts, Interconnect and Metalization
- Planarization
Implantation

Application of impurities into the surface of the silicon wafer or substrate
- Individual atoms are first ionized (so they can be accelerated)
- Impinge on the surface and burry themselves into the upper layers
- Often very shallow but with high enough energy can go modestly deep
- Causes damage to target on impact
- Annealing heals most of the damage
- Very precise control of impurity numbers is possible
- Very high energy required
- High-end implanters considered key technology for national security
Ion Implantation Process

From http://www.casetechnology.com/implanter
Ion Implantation Process

From http://www.casetechnology.com/implanter
Ion Implanter

From http://www.casetechnology.com/implanter
IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Implantation
- Etching
- Diffusion
- Oxidation
- Epitaxy
- Polysilicon
- Contacts, Interconnect and Metalization
- Planarization
Etching

Selective Removal of Unwanted Materials

- Wet Etch
  - Inexpensive but under-cutting a problem

- Dry Etch
  - Often termed ion etch or plasma etch
Desired Physical Features

Note: Vertical Dimensions Generally Orders of Magnitude Smaller Than Lateral Dimensions so Different Vertical and Lateral Scales Will be Used In This Discussion
Etching

Dry etch (anisotropic)

SiO₂

Photoresist

p⁻ Silicon

Desired Physical Features

Dry Etch can provide very well-defined and nearly vertical edges (relative to photoresist patterning)
Etching (limited by photolithographic process)

Dry etch (anisotropic)  Photoresist

SiO₂  p⁻ Silicon  Dry etch (anisotropic)

Consider neg photoresist

Over Exposed  Correctly Developed  Over Developed  Under Developed

Under Exposed  Correctly Developed  Over Developed  Under Developed
For Example, the wafer thickness is around 250μ and the gate oxide is around 50Å (5E-3μ) and diffusion depths are around λ/5.
Etching

**SiO$_2$**

- Undercutting (wet etch)
- Desired Edges of SiO$_2$ from Mask
- Edge Movement Due to Over Etch, Over Exposure, or Over-Development

**p$^-$ Silicon**

**Isotropic Feature Degradation**

**Photoresist**
Etching

Undercutting (wet etch)

Desired Edges of SiO$_2$ from Mask

SiO$_2$ after photoresist removal

Edge Movement Due to Over Etch, Over Exposure, or Over-Development
IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Ion Implantation
- Etching
- Diffusion
- Oxidation
- Epitaxy
- Polysilicon
- Contacts, Interconnect and Metalization
- Planarization
Diffusion

- Controlled Migration of Impurities
  - Time and Temperature Dependent
  - Both vertical and lateral diffusion occurs
  - Crystal orientation affects diffusion rates in lateral and vertical dimensions
  - Materials Dependent
  - Subsequent Movement
  - Electrical Properties Highly Dependent upon Number and Distribution of Impurities
  - Diffusion at 800°C to 1200°C

- Source of Impurities
  - Deposition
  - Ion Implantation
    - Only a few Å deep
    - More accurate control of doping levels
    - Fractures silicon crystalline structure during implant
    - Annealing occurs during diffusion

- Types of Impurities
  - n-type Arsenic, Antimony, Phosphorous
  - p-type Gallium, Aluminum, Boron