Quiz 7

The layout of the cascade of two CMOS inverters is shown. It has some layout errors. Identify them.
And the number is ....
And the number is ....
Quiz 7 Solution:

- Bulk Connection on P-well is missing
- Poly from first gate is shorted to poly from second gate (circuit error, not DRC)
Quiz 7 solution:

- Corrected Circuit
Technology Files

• Provide Information About Process
  – Process Flow (Fabrication Technology)
  – Model Parameters
  – Design Rules

• Serve as Interface Between Design Engineer and Process Engineer

• Insist on getting information that is deemed important for a design
  – Limited information available in academia
  – Foundries often sensitive to who gets access to information
  – Customer success and satisfaction is critical to foundries
Design Rules and Layout – consider transistors

Review from Last Time

Layer Map
- p-active
- n-active
- Poly 1
- Metal 1
- n-well
- contact

- Bulk connection needed
- Single bulk connection can often be used for several (many) transistors
Design Rules and Layout – consider transistors

• Bulk connection needed
• Single bulk connection can often be used for several (many) transistors if they share the same well
Design Rules

• Design rules can be given in absolute dimensions for every rule

• Design rules can be parameterized and given relative to a parameter
  – Makes movement from one process to another more convenient
  – Easier for designer to remember
  – Some penalty in area efficiency
  – Often termed $\lambda$-based design rules
  – Typically $\lambda$ is $\frac{1}{2}$ the minimum feature size in a process
Review from Last Time

### SCMOS Layout Rules - Poly

<table>
<thead>
<tr>
<th>Rule</th>
<th>Description</th>
<th>Lambda</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>SCMOS</td>
</tr>
<tr>
<td>3.1</td>
<td>Minimum width</td>
<td>2</td>
</tr>
<tr>
<td>3.2</td>
<td>Minimum spacing over field</td>
<td>2</td>
</tr>
<tr>
<td>3.2.a</td>
<td>Minimum spacing over active</td>
<td>2</td>
</tr>
<tr>
<td>3.3</td>
<td>Minimum gate extension of active</td>
<td>2</td>
</tr>
<tr>
<td>3.4</td>
<td>Minimum active extension of poly</td>
<td>3</td>
</tr>
<tr>
<td>3.5</td>
<td>Minimum field poly to active</td>
<td>1</td>
</tr>
</tbody>
</table>

![Diagram of SCMOS Layout Rules - Poly](image)
Technology Files

• Design Rules

Process Flow (Fabrication Technology)

• Model Parameters (will discuss in substantially more detail after device operation and more advanced models are introduced)
IC Fabrication Technology

See Chapter 3 and a little of Chapter 1 of WH
or Chapter 2 GAS for details
Generic Process Flow
IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Etching
- Diffusion
- Oxidation
- Epitaxy
- Polysilicon
- Contacts, Interconnect and Metalization
- Planarization
MOS Transistor

n-channel MOSFET
MOS Transistor

p-channel MOSFET

Bulk

Source

Gate

Drain

Review
n-channel MOS transistor in Bulk CMOS n-well process with bulk contact
p-channel MOS transistor in Bulk CMOS n-well process with bulk contact and well (tub)
MOS Transistor

- Single-crystalline silicon
  - Serves as physical support member
  - Lightly doped
  - Vertical dimensions are not linearly depicted
MOS Transistor

- Single-crystalline silicon
  - Serves as physical support member
  - Lightly doped
  - Vertical dimensions are not linearly depicted
MOS Transistor

- Single-crystalline silicon
  - Serves as physical support member
  - Lightly doped (p-doping in the $10^{15}/\text{cm}^3$ range, silicon in the $2.2\times10^{22}/\text{cm}^3$ range)
  - Vertical dimensions are not linearly depicted
MOS Transistor

- Lightly-doped n-type (5x10^{16}/cm^{3} range)
- More heavily-doped p-type (10^{18}/cm^{3} range)
- Lightly doped p-type (10^{15}/cm^{3} range)
- p-channel MOSFET

Bulk

Source

Gate

Drain
Crystal Preparation

• Large crystal is grown (pulled)
  – 12 inches in diameter and 1 to 2 m long
  – Sliced to 250μ to 500μ thick
    • Prefer to be much thinner but thickness needed for mechanical integrity
  – 4 to 8 cm/hr pull rate
  – T=1430 °C

• Crystal is sliced to form wafers
• Cost for 12” wafer around $200
• 5 companies provide 90% of worlds wafers
• Somewhere around 400,000 12in wafers/month
Crystal Preparation

Lightly-doped silicon
Excellent crystalline structure

To go to 450mm (18in) by 2010
(ITRS 2007 FEP page 3)
Crystal Preparation

From www.infras.com
Crystal Preparation
Crystal Preparation

Source: WEB
Crystal Preparation

Source: WEB
Crystal Preparation

A section of 300mm ingot is loaded into a wire saw

Source: WEB
Crystal Preparation
IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Etching
- Diffusion
- Oxidation
- Epitaxy
- Polysilicon
- Contacts, Interconnect and Metalization
- Planarization
Masking

- Use masks or reticles to define features on a wafer
  - Masks same size as wafer
  - Reticles used for projection
  - Reticle much smaller (but often termed mask)
  - Reticles often of quartz with chrome
  - Quality of reticle throughout life of use is critical
  - Single IC may require 20 or more reticles
  - Cost of “mask set” now exceeds $1 million for state of the art processes
  - Average usage 500 to 1500 times
  - Mask costs exceeding 50% of total fabrication costs in sub 100nm processes
  - Serve same purpose as a negative (or positive) in a photographic process
  - Usually use 4X optical reduction - exposure area approx. 860 mm²

  (now through 2022 ITRS 2007 litho, Table LITH3a)
Masking

Step and Repeat (stepper) used to image across wafer
Masking

Exposure through reticle
Masking

Mask Features
Masking

Mask Features Intentionally Distorted to Compensate For Wavelength Limitations in Small Features
IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
  - Deposition
  - Etching
  - Diffusion
  - Oxidation
  - Epitaxy
  - Polysilicon
  - Contacts, Interconnect and Metalization
- Planarization
Photolithographic Process

• Photoresist
  – Viscous Liquid
  – Uniform Application Critical (spinner)
  – Baked to harden
  – Approx 1u thick
  – Non-Selective
  – Types
    • Negative – unexposed material removed when developed
    • Positive-exposed material removed when developed
    • Thickness about 450nm in 90nm process (ITRS 2007 Litho)

• Exposure
  – Projection through reticle with stepper
  – Alignment is critical !!
  – E-Bean Exposures
    • Eliminate need fro reticle
    • Capacity very small
Mask Alignment

Correctly Aligned
Mask Alignment

Alignment Errors

ΔX

ΔY
IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Implantation
- Etching
- Diffusion
- Oxidation
- Epitaxy
- Polysilicon
- Contacts, Interconnect and Metalization
- Planarization
Deposition

• Application of something to the surface of the silicon wafer or substrate
  – Layers 15A to 20u thick
• Methods
  – Physical Vapor Deposition (nonselective)
    • Evaporation/Condensation
    • Sputtering (better host integrity)
  – Chemical Vapor Deposition (nonselective)
    • Reaction of 2 or more gases with solid precipitate
    • Reduction by heating creates solid precipitate (pyrolytic)
  – Screening (selective)
    • For thick films
    • Low Tech, not widely used today
End of Lecture 8