# EE 330
# Lecture 8

Design Rules

IC Fabrication Technology Part 1

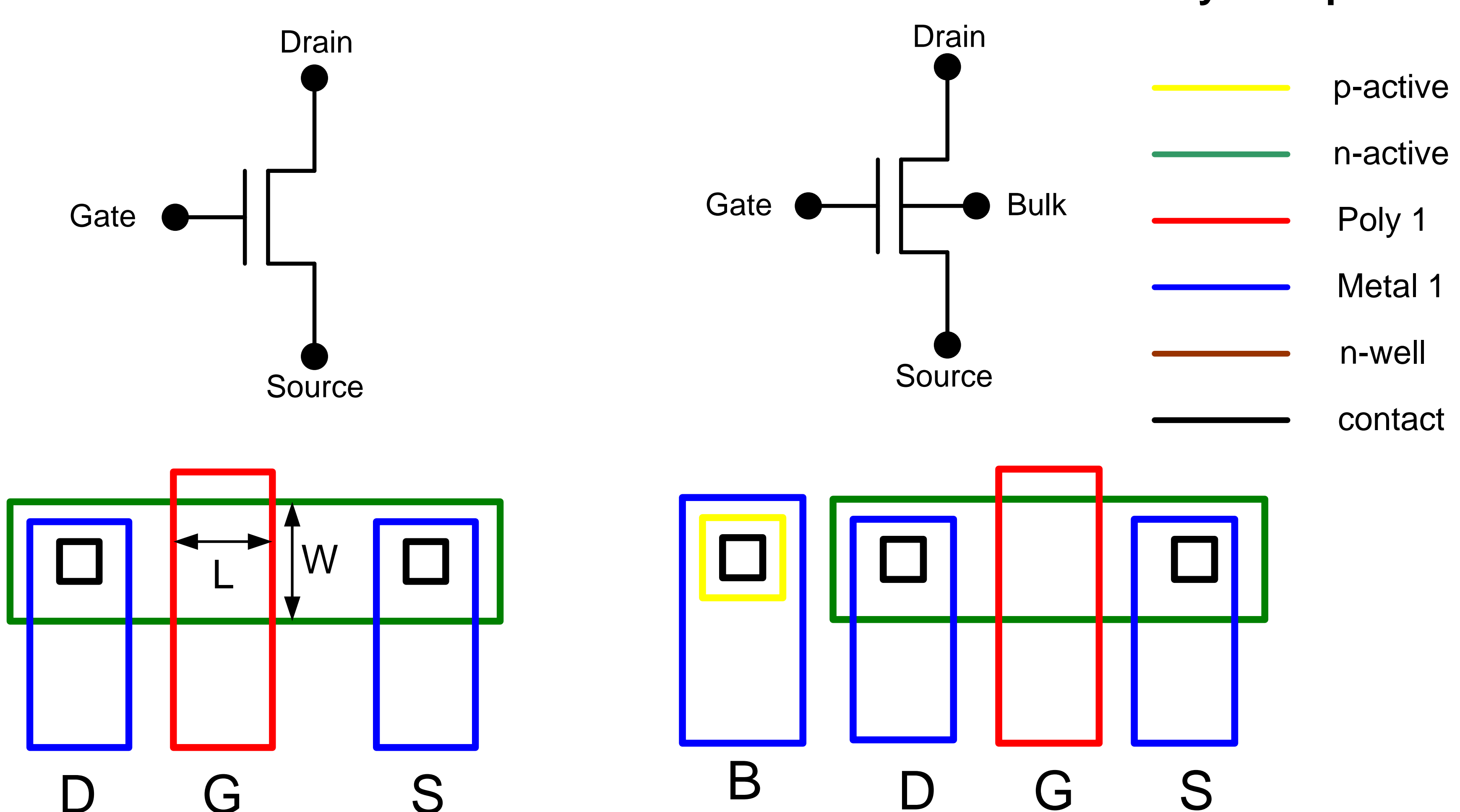
**Review from Last Time**

# Technology Files

- Provide Information About Process
  - Process Flow (Fabrication Technology)
  - Model Parameters
  - Design Rules
- Serve as Interface Between Design Engineer and Process Engineer
- Insist on getting information that is deemed important for a design
  - Limited information available in academia
  - Foundries often sensitive to who gets access to information
  - Customer success and satisfaction is critical to foundries

Review from Last Time

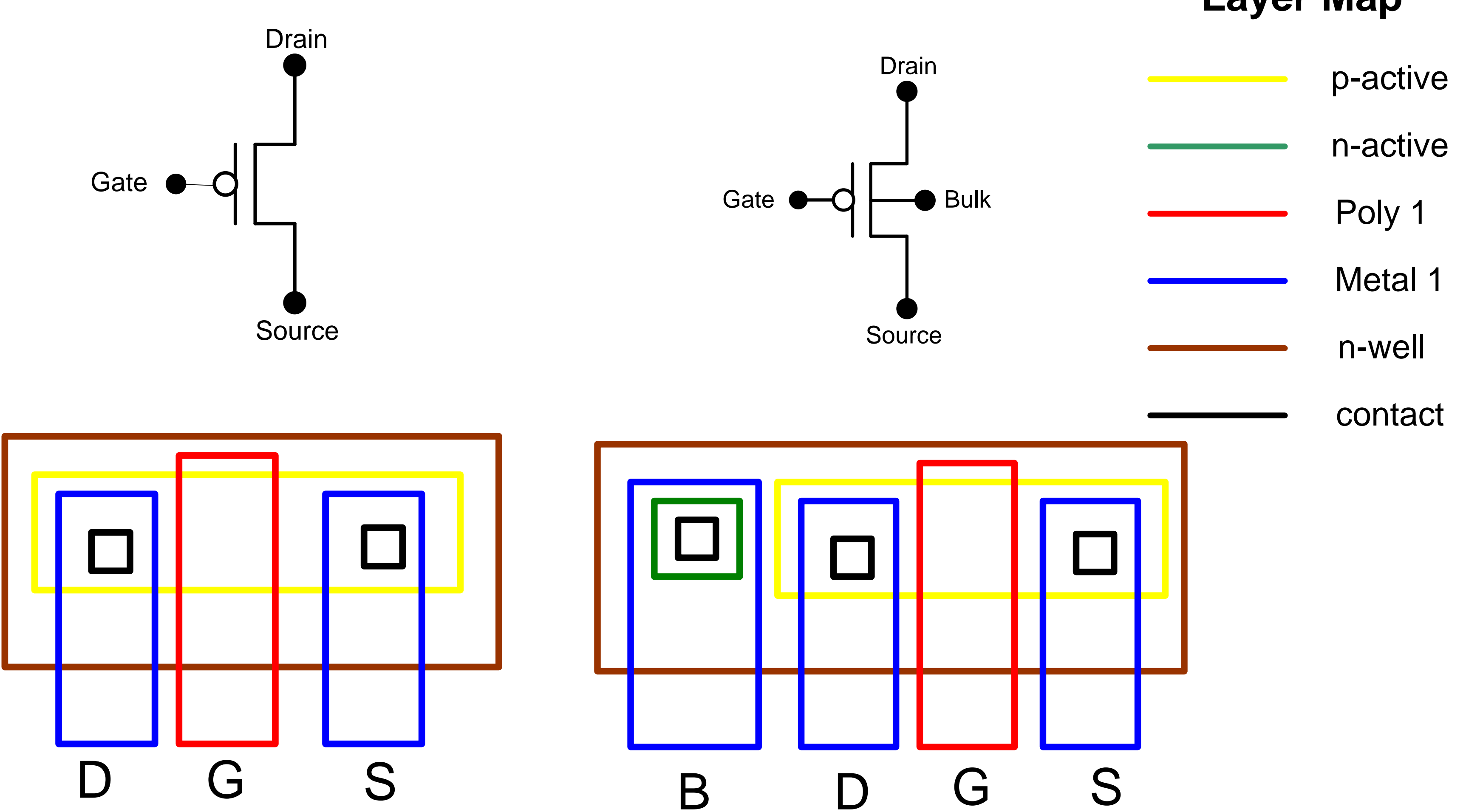
# Design Rules and Layout – consider transistors




- **Bulk connection needed**
- **Single bulk connection can often be used for several (many) transistors**

Review from Last Time

# Design Rules and Layout – consider transistors




- **Bulk connection needed**
- **Single bulk connection can often be used for several (many) transistors is they share the same well**

Review from Last Time

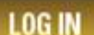
# Design Rules

- Design rules can be given in absolute dimensions for every rule
- Design rules can be parameterized and given relative to a parameter
  - Makes movement from one process to another more convenient
  - Easier for designer to remember
  - Some penalty in area efficiency
  - Often termed λ-based design rules
  - Typically λ is ½ the minimum feature size in a process

# Design Rules

- See www.MOSIS.com for design rules

The MOSIS Service



LOG IN

Google™ Custom Search | Search

About Us You Are Products Requests Support

microelectronics fabrication

Production Solutions for IC Innovation

| About Us | You Are | Products | Requests | Support |
|---|---|---|---|---|
| What is MOSIS | Buyer | IC Fabrication | Orders | Online Support |
| Events | IC Designer | Fab Processes | MOSIS Documents | Contact Us |
| Announcements | New MOSIS User | Fab Schedule | Design Submission | MOSIS User Group |
| Job Openings | Experienced User | Assembly | MOSIS Web Forms | |
| | Academic Institutions | Prices/Quotes | Test Data | |
| | Other | Run Status | | |

Multi-Project Wafers, making IC Fabrication affordable since 1981

The MOSIS Service

LOG IN

Google™ Custom Search | Search

About Us | You Are | Products | Requests | Support

IC Fabrication | Fab Processes | Fab Schedule | Assembly | Prices/Quotes | Run Status

Products > IC Fabrication

# Fabrication

## Design

Design Flows, Design Kits and Design Rules.

## Fabrication Schedule

Multi-Project Wafer Fabrication Schedule

## Fabrication Processes

Fabrication Processes Available through MOSIS

### Related Resources

- MOSIS Fabrication Schedule
- Customer Support
- MOSIS Products

# Design

A variety of design flows (digital, analog, mixed-signal) can be used with a number of different CAD tools, technology files, design kits, libraries and IP to create designs for processes accessed by MOSIS.

## Design Kits

Design kits (PDKs), technology files, etc. (see design kit summary) that support a variety of CAD tools, e.g. Cadence, Mentor, Synopsys and Tanner. Except where noted, these are distributed free of charge and are made available (other than austriamicrosystems) through our document server after signature of the MOSIS customer agreement and the vendor required agreements.

## Design Rules

Vendor design rules, SPICE models, etc. are available for each process. MOSIS provides electrical test data and SPICE parameters from MOSIS measurements on most MPW (multiproject wafer) runs. Projects submitted to MOSIS for fabrication can be designed using either the vendor's native design rules (specific to a process) or (for some processes) the SCMOS vendor-independent, scalable rules. These rule sets cannot be mixed within a design. SCMOS kits, cells and technology files are available.

### Related Resources

- Vendor Native-Rule Design Kits
- SCMOS Rule Design Kits
- Design Submission Procedures
- Fabrication Processes

The MOSIS Service

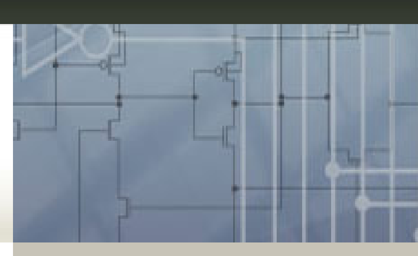
LOG IN

Search

About Us You Are Products Requests Support

# Vendor and MOSIS SCMOS Design Rules

Projects submitted to MOSIS for fabrication can be designed using either vendor-independent, scalable rules (MOSIS SCMOS Rules), or design rules specific to a process.



Projects submitted to MOSIS for fabrication can be designed using either layout design rules specific to a process (vendor native rules) or (for some processes) vendor-independent, scalable rules (SCMOS rules). These rule sets cannot be mixed within a design.

Use SCMOS rules for portability and simplicity. Use vendor specific rules for fine-tuned layout.

## Vendor Rules

Vendors consider their rules, process specifications, and SPICE parameters proprietary and make them available to MOSIS commercial account holders in different ways.

## SCMOS Rules

MOSIS Scalable CMOS (SCMOS) is a set of logical layers together with their design rules, which provide a nearly process- and metric-independent interface to many CMOS fabrication processes available through MOSIS.

### Related Resources

- MOSIS Fabrication Schedule
- Customer Support
- MOSIS Products

# Design Rules

- See www.MOSIS.com for design rules

- Some of these files are on class WEB site
  - SCMOS Rules Updated Sept 2005.pdf
  - Mosis Rules Pictorial.pdf

Table 2a: MOSIS SCMOS-Compatible Mappings

| Foundry | Process | Lambda (micro- meters) | Options |
|---|---|---|---|
| ON Semi | C5F/N (0.5 micron *n*-well) | 0.35 | SCN3M, SCN3ME |
| TSMC | 0.35 micron 2P4M (4 Metal Polycided, 3.3 V/5 V) | 0.25 | SCN4ME |
| TSMC | 0.35 micron 1P4M (4 Metal Silicided, 3.3 V/5 V) | 0.25 | SCN4M |

Table 2b: MOSIS SCMOS_SUBM-Compatible Mappings

| Foundry | Process | Lambda (micro- meters) | Options |
|---|---|---|---|
| ON Semi | C5F/N (0.5 micron *n*-well) | 0.30 | SCN3M_SUBM, SCN3ME_SUBM |
| TSMC | 0.35 micron 2P4M (4 Metal Polycided, 3.3 V/5 V) | 0.20 | SCN4ME_SUBM |
| TSMC | 0.35 micron 1P4M (4 Metal Silicided, 3.3 V/5 V) | 0.20 | SCN4M_SUBM |
| TSMC | 0.25 micron 5 Metal 1 Poly (2.5 V/3.3 V) | 0.15 | SCN5M_SUBM |
| TSMC | 0.18 micron 6 Metal 1 Poly (1.8 V/3.3 V) | 0.10 | SCN6M_SUBM |

Table 2c: MOSIS SCMOS_DEEP-Compatible Mappings

| Foundry | Process | Lambda (micro- meters) | Options |
|---|---|---|---|
| TSMC | 0.25 micron 5 Metal 1 Poly (2.5 V/3.3 V) | 0.12 | SCN5M_DEEP |
| TSMC | 0.18 micron 6 Metal 1 Poly (1.8 V/3.3 V) | 0.09 | SCN6M_DEEP |

## 2.1. Well Type

The Scalable CMOS (SC) rules support both *n*-well and *p*-well processes. MOSIS recognizes three base technology codes that let the designer specify the well type of the process selected. SCN specifies an *n*-well process, SCP specifies a *p*-well process, and SCE indicates that the designer is willing to utilize a process of either *n*-well or *p*-well.

An SCE design must provide both a drawn *n*-well and a drawn *p*-well; MOSIS will use the well that corresponds to the selected process and ignore the other well. As a convenience, SCN and SCP designs may also include the other well (*p*-well in an SCN design or *n*-well in an SCP design), but it will always be ignored.

MOSIS currently offers only *n*-well processes or foundry-designated twin-well processes that from the design and process flow standpoints are equivalent to *n*-well processes. These twin-well processes may have options (deep *n*-well) that provide independently isolated *p*-wells. For all of these processes at this time use the technology code SCN. SCP is currently not supported, and SCE is treated exactly as SCN.

## 2.2. SCMOS Options

SCMOS options are used to designate projects that use additional layers beyond the standard single-poly, double metal CMOS. Each option is called out with a designator that is appended to the basic technology-code. Please note that not all possible combinations are available. The current list is shown in Table 1.

MOSIS has not issued SCMOS design rules for some vendor-supported options. For example, any designer using the SCMOS rules who wants the TSMC Thick_Top_Metal must draw the top metal to comply with the TSMC rules for that layer. Questions about other non-SCMOS layers should be directed to support@mosis.com.

Table 1: SCMOS Technology Options

| Designation | Long Form | Description |
|---|---|---|
| E | Electrode | Adds a second polysilicon layer (poly2) that can serve either as the upper electrode of a poly capacitor or (1.5 micron only) as a gate for transistors |
| A | Analog | Adds electrode (as in E option), plus layers for vertical NPN transistor pbase |
| 3M | 3 Metal | Adds second via (via2) and third metal (metal3) layers |
| 4M | 4 Metal | Adds 3M plus third via (via3) and fourth metal (metal4) layers |
| 5M | 5 Metal | Adds 4M plus fourth via (via4) and fifth metal (metal5) layers |
| 6M | 6 Metal | Adds 5M plus fifth via (via5) and sixth metal (metal6) layers |
| LC | Linear Capacitor | Adds a cap_well layer for linear capacitors |
| PC | Poly Cap | Adds poly_cap, a different layer for linear capacitors |
| SUBM | Sub-Micron | Uses revised layout rules for better fit to sub-micron processes (see section 2.4) |
| DEEP | Deep | Uses revised layout rules for better fit to deep sub-micron processes (see section 2.4) |

Table 5: Technology-code Map

| Technology code with link to layer map | Layers |
|---|---|
| SCNE | N_well, Active, N_select, P_select, Poly, Poly2, Contact, Metal1, Via, Metal2, Glass |
| SCNA | N_well, Active, N_select, P_select, Poly, Poly2, Contact, Pbase, Metal1, Via, Metal2, Glass |
| SCNPC | N_well, Active, N_select, P_select, Poly_cap, Poly, Contact, Metal1, Via, Metal2, Glass |
| SCN3M | N_well, Active, N_select, P_select, Poly, Silicide block (Agilent/HP only), Hi_Res_Implant, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass |
| SCN3ME | N_well, Active, N_select, P_select, Poly, Poly2, Hi_Res_Implant, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass |

Table 5: Technology-code Map

| Technology code with link to layer map | Layers |
|---|---|
| SCNE | N_well, Active, N_select, P_select, Poly, Poly2, Contact, Metal1, Via, Metal2, Glass |
| SCNA | N_well, Active, N_select, P_select, Poly, Poly2, Contact, Pbase, Metal1, Via, Metal2, Glass |
| SCNPC | N_well, Active, N_select, P_select, Poly_cap, Poly, Contact, Metal1, Via, Metal2, Glass |
| SCN3M | N_well, Active, N_select, P_select, Poly, Silicide block (Agilent/HP only), Hi_Res_Implant, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass |
| SCN3ME | N_well, Active, N_select, P_select, Poly, Poly2, Hi_Res_Implant, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass |

# SCMOS Layout Rules - Well

| Rule | Description | Lambda | | |
|---|---|---|---|---|
| | | SCMOS | SUBM | DEEP |
| 1.1 | Minimum width | 10 | 12 | 12 |
| 1.2 | Minimum spacing between wells at different potential | 9 [1] | 18 [2] | 18 |
| 1.3 | Minimum spacing between wells at same potential | 6 [3] | 6 [4] | 6 |
| 1.4 | Minimum spacing between wells of different type (if both are drawn) | 0 | 0 | 0 |

Exceptions for AMIS C30 0.35 micron process:

[1] Use lambda=16 for rule 1.2 only when using SCN4M or SCN4ME

[2] Use lambda=21 for rule 1.2 only when using SCN4M_SUBM or SCN4ME_SUBM

[3] Use lambda=8 for rule 1.3 only when using SCN4M or SCN4ME

[4] Use lambda=11 for rule 1.3 only when using SCN4M_SUBM or SCN4ME_SUBM

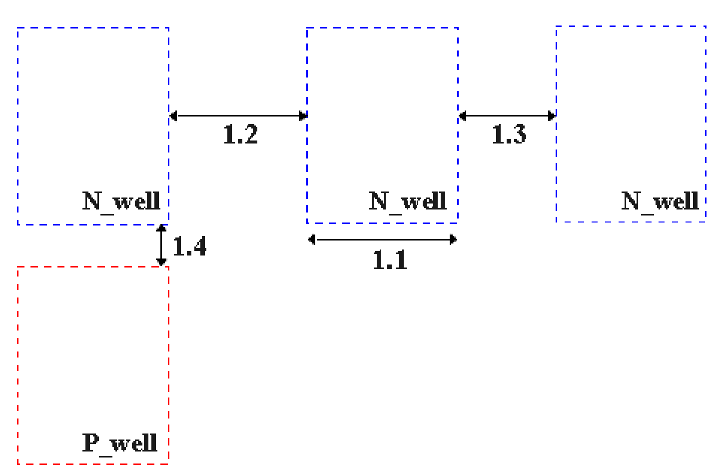


Table 5: Technology-code Map

| Technology code with link to layer map | Layers |
| --- | --- |
| SCNE | N_well, Active, N_select, P_select, Poly, Poly2, Contact, Metal1, Via, Metal2, Glass |
| SCNA | N_well, Active, N_select, P_select, Poly, Poly2, Contact, Pbase, Metal1, Via, Metal2, Glass |
| SCNPC | N_well, Active, N_select, P_select, Poly_cap, Poly, Contact, Metal1, Via, Metal2, Glass |
| SCN3M | N_well, Active, N_select, P_select, Poly, Silicide block (Agilent/HP only), Hi_Res_Implant, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass |
| SCN3ME | N_well, Active, N_select, P_select, Poly, Poly2, Hi_Res_Implant, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass |

| Rule | Description | Lambda | | |
|---|---|---|---|---|
| | | SCMOS | SUBM | DEEP |
| 2.1 | Minimum width | 3 * | 3 * | 3 |
| 2.2 | Minimum spacing | 3 | 3 | 3 |
| 2.3 | Source/drain active to well edge | 5 | 6 | 6 |
| 2.4 | Substrate/well contact active to well edge | 3 | 3 | 3 |
| 2.5 | Minimum spacing between non-abutting active of different implant. Abutting active ("split-active") is illustrated under Select Layout Rules. | 4 | 4 | 4 |

* Note: For analog and critical digital designs, MOSIS recommends the following minimum MOS channel widths (active under poly) for AMIS designs. Narrower devices, down to design rule minimum, will be functional, but their electrical characteristics will not scale, and their performance is not predictable from MOSIS SPICE parameters.

| Process | Design Technology | Design Lambda (micrometers) | Minimum Width (lambda) |
|---|---|---|---|
| AMI_ABN | SCNA, SCNE | 0.80 | 5 |
| AMI_C5F/N | SCN3M, SCN3ME | 0.35 | 9 |
| AMI_C5F/N | SCN3M_SUBM, SCN3ME_SUBM | 0.30 | 10 |

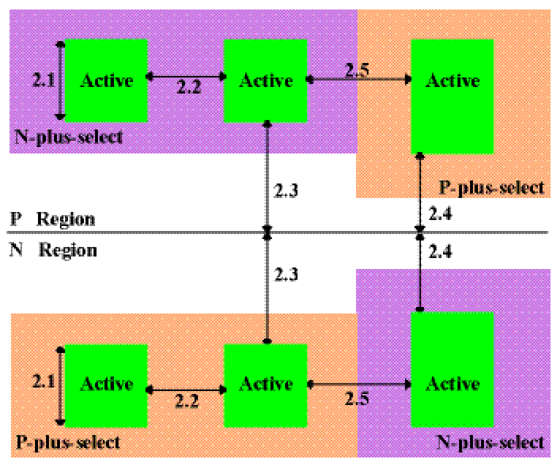


Table 5: Technology-code Map

| Technology code with link to layer map | Layers |
|---|---|
| SCNE | N_well, Active, N_select, P_select, Poly, Poly2, Contact, Metal1, Via, Metal2, Glass |
| SCNA | N_well, Active, N_select, P_select, Poly, Poly2, Contact, Pbase, Metal1, Via, Metal2, Glass |
| SCNPC | N_well, Active, N_select, P_select, Poly_cap, Poly, Contact, Metal1, Via, Metal2, Glass |
| SCN3M | N_well, Active, N_select, P_select, Poly, Silicide block (Agilent/HP only), Hi_Res_Implant, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass |
| SCN3ME | N_well, Active, N_select, P_select, Poly, Poly2, Hi_Res_Implant, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass |

# SCMOS Layout Rules - Poly

| Rule | Description | Lambda | | |
|---|---|---|---|---|
| | | SCMOS | SUBM | DEEP |
| 3.1 | Minimum width | 2 | 2 | 2 |
| 3.2 | Minimum spacing over field | 2 | 3 | 3 |
| 3.2.a | Minimum spacing over active | 2 | 3 | 4 |
| 3.3 | Minimum gate extension of active | 2 | 2 | 2.5 |
| 3.4 | Minimum active extension of poly | 3 | 3 | 4 |
| 3.5 | Minimum field poly to active | 1 | 1 | 1 |

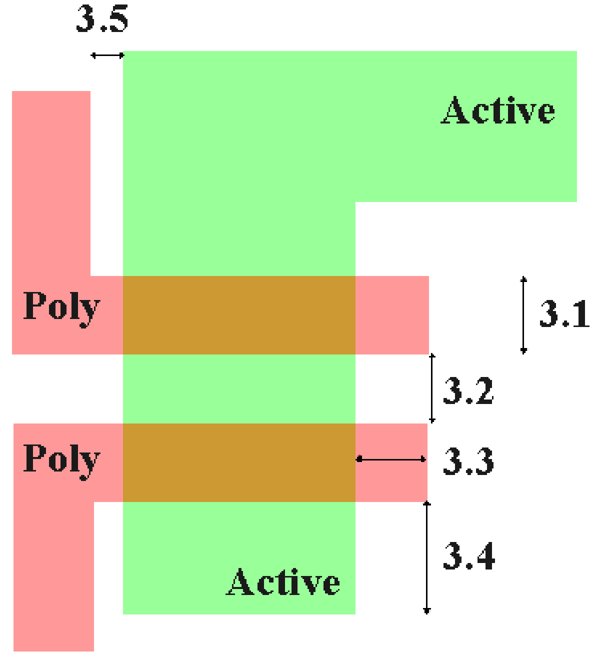
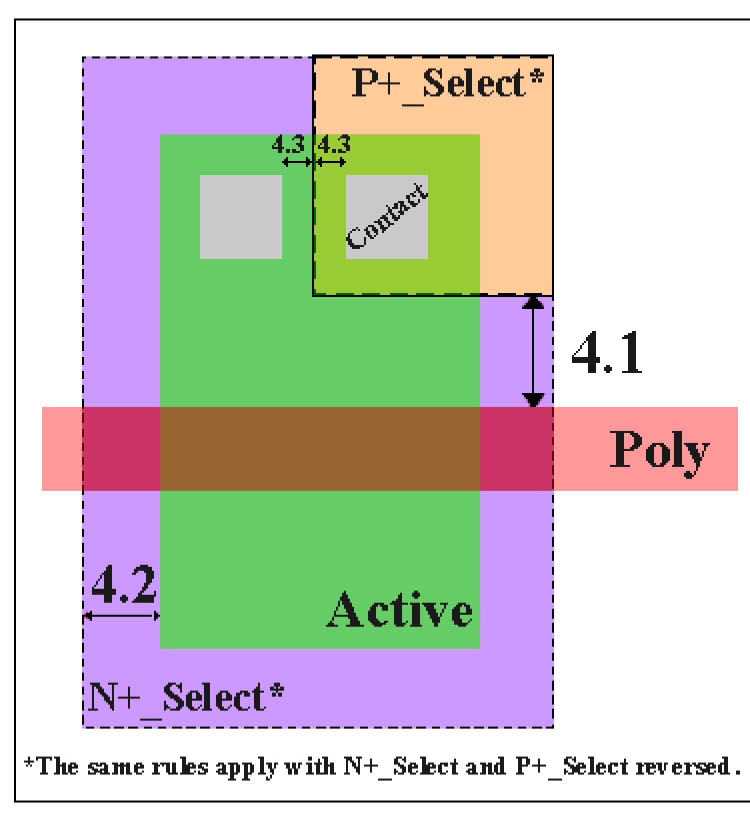


Table 5: Technology-code Map

| Technology code with link to layer map | Layers |
|---|---|
| SCNE | N_well, Active, N_select, P_select, Poly, Poly2, Contact, Metal1, Via, Metal2, Glass |
| SCNA | N_well, Active, N_select, P_select, Poly, Poly2, Contact, Pbase, Metal1, Via, Metal2, Glass |
| SCNPC | N_well, Active, N_select, P_select, Poly_cap, Poly, Contact, Metal1, Via, Metal2, Glass |
| SCN3M | N_well, Active, N_select, P_select, Poly, Silicide block (Agilent/HP only), Hi_Res_Implant, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass |
| SCN3ME | N_well, Active, N_select, P_select, Poly, Poly2, Hi_Res_Implant, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass |

# SCMOS Layout Rules - Select

| Rule | Description | Lambda | | |
|---|---|---|---|---|
| | | SCMOS | SUBM | DEEP |
| 4.1 | Minimum select spacing to channel of transistor to ensure adequate source/drain width | 3 | 3 | 3 |
| 4.2 | Minimum select overlap of active | 2 | 2 | 2 |
| 4.3 | Minimum select overlap of contact | 1 | 1 | 1.5 |
| 4.4 | Minimum select width and spacing (Note: P-select and N-select may be coincident, but must *not* overlap) (not illustrated) | 2 | 2 | 4 |



*The same rules apply with N+_Select and P+_Select reversed.

# Technology Files

- Design Rules

Process Flow (Fabrication Technology)

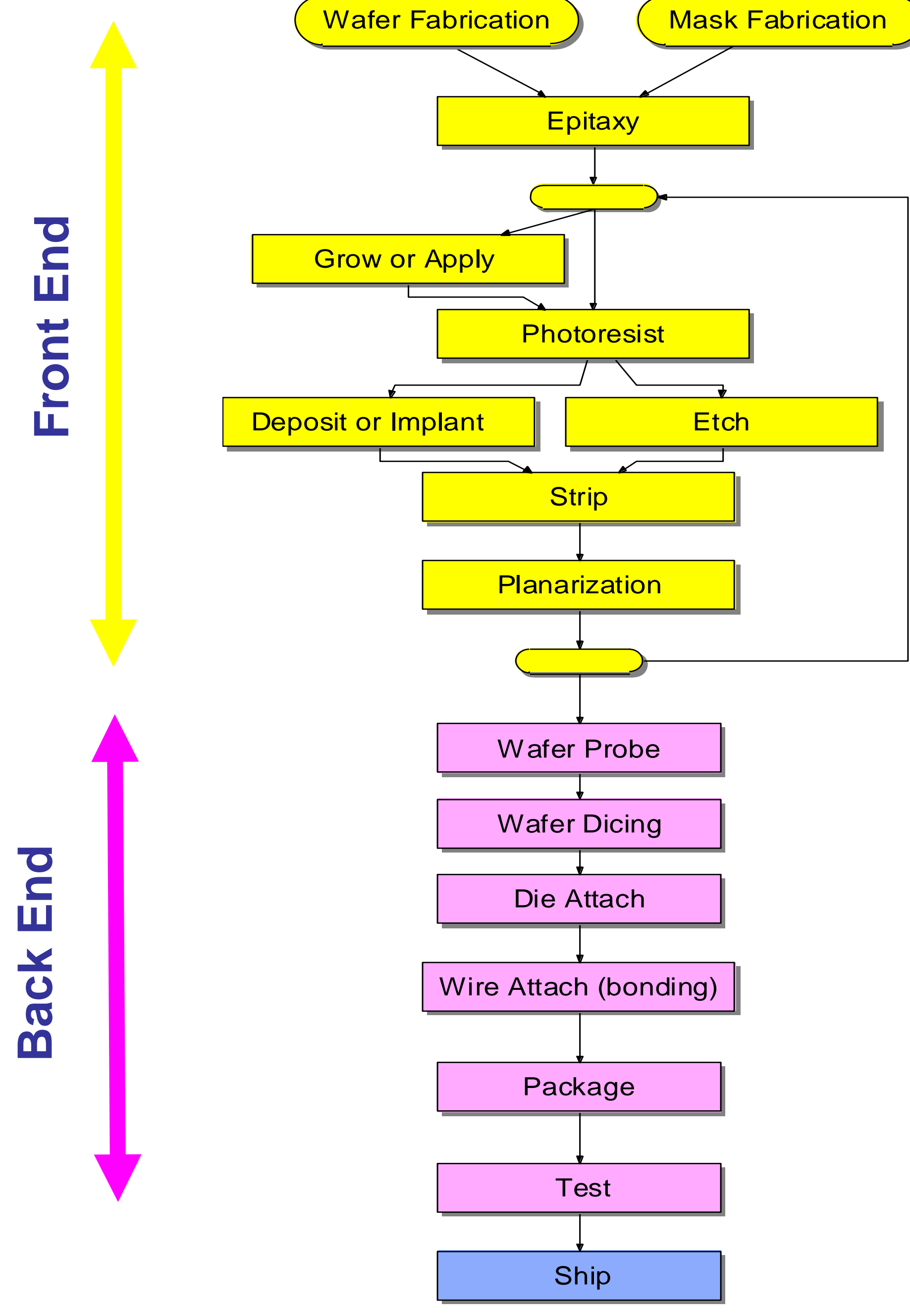
- Model Parameters (will discuss in substantially more detail after device operation and more advanced models are introduced)

# IC Fabrication Technology

See Chapter 3 and a little of Chapter 1 of WH

or Chapter 2 GAS for details

# Generic Process Flow

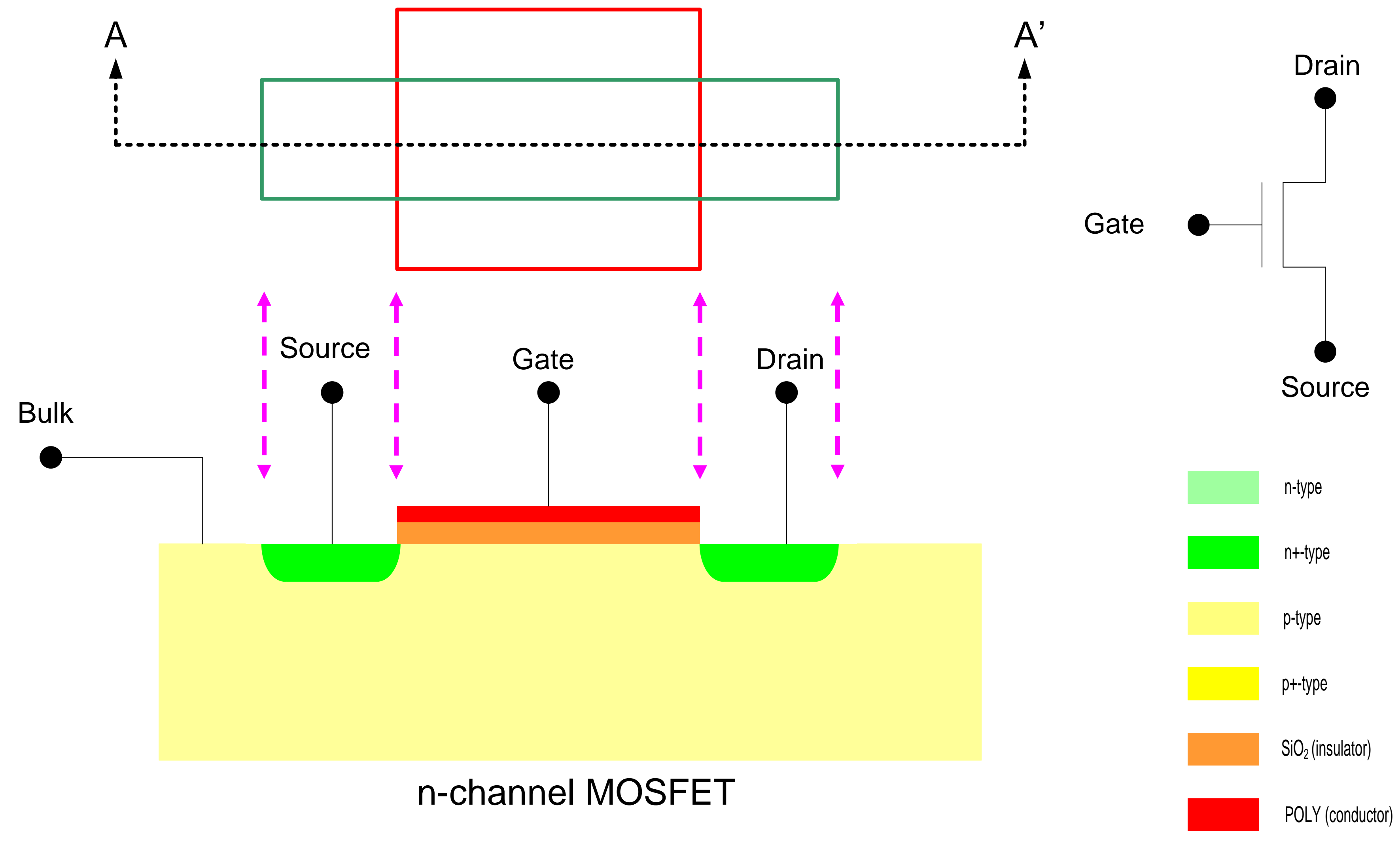


# IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Etching
- Diffusion
- Oxidation
- Epitaxy
- Polysilicon
- Contacts, Interconnect and Metalization
- Planarization

Review

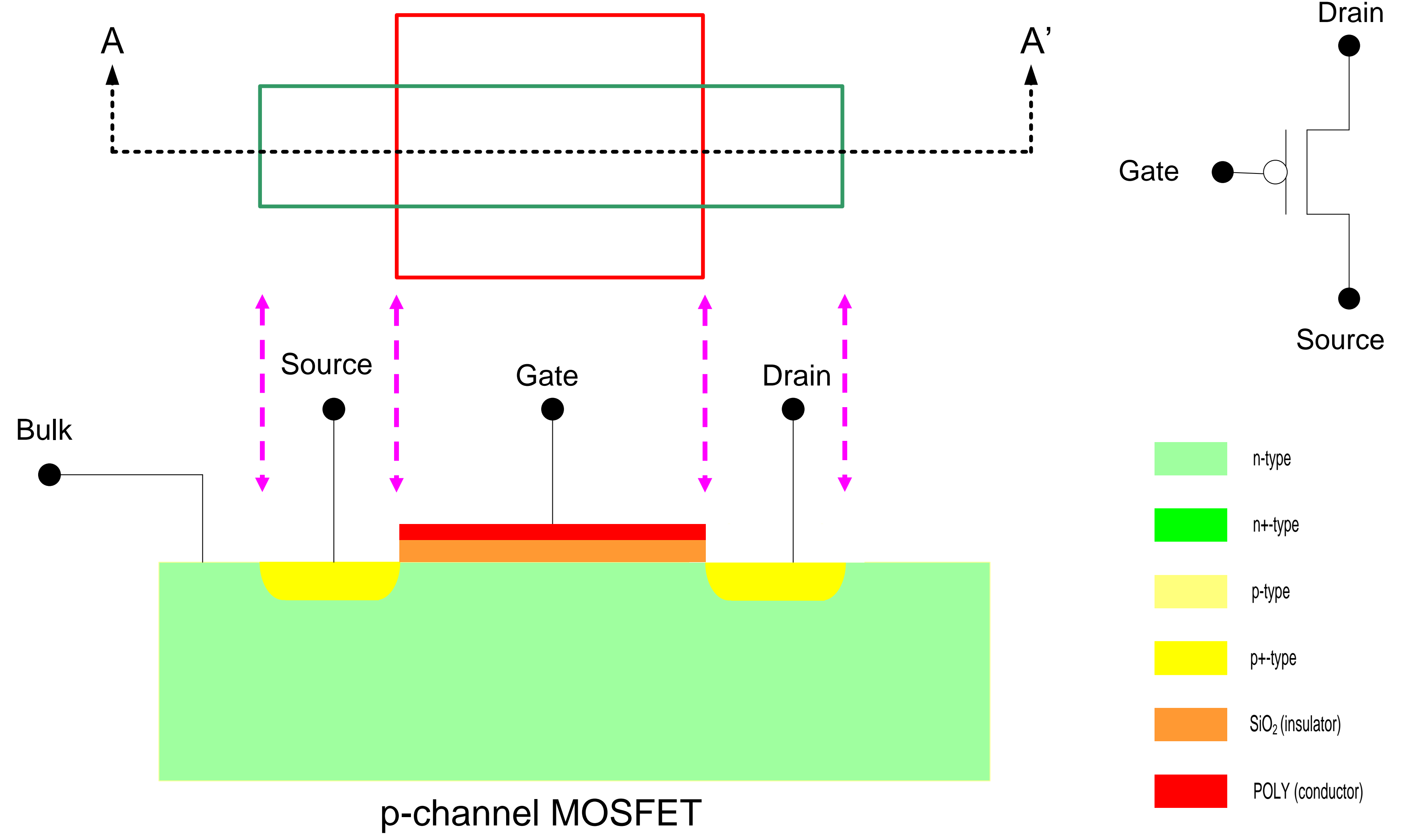
# MOS Transistor




n-channel MOSFET

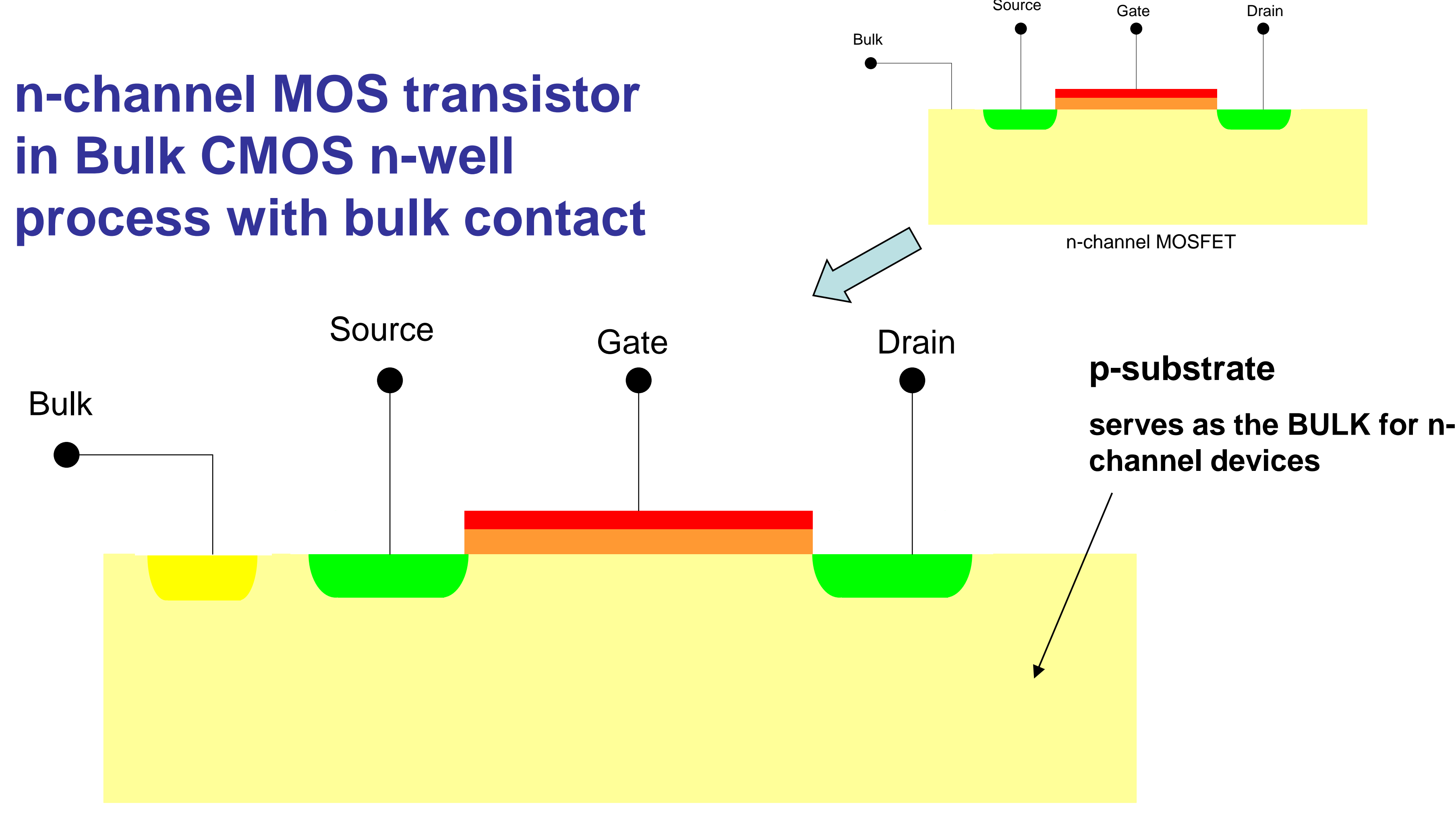
Review

# MOS Transistor

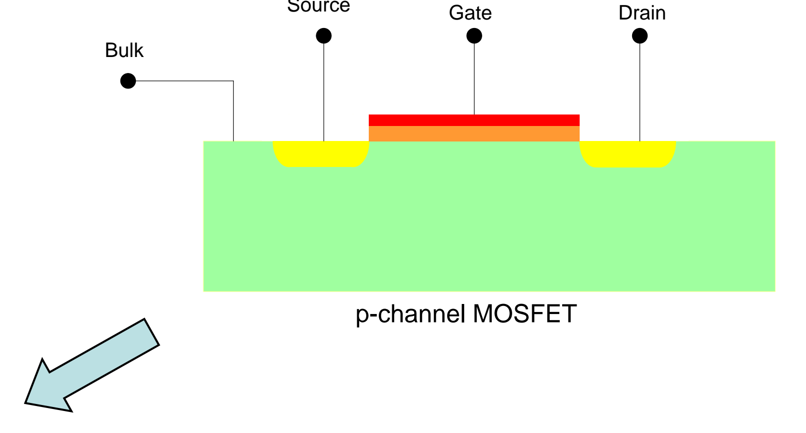


# MOS Transistor

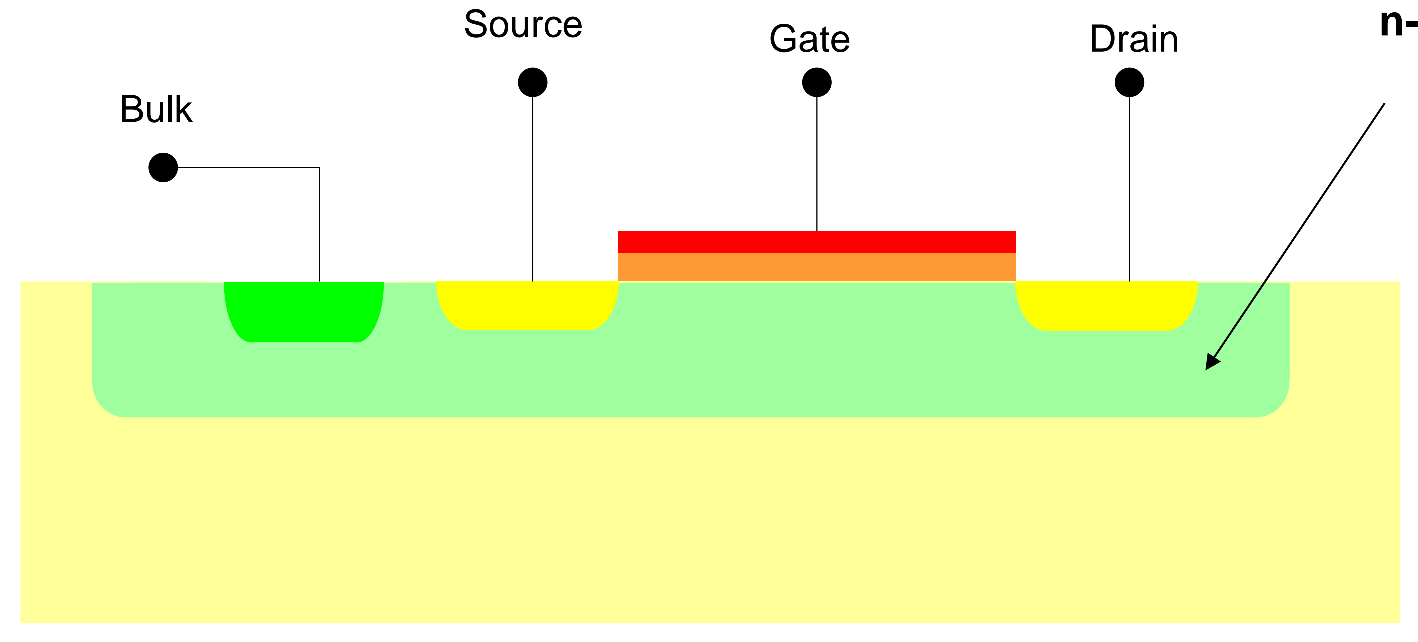
**n-channel MOS transistor in Bulk CMOS n-well process with bulk contact**



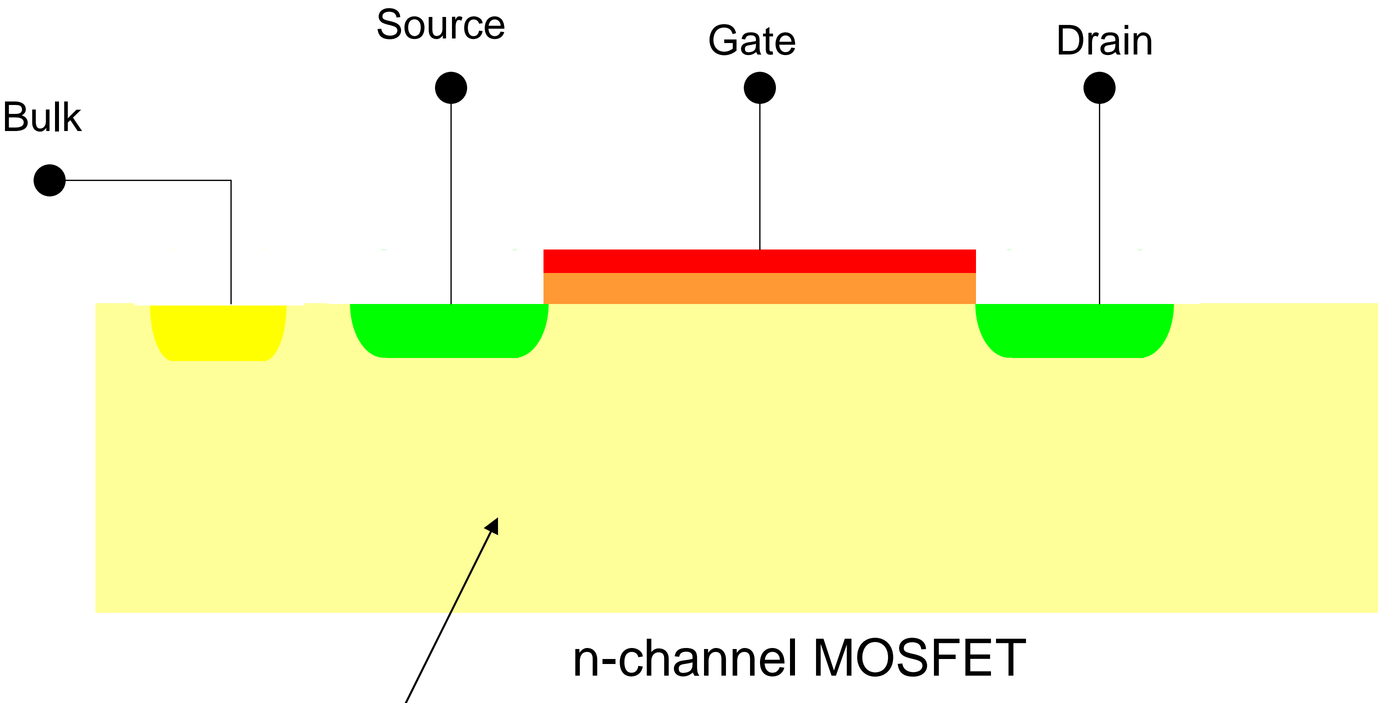
# MOS Transistor




**p-channel MOS transistor in Bulk CMOS n-well process with bulk contact and well (tub)**

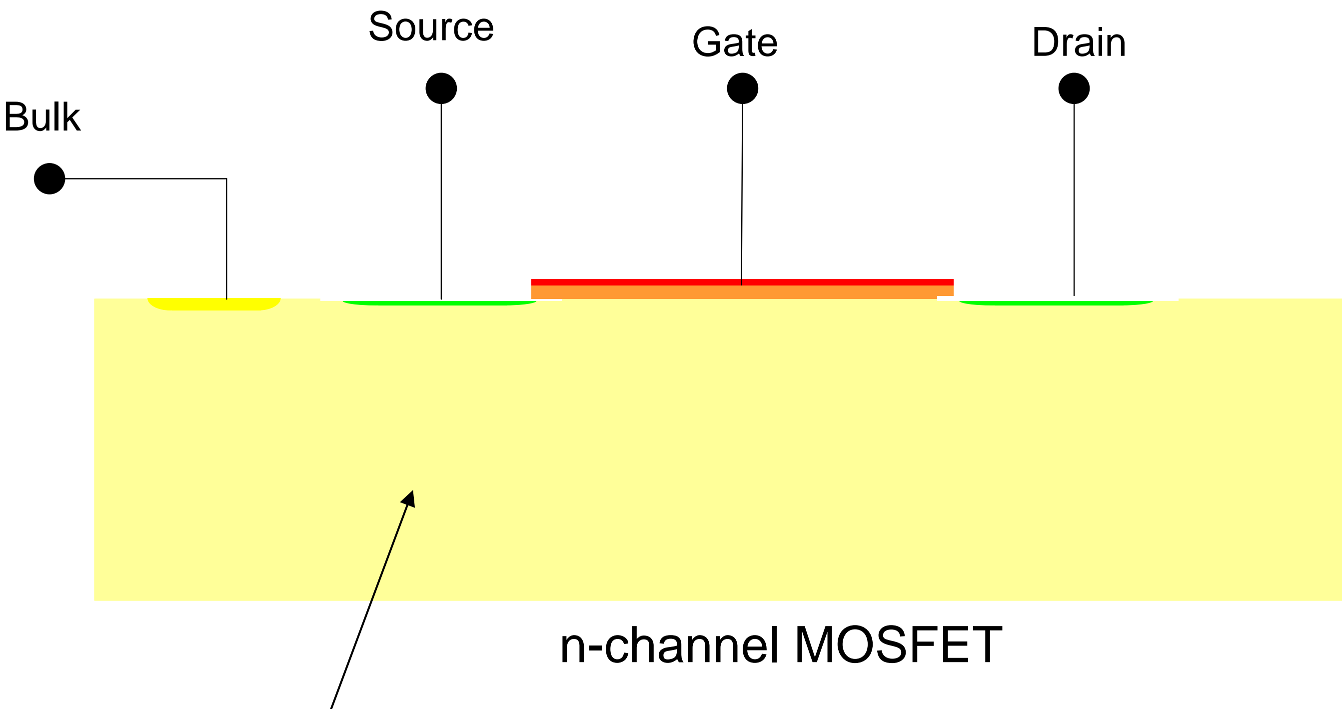


# MOS Transistor




- **Single-crystalline silicon**
  - **Serves as physical support member**
  - **Lightly doped**
  - **Vertical dimensions are not linearly depicted**
  - **Often termed the Bulk**

# MOS Transistor




- **Single-crystalline silicon**
  - **Serves as physical support member**
  - **Lightly doped**
  - **Vertical dimensions are not linearly depicted**
  - **Often termed the BULK**

# MOS Transistor

Conductor (usually polysilicon)

Source

Gate

Drain

Bulk

**Thin insulator**

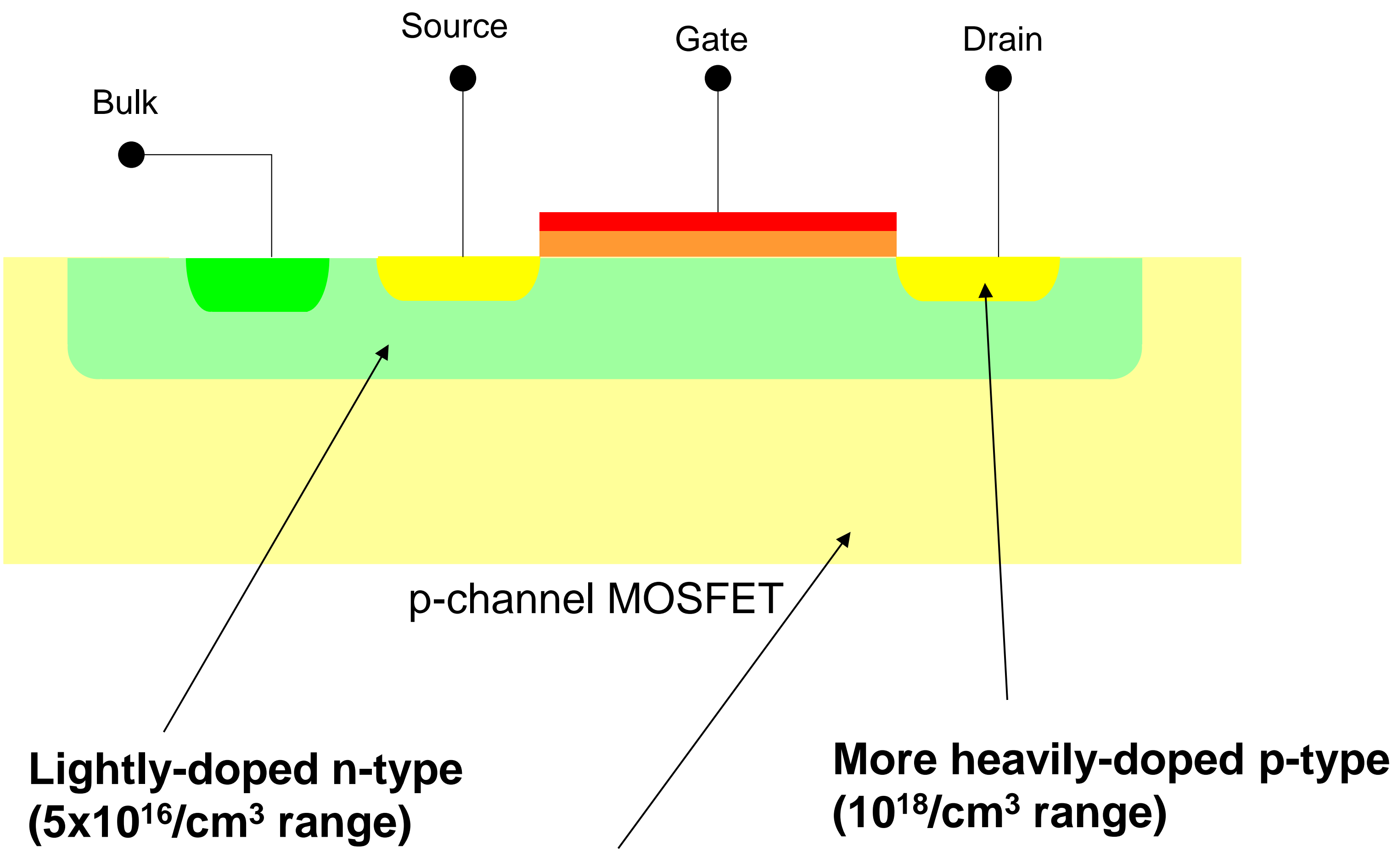
**(10A to 50A range)**

n-channel MOSFET

- **Single-crystalline silicon**
  - **Serves as physical support member**
  - **Lightly doped (p-doping in the $10^{15}/cm^3$ range, silicon in the $2.2x10^{22}/cm^3$ range)**
  - **Vertical dimensions are not linearly depicted**
  - **Often termed the BULK**

**More heavily doped ($10^{17}/cm^3$ range)**

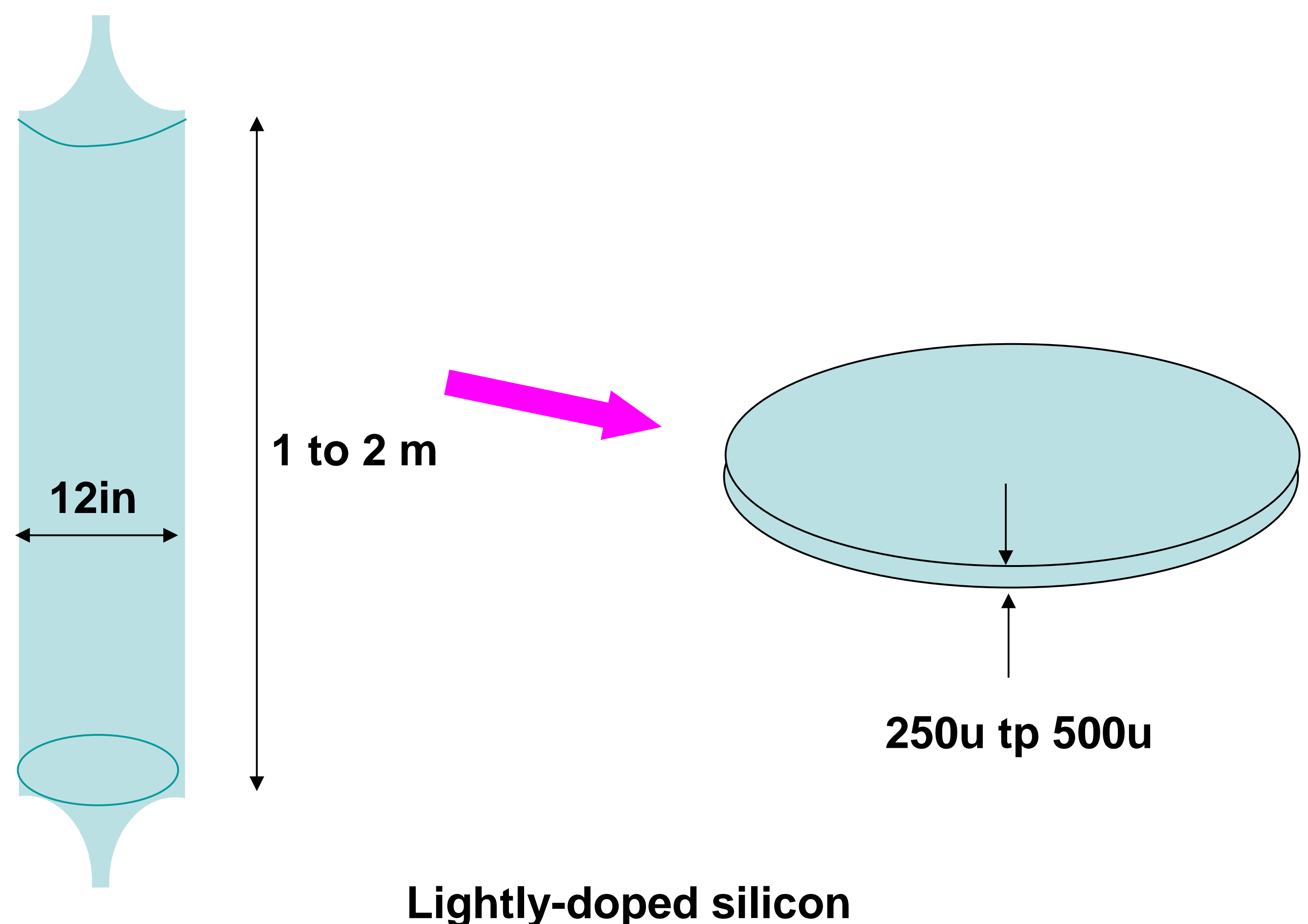
# MOS Transistor



# Crystal Preparation

- Large crystal is grown (pulled)
  - 12 inches in diameter and 1 to 2 m long
  - Sliced to 250u to 500u thick
    - Prefer to be much thinner but thickness needed for mechanical integrity
  - 4 to 8 cm/hr pull rate
  - T=1430 $^{o}$C
- Crystal is sliced to form wafers
- Cost for 12" wafer around $200
- 5 companies provide 90% of worlds wafers
- Somewhere around 400,000 12in wafers/month

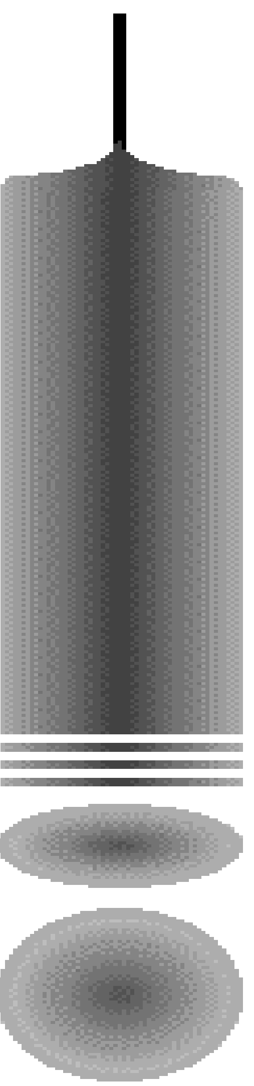
# Crystal Preparation




**Lightly-doped silicon**
**Excellent crystalline structure**

**To go to 450mm (18in) by 2010**
**(ITRS 2007 FEP page 3)**

# Crystal Preparation

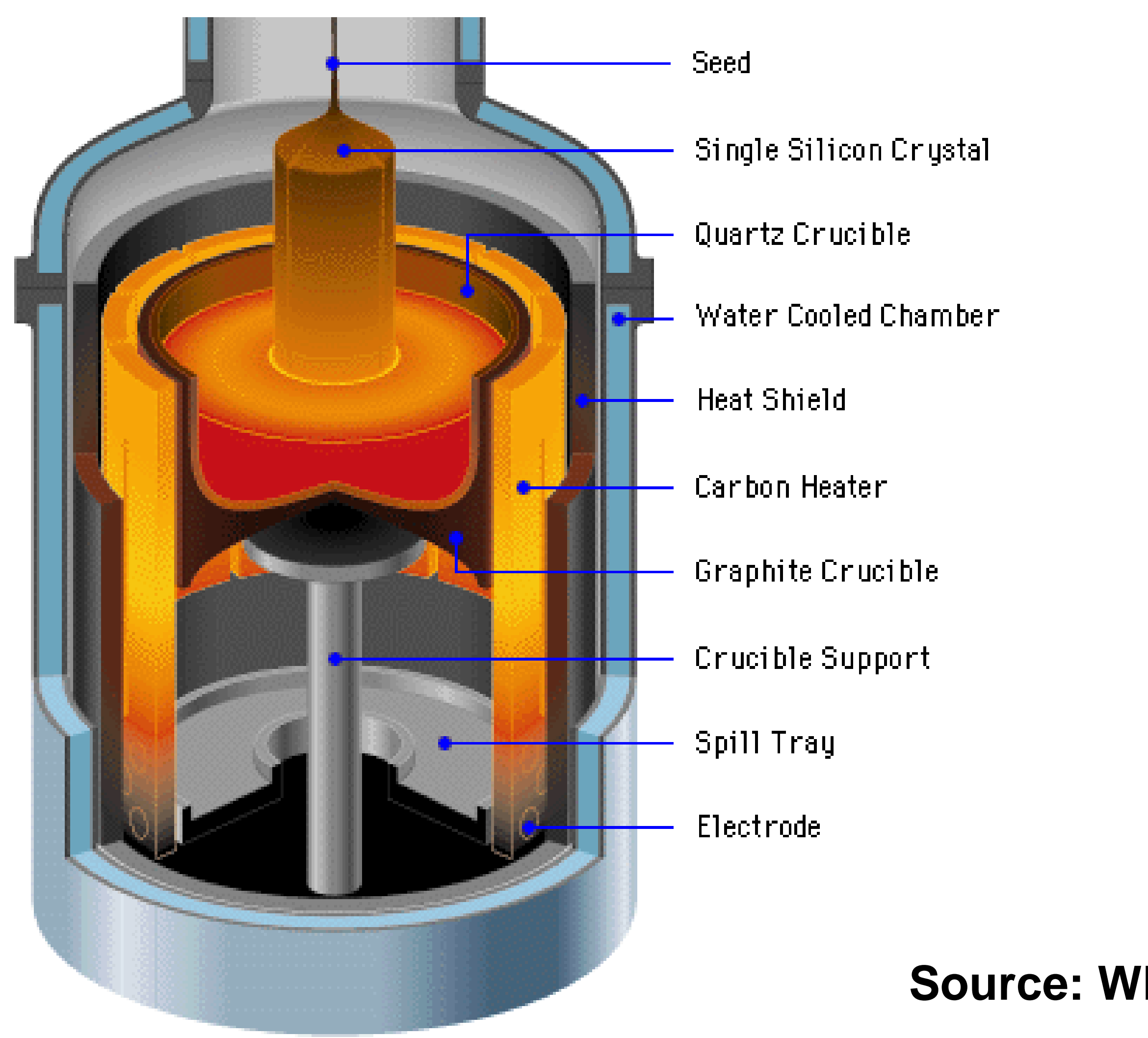


**From www.infras.com**

# Crystal Preparation

**Source: WEB**

# Crystal Preparation




**Source: WEB**

# Crystal Preparation

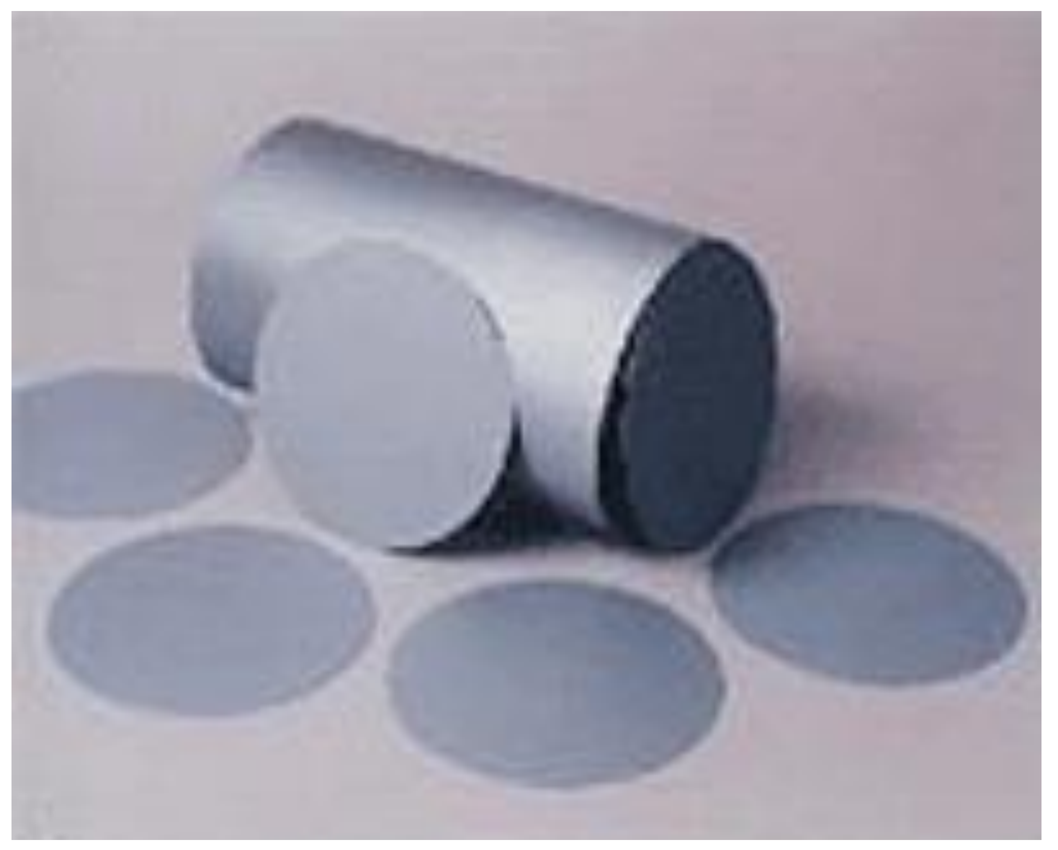
**Source: WEB**

# Crystal Preparation

A section of 300mm ingot is loaded into a wiresaw

**Source: WEB**

# Crystal Preparation



**Source: WEB**

# IC Fabrication Technology

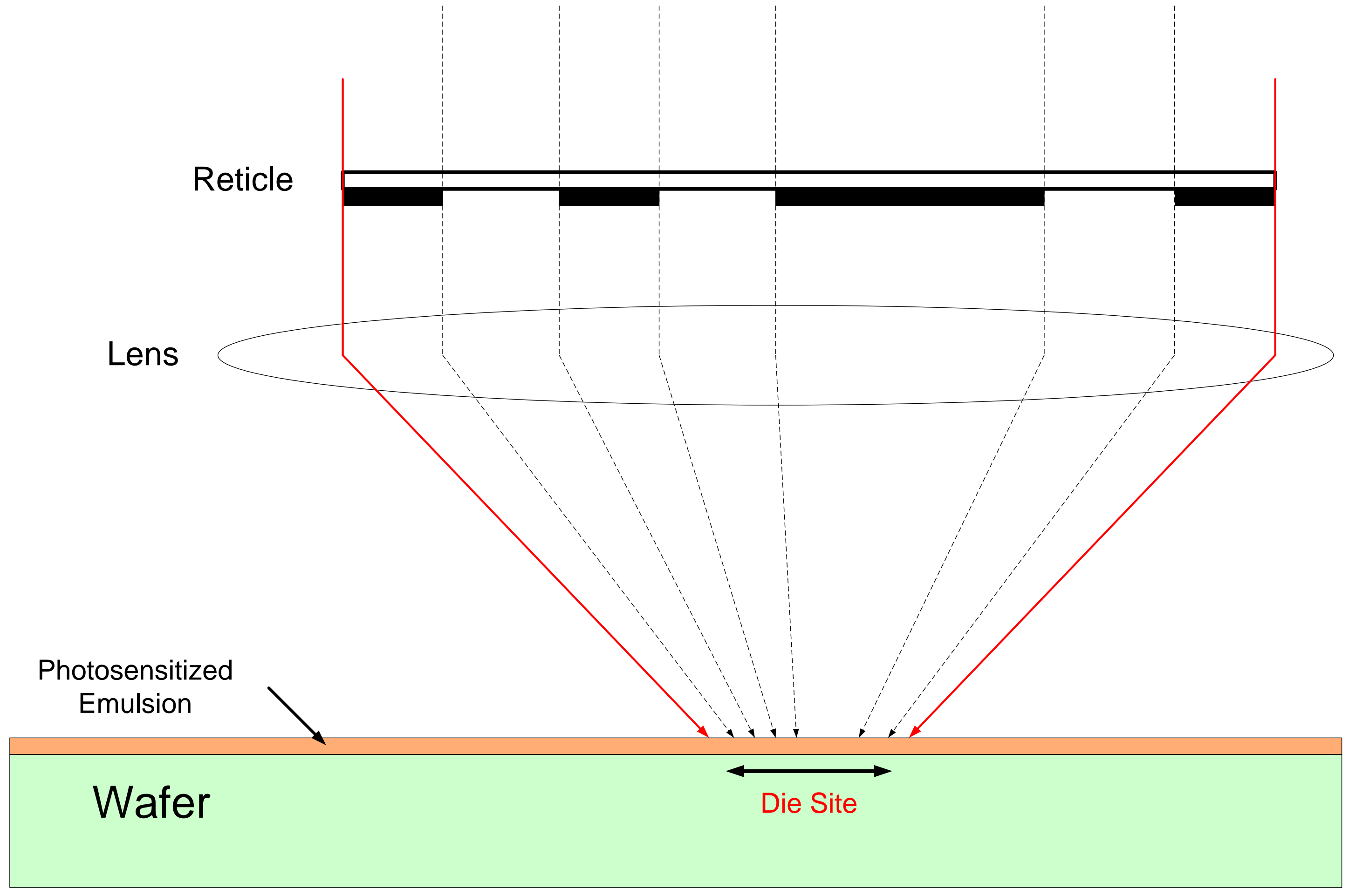
- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Etching
- Diffusion
- Oxidation
- Epitaxy
- Polysilicon
- Contacts, Interconnect and Metalization
- Planarization

# Masking

- Use masks or reticles to define features on a wafer
  - Masks same size as wafer
  - Reticles used for projection
  - Reticle much smaller (but often termed mask)
  - Reticles often of quartz with chrome
  - Quality of reticle throughout life of use is critical
  - Single IC may require 20 or more reticles
  - Cost of “mask set” now exceeds $1million for state of the art processes
  - Average usage 500 to 1500 times
  - Mask costs exceeding 50% of total fabrication costs in sub 100nm processes
  - Serve same purpose as a negative (or positive) in a photographic process
  - Usually use 4X optical reduction - exposure area approx. 860mm$^2$

    (now through 2022 ITRS 2007 litho, Table LITH3a)

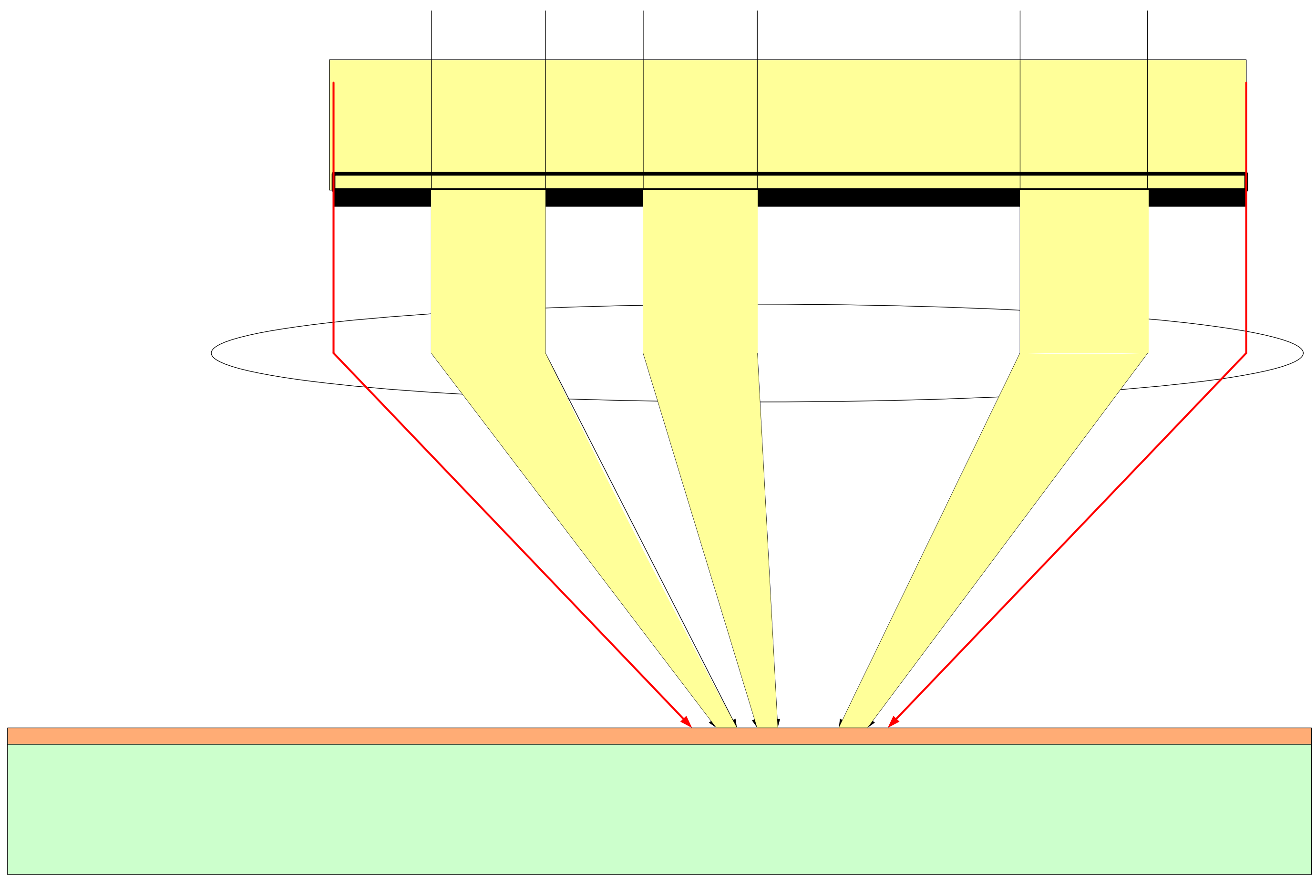
# Masking




**Step and Repeat (stepper) used to image across wafer**

# Masking

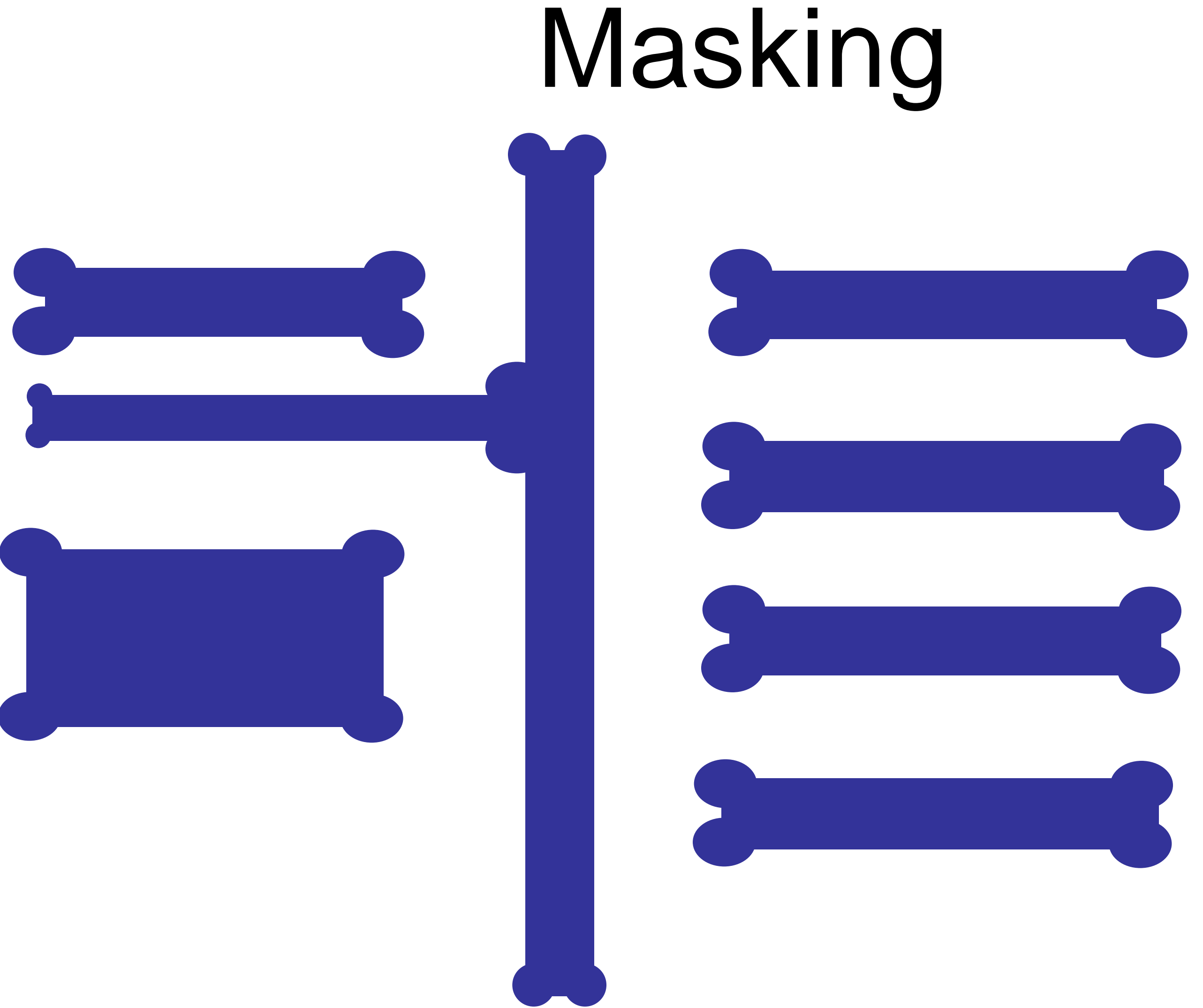
## Exposure through reticle



# Masking

**Mask Features**

# Masking



**Mask Features Intentionally Distorted to Compensated For Wavelength Limitations in Small Features**

# IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Etching
- Diffusion
- Oxidation
- Epitaxy
- Polysilicon
- Contacts, Interconnect and Metalization
- Planarization

# Photolithographic Process

- Photoresist
  - Viscous Liquid
  - Uniform Application Critical (spinner)
  - Baked to harden
  - Approx 1u thick
  - Non-Selective
  - Types
    - Negative – unexposed material removed when developed
    - Positive-exposed material removed when developed
    - Thickness about 450nm in 90nm process (ITRS 2007 Litho)
- Exposure
  - Projection through reticle with stepper (scanners becoming popular)
  - Alignment is critical !!
  - E-Bean Exposures
    - Eliminate need fro reticle
    - Capacity very small

**Stepper: Optics fixed, wafer steps in fixed increments**
**Scanner: Wafer steps in fixed increments and during exposure both optics and wafer are moved to increase effective reticle size**

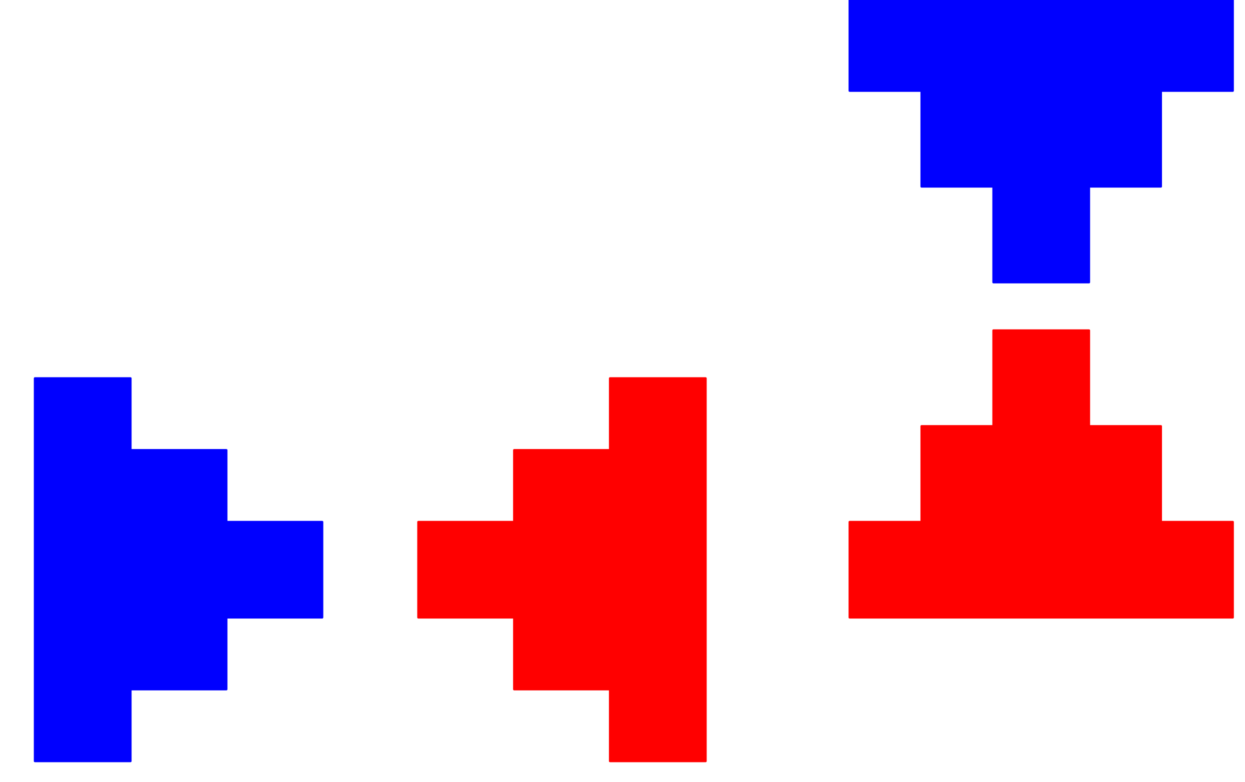
# Steppers

**Stepper costs in the $10M range with thru-put of around 100 wafers/hou**

# Steppers

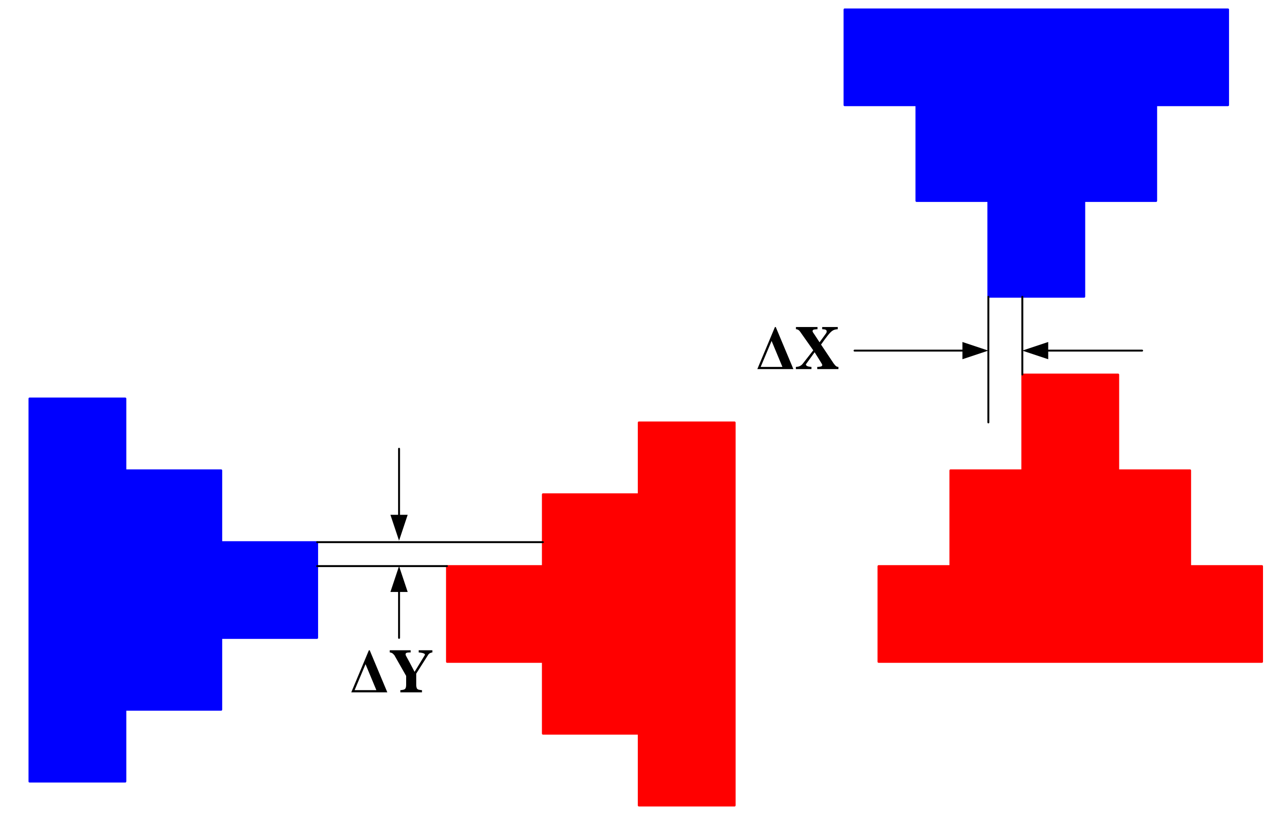
# Mask Alignment

**Correctly Aligned**



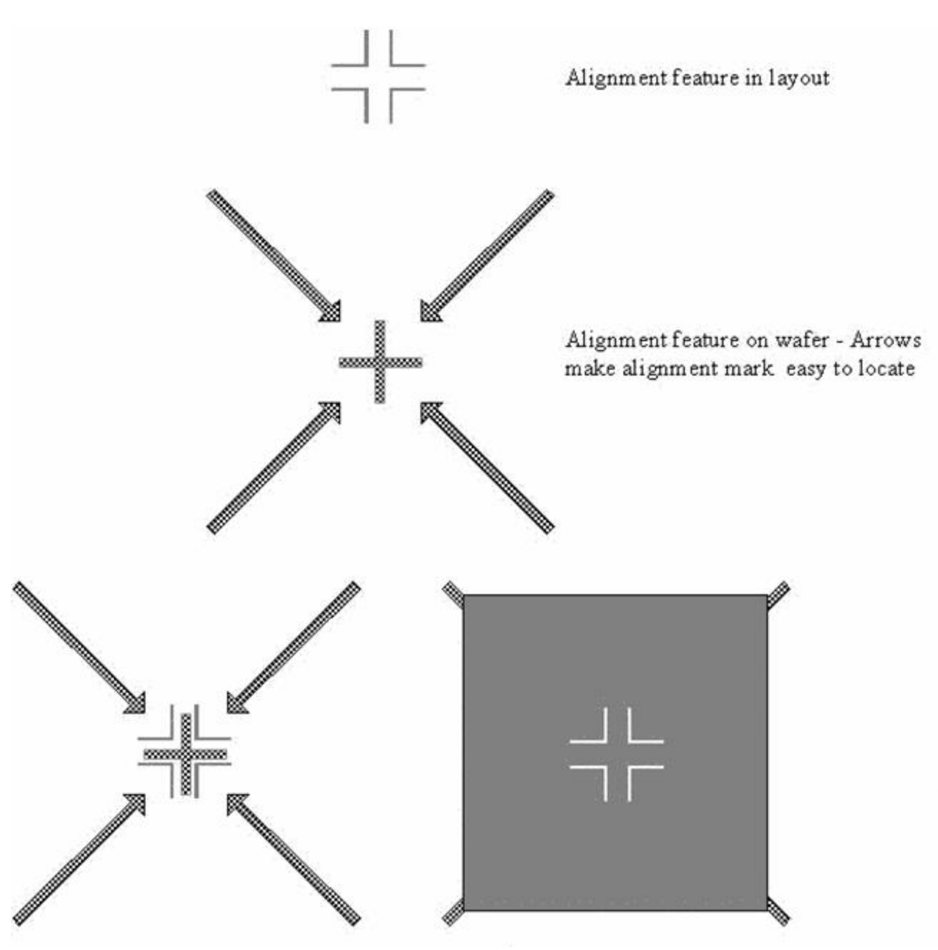
# Mask Alignment

## Alignment Errors



# Mask Alignment

**Other alignment marks** (http://www.mems-exchange.org/users/masks/intro-equipment.html)



# End of Lecture 8