EE 330
Lecture 8
IC Fabrication Technology
Part II
- Masking
- Photolithography
- Deposition
- Etching
- Diffusion
- Oxidation
MOS Transistor

Review from Last Time

Lightly-doped n-type (5x10^{16}/cm^3 range)

More heavily-doped p-type (10^{18}/cm^3 range)

Lightly doped p-type (10^{15}/cm^3 range)
Review from Last Time

Generic Process Flow

- Wafer Fabrication
- Mask Fabrication
- Epitaxy
- Grow or Apply
- Photoresist
- Deposit or Implant
- Etch
- Strip
- Planarization
- Wafer Probe
- Wafer Dicing
- Die Attach
- Wire Attach (bonding)
- Package
- Test
- Ship
IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
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- Oxidation
- Epitaxy
- Polysilicon
- Contacts, Interconnect and Metalization
- Planarization
Crystal Preparation

Review from Last Time

Lightly-doped silicon
Excellent crystalline structure

To go to 450mm (18in) by 2010
(ITRS 2007 FEP page 3)
IC Fabrication Technology

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Masking

- Use masks or reticles to define features on a wafer
  - Masks same size as wafer
  - Reticles used for projection
  - Reticle much smaller (but often termed mask)
  - Reticles often of quartz with chrome
  - Quality of reticle throughout life of use is critical
  - Single IC may require 20 or more reticles
  - Cost of “mask set” now exceeds $1million for state of the art processes
  - Average usage 500 to 1500 times
  - Mask costs exceeding 50% of total fabrication costs in sub 100nm processes
  - Serve same purpose as a negative (or positive) in a photographic process
  - Usually use 4X optical reduction - exposure area approx. 860mm$^2$
    (now through 2022 ITRS 2007 litho, Table LITH3a)
Masking

Step and Repeat (stepper) used to image across wafer
Masking

Exposure through reticle
Masking

Mask Features
Masking

Mask Features Intentionally Distorted to Compensate For Wavelength Limitations in Small Features
IC Fabrication Technology

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Photolithographic Process

- **Photoresist**
  - Viscous Liquid
  - Uniform Application Critical (spinner)
  - Baked to harden
  - Approx 1μ thick
  - Non-Selective
  - Types
    - Negative – unexposed material removed when developed
    - Positive-exposed material removed when developed
    - Thickness about 450nm in 90nm process (ITRS 2007 Litho)

- **Exposure**
  - Projection through reticle with stepper (scanners becoming popular)
  - Alignment is critical !!
  - E-Bean Exposures
    - Eliminate need fro reticle
    - Capacity very small

Stepper: Optics fixed, wafer steps in fixed increments
Scanner: Wafer steps in fixed increments and during exposure both optics and wafer are moved to increase effective reticle size
Steppers

Stepper costs in the $10M range with thru-put of around 100 wafers/hour
Steppers
Mask Alignment

Correctly Aligned
Mask Alignment

Alignment Errors

ΔX

ΔY
Mask Alignment

Other alignment marks  (http://www.mems-exchange.org/users/masks/intro-equipment.html)
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Deposition

• Application of something to the surface of the silicon wafer or substrate
  – Layers 15A to 20u thick

• Methods
  – Physical Vapor Deposition (nonselective)
    • Evaporation/Condensation
    • Sputtering (better host integrity)
  – Chemical Vapor Deposition (nonselective)
    • Reaction of 2 or more gases with solid precipitate
    • Reduction by heating creates solid precipitate (pyrolytic)
  – Screening (selective)
    • For thick films
    • Low Tech, not widely used today
Deposition

Example: Chemical Vapor Deposition

Silane (SiH$_4$) is a gas (toxic and spontaneously combustible in air) at room temperature but breaks down into Si and H$_2$ above 400°C so can be used to deposit Si.

$$\text{SiH}_4 \rightarrow \text{Si} + 2\text{H}_2$$
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Implantation

Application of impurities into the surface of the silicon wafer or substrate

- Individual atoms are first ionized (so they can be accelerated)
- Impinge on the surface and burry themselves into the upper layers
- Often very shallow but with high enough energy can go modestly deep
- Causes damage to target on impact
- Annealing heals most of the damage
- Very precise control of impurity numbers is possible
- Very high energy required
- High-end implanters considered key technology for national security
Ion Implantation Process

From http://www.casetechnology.com/implanter
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Etching

Selective Removal of Unwanted Materials

• Wet Etch
  – Inexpensive but under-cutting a problem

• Dry Etch
  – Often termed ion etch or plasma etch
Etching

SiO$_2$  

$\text{p}^-$ Silicon  

Photoresist

**Desired Physical Features**

*Note: Vertical Dimensions Generally Orders of Magnitude Smaller Than Lateral Dimensions so Different Vertical and Lateral Scales Will be Used In This Discussion*
Etching

Dry Etch can provide very well-defined and nearly vertical edges (relative to photoresist patterning)
Etching (limited by photolithographic process)

SiO$_2$

Dry etch (anisotropic)

Photoresist

Consider neg photoresist

$p^-$ Silicon

Over Exposed

Correctly Developed

Over Developed

Under Developed

Under Exposed

Correctly Developed

Over Developed

Under Developed
For Example, the wafer thickness is around 250\(\mu\) and the gate oxide is around 50\(\text{A} \ (5\times10^{-3}\mu)\) and diffusion depths are around \(\lambda/5\).
Etching

SiO₂

p- Silicon

Photoresist

Desired Edges of SiO₂ from Mask

Undercutting (wet etch)

Edge Movement Due to Over Etch, Over Exposure, or Over-Development

Isotropic Feature Degradation
Etching

SiO₂

Undercutting (wet etch)

Desired Edges of SiO₂ from Mask

Edge Movement Due to Over Etch, Over Exposure, or Over-Development

SiO₂ after photoresist removal
IC Fabrication Technology

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Diffusion

- Controlled Migration of Impurities
  - Time and Temperature Dependent
  - Both vertical and lateral diffusion occurs
  - Crystal orientation affects diffusion rates in lateral and vertical dimensions
  - Materials Dependent
  - Subsequent Movement
  - Electrical Properties Highly Dependent upon Number and Distribution of Impurities
  - Diffusion at 800°C to 1200°C

- Source of Impurities
  - Deposition
  - Ion Implantation
    - Only a few Å deep
    - More accurate control of doping levels
    - Fractures silicon crystaline structure during implant
    - Annealing occurs during diffusion

- Types of Impurities
  - n-type  Arsenic, Antimony, Phosphorous
  - p-type  Gallium, Aluminum, Boron
Diffusion

Source of Impurities Deposited on Silicon Surface

Before Diffusion

After Diffusion
Diffusion

Source of Impurities Implanted in Silicon Surface

Before Diffusion

After Diffusion

p⁻ Silicon
Diffusion

Before Diffusion

Implant

After Diffusion

Lateral Diffusion

p- Silicon
p- Silicon
p- Silicon
p- Silicon
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Oxidation

- SiO$_2$ is widely used as an insulator
  - Excellent insulator properties
- Used for gate dielectric
  - Gate oxide layers very thin
- Used to separate devices by raising threshold voltage
  - termed field oxide
  - field oxide layers very thick
- Methods of Oxidation
  - Thermal Growth (LOCOS)
    - Consumes host silicon
    - $x$ units of SiO$_2$ consumes $0.47x$ units of Si
    - Undercutting of photoresist
    - Compromises planar surface for thick layers
    - Excellent quality
  - Chemical Vapor Deposition
    - Needed to put SiO$_2$ on materials other than Si
Oxidation

Photoresist

SiO$_2$

p$^-$ Silicon

Patterned Edges

Thermally Grown SiO$_2$ - desired growth
Oxidation

Thermally Grown SiO$_2$ - actual growth
Oxidation

Nonplanar Surface

p- Silicon

Patterned Edges

Thermally Grown SiO₂ - actual growth
Oxidation

**Shallow Trench Isolation (STI)**

- Photoresist
- Silicon Nitride
- Pad Oxide
- p$^-$ Silicon
Oxidation

Shallow Trench Isolation (STI)

- Silicon Nitride
- Etched Shallow Trench
- Pad Oxide
- p⁻ Silicon

Shallow Trench Isolation (STI)
Oxidation

Shallow Trench Isolation (STI)

- Silicon Nitride
- CVD SiO$_2$
- Pad Oxide
- p$^-$ Silicon

Shallow Trench Isolation (STI)
Oxidation

Planarity Improved

p^- Silicon

Planarization Target

Shallow Trench Isolation (STI)
Oxidation

After Planarization

CVD SiO$_2$

$\textit{p}^-$ Silicon

Shallow Trench Isolation (STI)
End of Lecture 8