EE 330
Lecture 8

Stick Diagrams

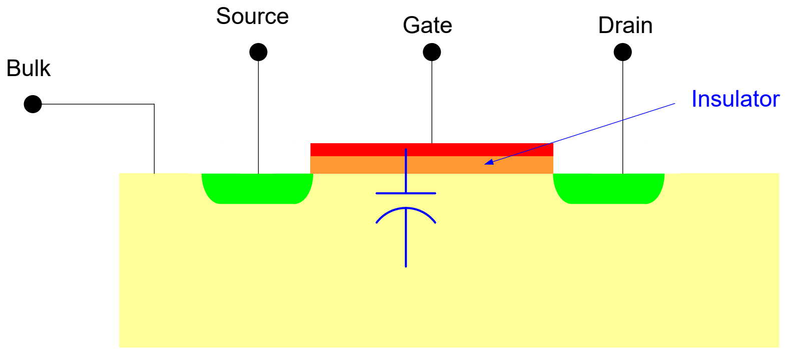
Technology Files

- Design Rules
- Process Flow
- Model Parameters

Review from Last Time

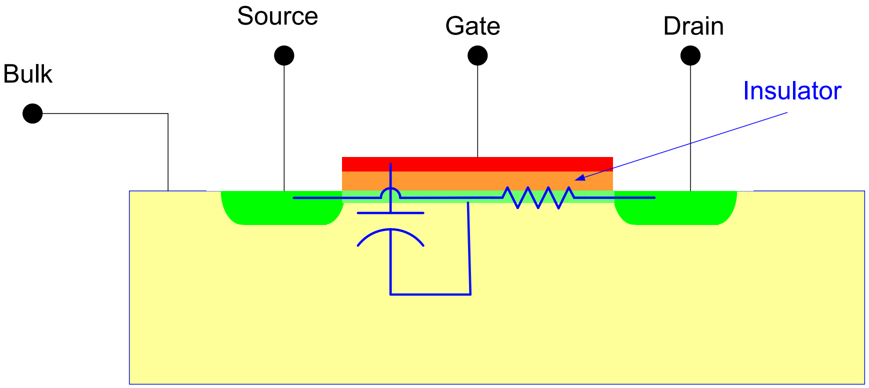
MOS Transistor

Qualitative Discussion of n-channel Operation



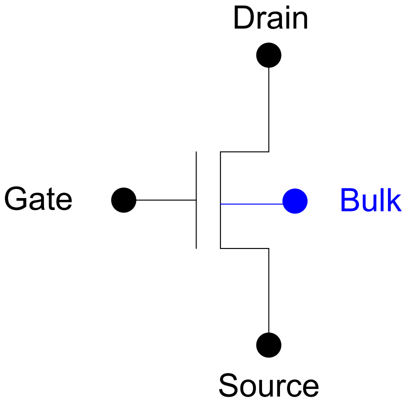
n-channel MOSFET

For V_{GS} small



n-channel MOSFET

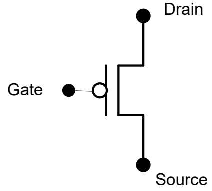
For V_{GS} large



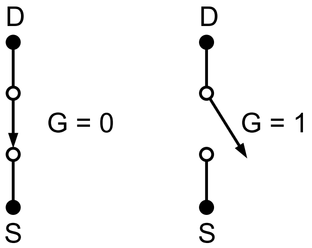
- Electrically created inversion layer forms a “thin “film” resistor
- Capacitance from gate to channel region is distributed
- Lumped capacitance much easier to work with

Review from Last Time

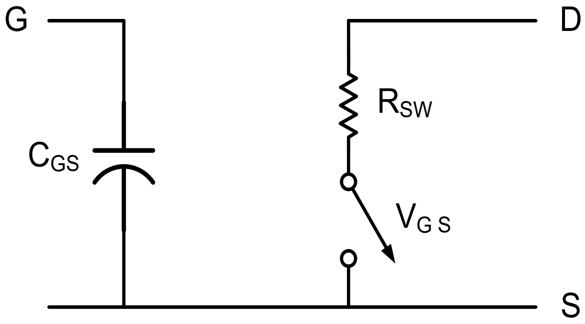
Model Summary (for p-channel)



1. Switch-Level model



2. Improved switch-level model



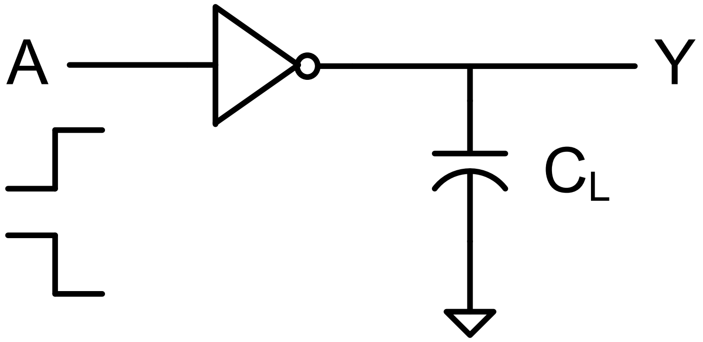
Switch closed for $|V_{GS}|$= large

Switch open for $|V_{GS}|$= small

Other models will be developed later

Review from Last Time

Response time of logic gates



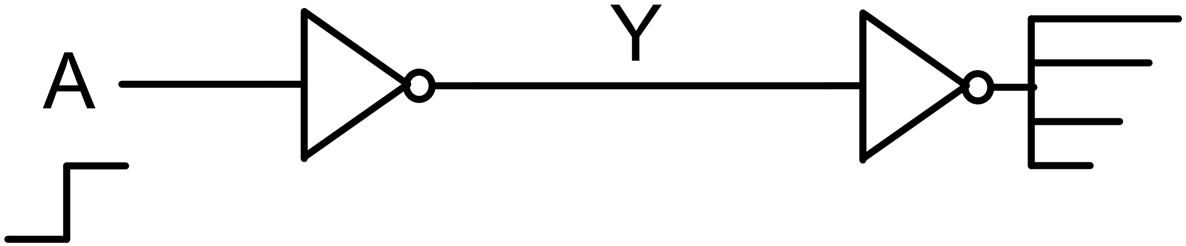
$$t_{HL} \cong R_{SWn} C_L$$

$$t_{LH} \cong R_{SWp} C_L$$

- Logic Circuits can operate very fast
- Extremely small parasitic capacitances play key role in speed of a circuit

Review from Last Time

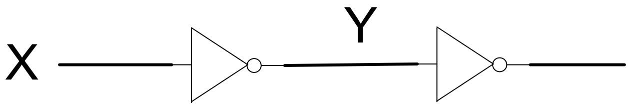
One gate often drives one or more other gates !

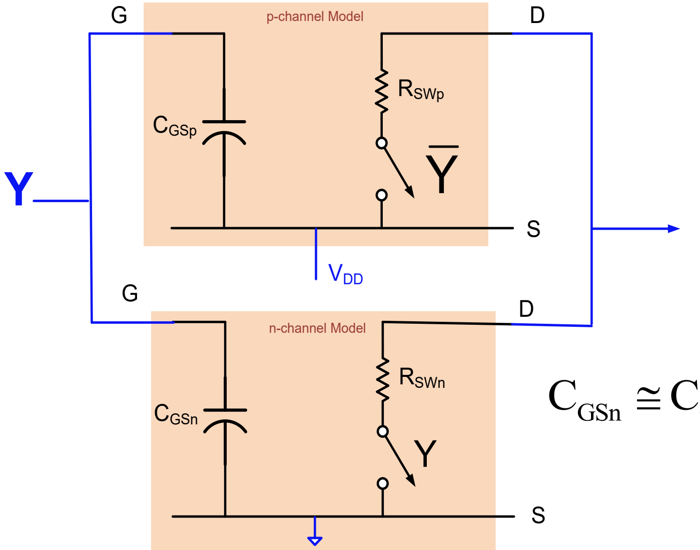


What are t_{HL} and t_{LH}?

Review from Last Time

Example: What is the delay of a minimum-sized inverter driving another identical device?





Load on first inverter

C_{GSn} *and* C_{GSp} *both* $1.5fF$

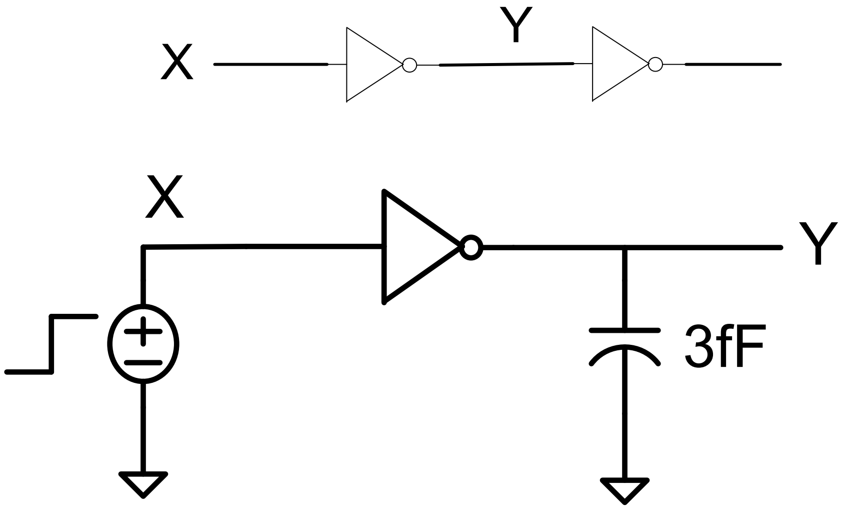
$$C_{GSn} \cong C_{GSp} \cong 1.5\text{fF}$$

Loading effects same whether C_{GSp} *and/or* C_{GSn} *connected to* V_{DD} *or GND*

For convenience, will reference both to ground

Review from Last Time

Example: What is the delay of a minimum-sized inverter driving another identical device?



$$t_{HL} \cong R_{SWn} C_L \qquad = 2K \bullet 3fF = 6p\,\text{sec}$$

$$t_{LH} \cong R_{SWp} C_L \qquad = 6K \bullet 3fF = 18p\,\text{sec}$$

Do gates really operate this fast?

What would be the maximum clock rate for acceptable operation?

Stick Diagrams

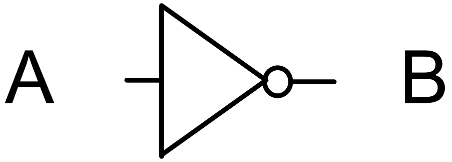
- It is often necessary to obtain information about placement, interconnect and physical-layer structure
- Stick diagrams are often used for small component-count blocks
- Approximate placement, routing, and area information can be obtained rather quickly with the use of stick diagrams

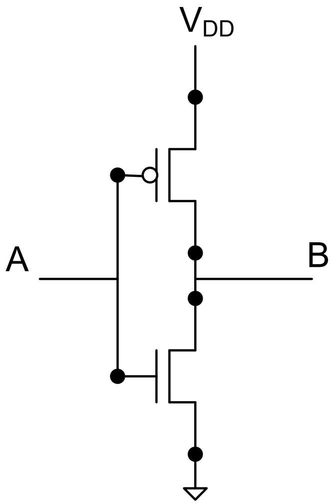
Stick Diagrams

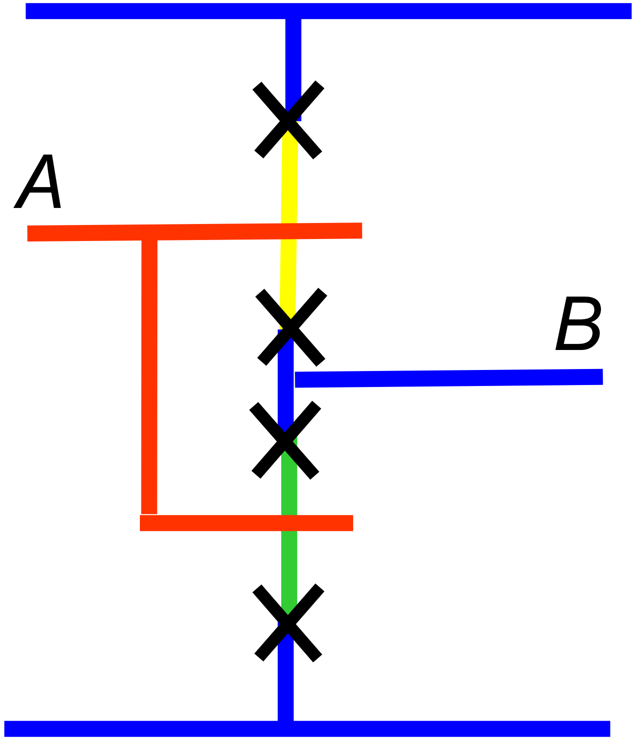
🟦	*Metal 1*
🟥	*poly*
🟩	*n-diffusion*
🟨	*p-diffusion*
🟪	*Metal 2*
✕	*Contact*

Additional layers can be added and color conventions are personal

Stick Diagram





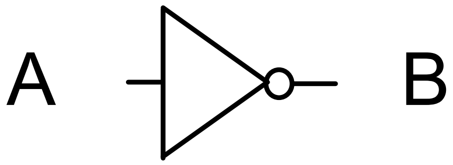


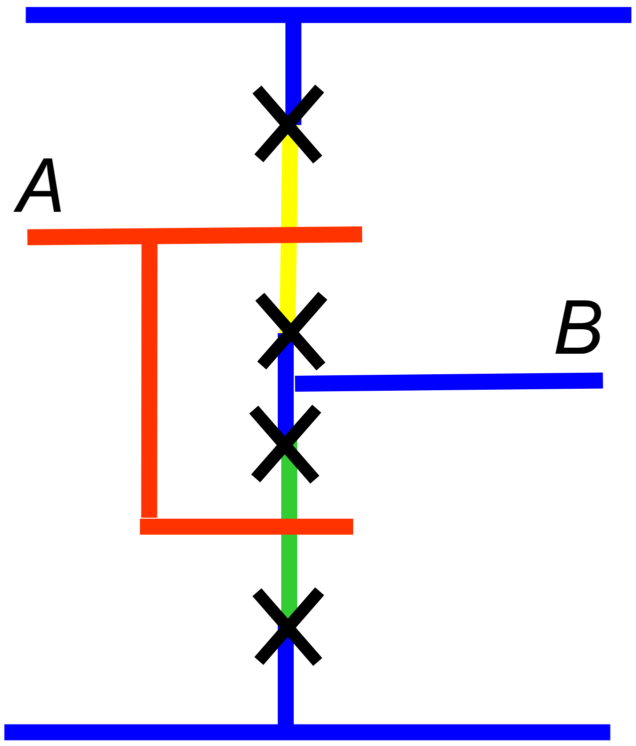
A stick diagram is not a layout but gives the basic structure (including location,, orientation and interconnects) that will be instantiated in the actual layout itself

Modifications can be made much more quickly on a stick diagram than on a layout

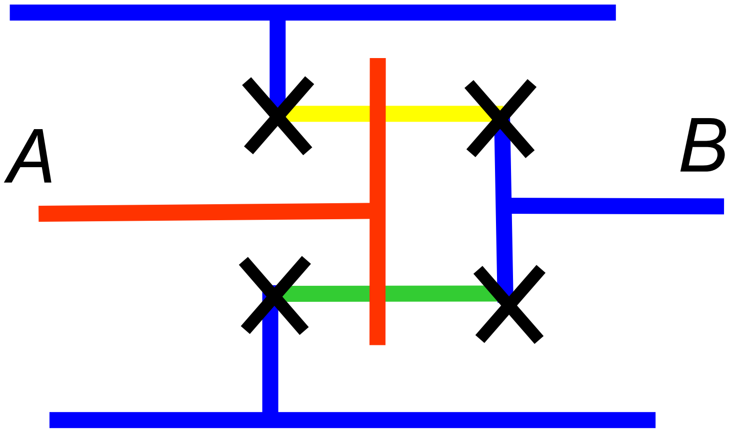
Iteration may be needed to come up with a good layout structure

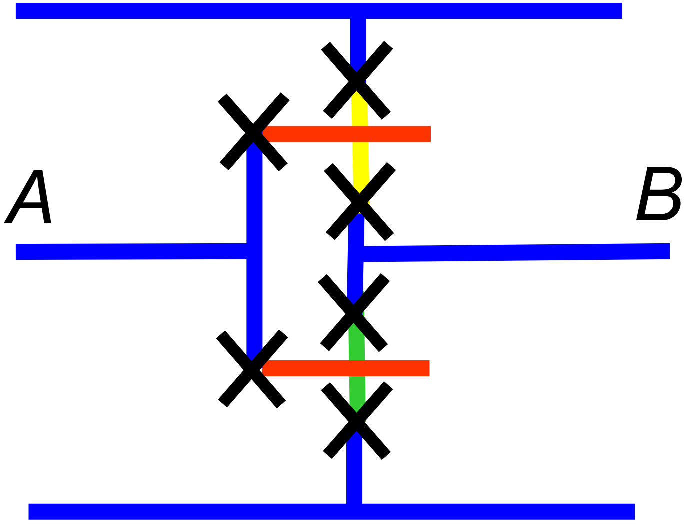
Stick Diagram



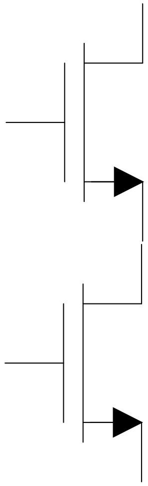


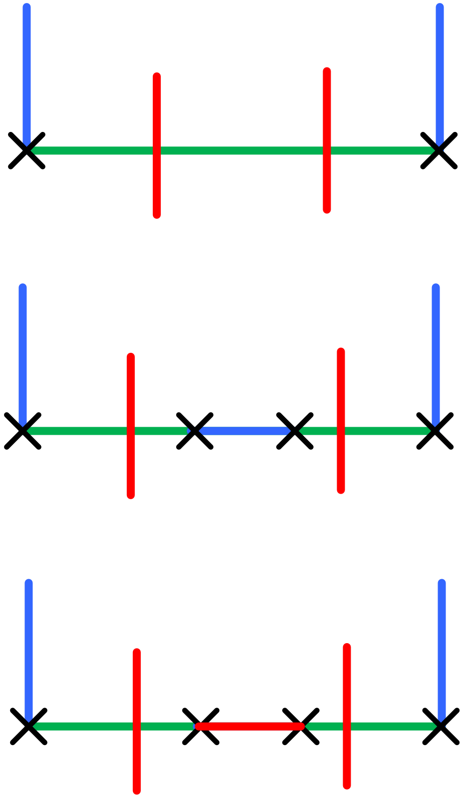
Alternate Representations





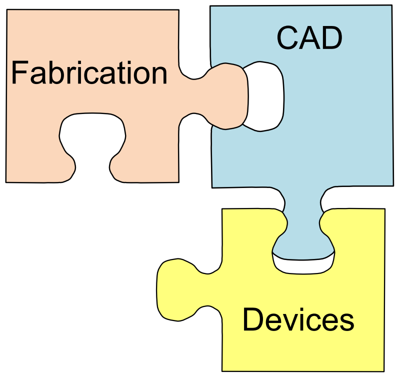
Stick Diagram





- Source and drain notation suppressed
- Shared active can serve as interconnect
- No contact needed to shared active
- Multiple ways to layout even simple circuits

Technology Files



- Provide Information About Process
  - Process Flow (Fabrication Technology)
  - Model Parameters
  - Design Rules
- Serve as Interface Between Design Engineer and Process Engineer
- Insist on getting information that is deemed important for a design
  - Limited information available in academia
  - Foundries often sensitive to who gets access to information
  - Customer success and satisfaction is critical to foundries

Technology Files

- Design Rules
- Process Flow (Fabrication Technology) (will discuss next)
- Model Parameters (will discuss in substantially more detail after device operation and more advanced models are introduced)

First – A preview of what the technology files look like !

Typical Design Rules

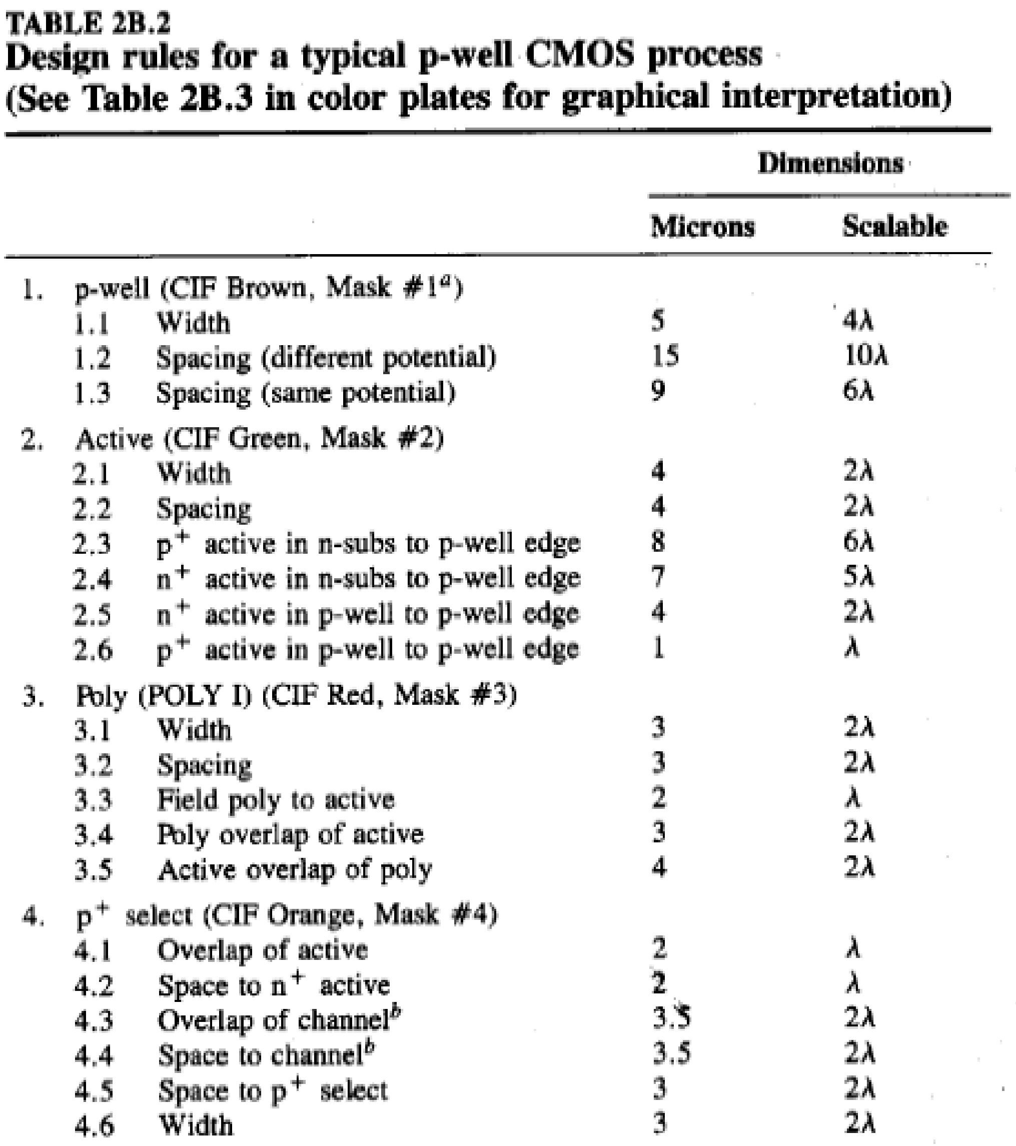


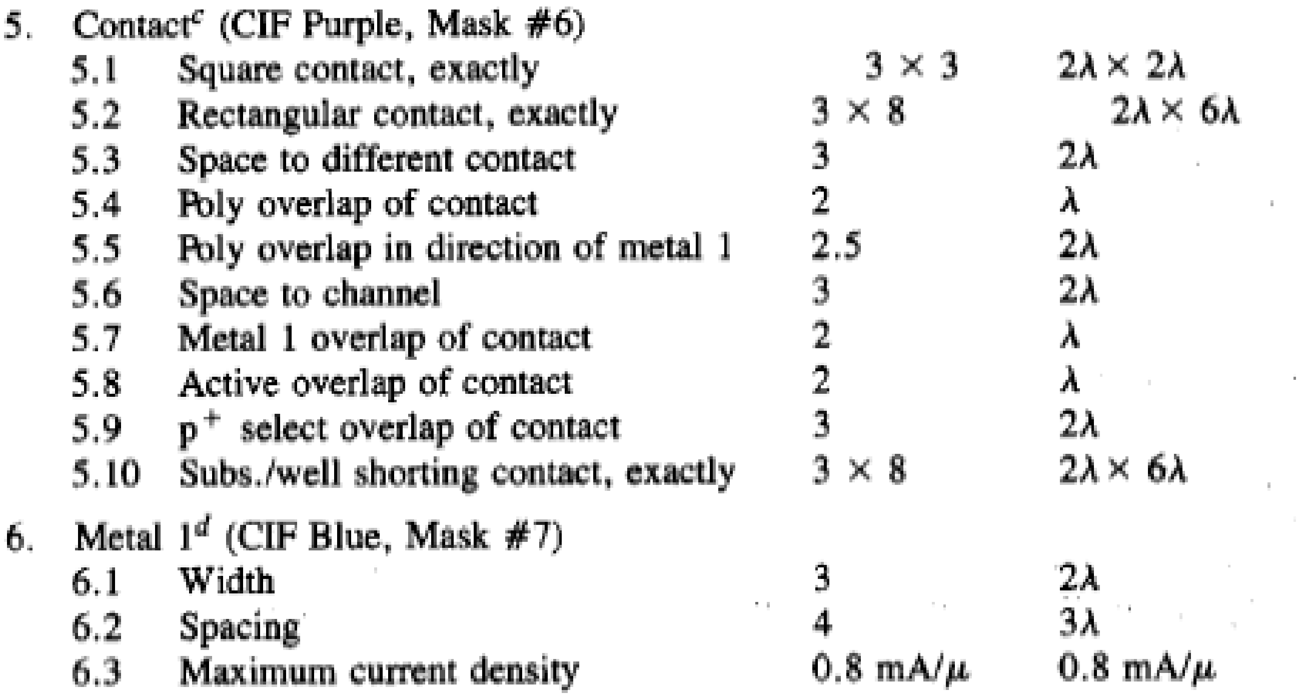
TABLE 2B.2

Design rules for a typical p-well CMOS process

(See Table 2B.3 in color plates for graphical interpretation)

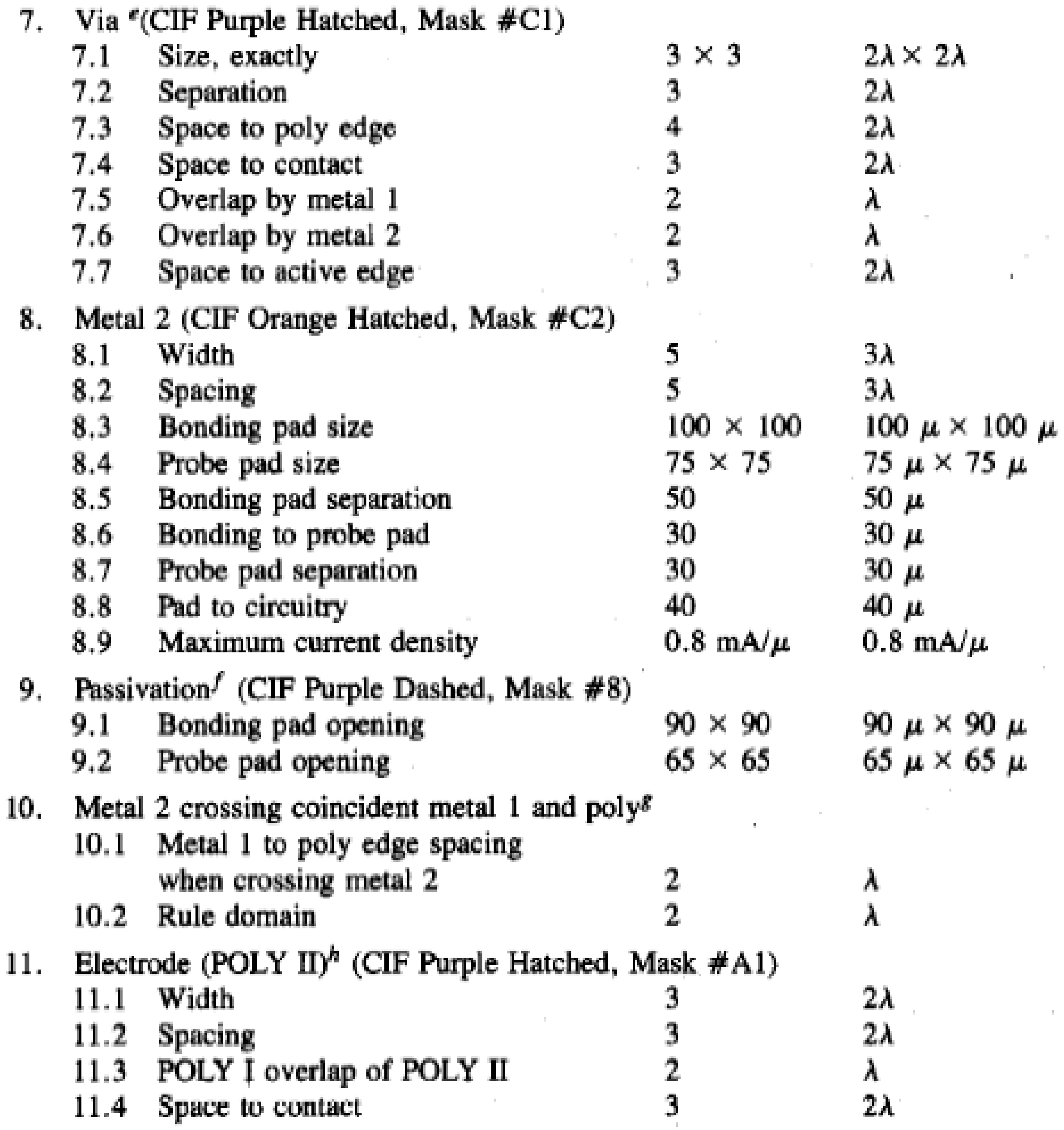
		Dimensions	
		Microns	**Scalable**
1.	p-well (CIF Brown, Mask #1[a])		
1.1	Width	5	4λ
1.2	Spacing (different potential)	15	10λ
1.3	Spacing (same potential)	9	6λ
2.	Active (CIF Green, Mask #2)		
2.1	Width	4	2λ
2.2	Spacing	4	2λ
2.3	p^+ active in n-subs to p-well edge	8	6λ
2.4	n^+ active in n-subs to p-well edge	7	5λ
2.5	n^+ active in p-well to p-well edge	4	2λ
2.6	p^+ active in p-well to p-well edge	1	λ
3.	Poly (POLY I) (CIF Red, Mask #3)		
3.1	Width	3	2λ
3.2	Spacing	3	2λ
3.3	Field poly to active	2	λ
3.4	Poly overlap of active	3	2λ
3.5	Active overlap of poly	4	2λ
4.	p^+ select (CIF Orange, Mask #4)		
4.1	Overlap of active	2	λ
4.2	Space to n^+ active	2	λ
4.3	Overlap of channel[b]	3.5	2λ
4.4	Space to channel[b]	3.5	2λ
4.5	Space to p^+ select	3	2λ
4.6	Width	3	2λ

Typical Design Rules (cont)



5.	Contact[c] (CIF Purple, Mask #6)		
5.1	Square contact, exactly	3 × 3	2λ × 2λ
5.2	Rectangular contact, exactly	3 × 8	2λ × 6λ
5.3	Space to different contact	3	2λ
5.4	Poly overlap of contact	2	λ
5.5	Poly overlap in direction of metal 1	2.5	2λ
5.6	Space to channel	3	2λ
5.7	Metal 1 overlap of contact	2	λ
5.8	Active overlap of contact	2	λ
5.9	p^+ select overlap of contact	3	2λ
5.10	Subs./well shorting contact, exactly	3 × 8	2λ × 6λ
6.	Metal 1[d] (CIF Blue, Mask #7)		
6.1	Width	3	2λ
6.2	Spacing	4	3λ
6.3	Maximum current density	0.8 mA/μ	0.8 mA/μ

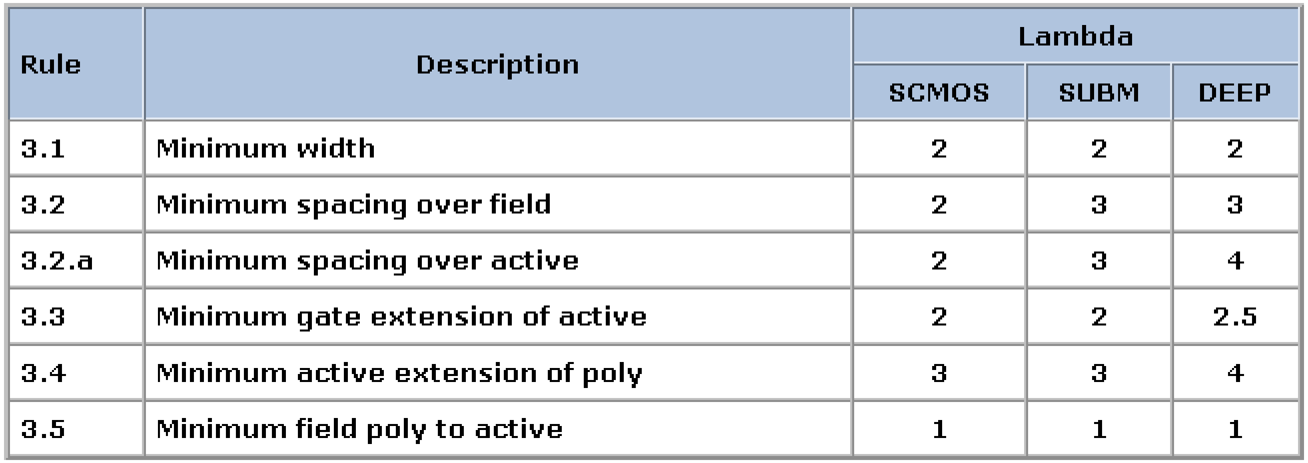
Typical Design Rules (cont)



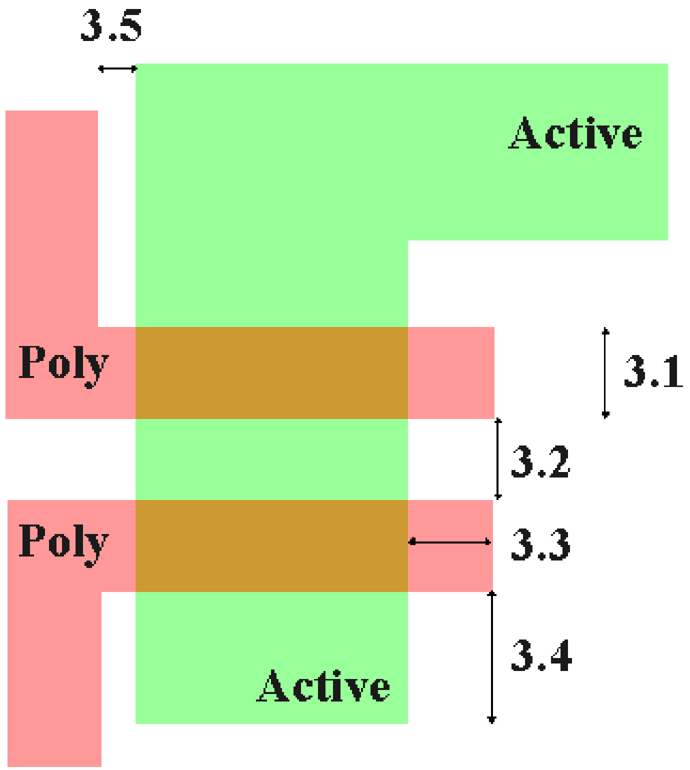
7.	Via [e](CIF Purple Hatched, Mask #C1)		
7.1	Size, exactly	3 × 3	$2\lambda \times 2\lambda$
7.2	Separation	3	2λ
7.3	Space to poly edge	4	2λ
7.4	Space to contact	3	2λ
7.5	Overlap by metal 1	2	λ
7.6	Overlap by metal 2	2	λ
7.7	Space to active edge	3	2λ
8.	Metal 2 (CIF Orange Hatched, Mask #C2)		
8.1	Width	5	3λ
8.2	Spacing	5	3λ
8.3	Bonding pad size	100 × 100	100 μ × 100 μ
8.4	Probe pad size	75 × 75	75 μ × 75 μ
8.5	Bonding pad separation	50	50 μ
8.6	Bonding to probe pad	30	30 μ
8.7	Probe pad separation	30	30 μ
8.8	Pad to circuitry	40	40 μ
8.9	Maximum current density	0.8 mA/μ	0.8 mA/μ
9.	Passivation[f] (CIF Purple Dashed, Mask #8)		
9.1	Bonding pad opening	90 × 90	90 μ × 90 μ
9.2	Probe pad opening	65 × 65	65 μ × 65 μ
10.	Metal 2 crossing coincident metal 1 and poly[g]		
10.1	Metal 1 to poly edge spacing when crossing metal 2	2	λ
10.2	Rule domain	2	λ
11.	Electrode (POLY II)[h] (CIF Purple Hatched, Mask #A1)		
11.1	Width	3	2λ
11.2	Spacing	3	2λ
11.3	POLY I overlap of POLY II	2	λ
11.4	Space to contact	3	2λ

Typical Design Rules (cont)

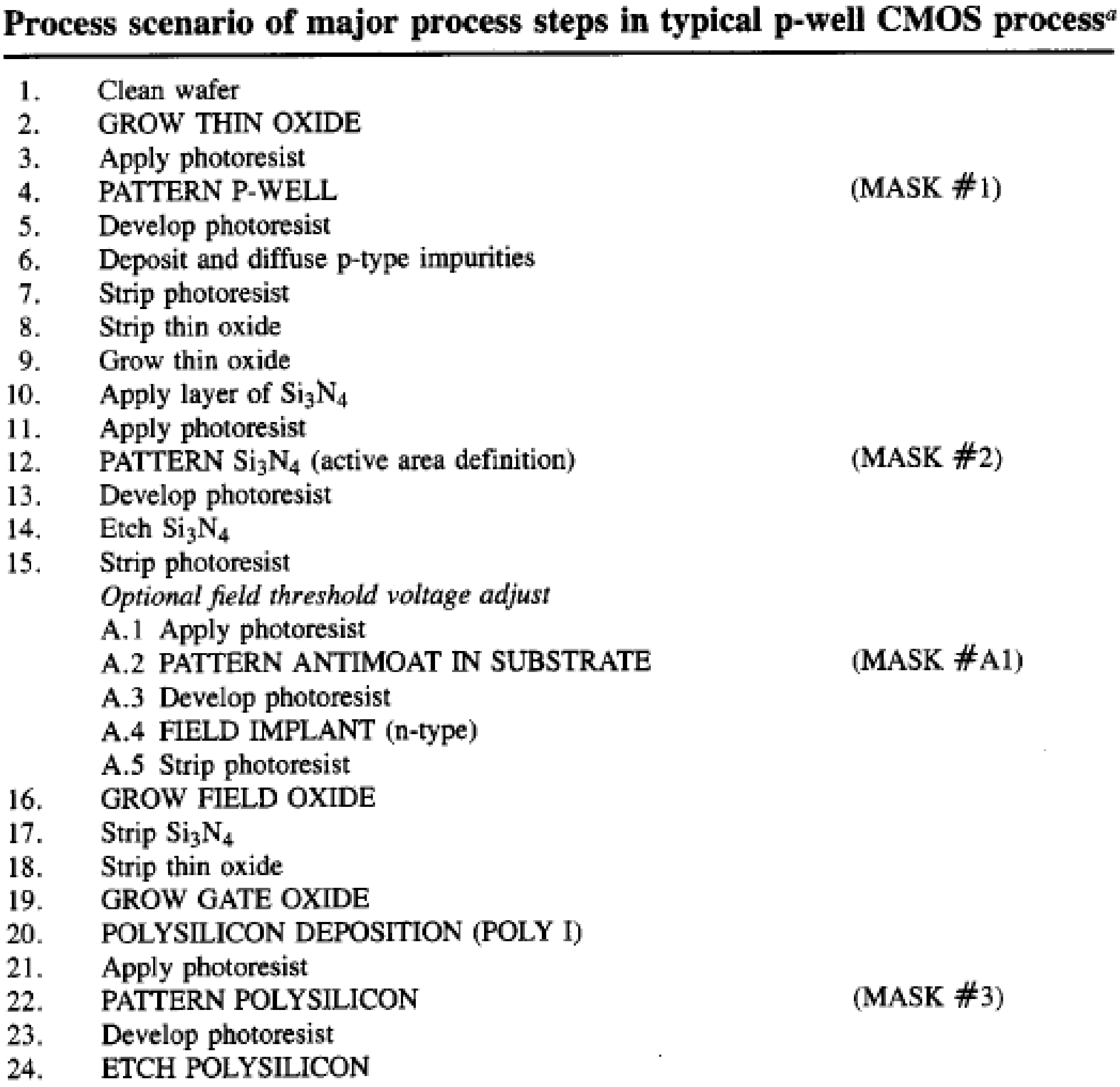
SCMOS Layout Rules - Poly



Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
3.1	Minimum width	2	2	2
3.2	Minimum spacing over field	2	3	3
3.2.a	Minimum spacing over active	2	3	4
3.3	Minimum gate extension of active	2	2	2.5
3.4	Minimum active extension of poly	3	3	4
3.5	Minimum field poly to active	1	1	1



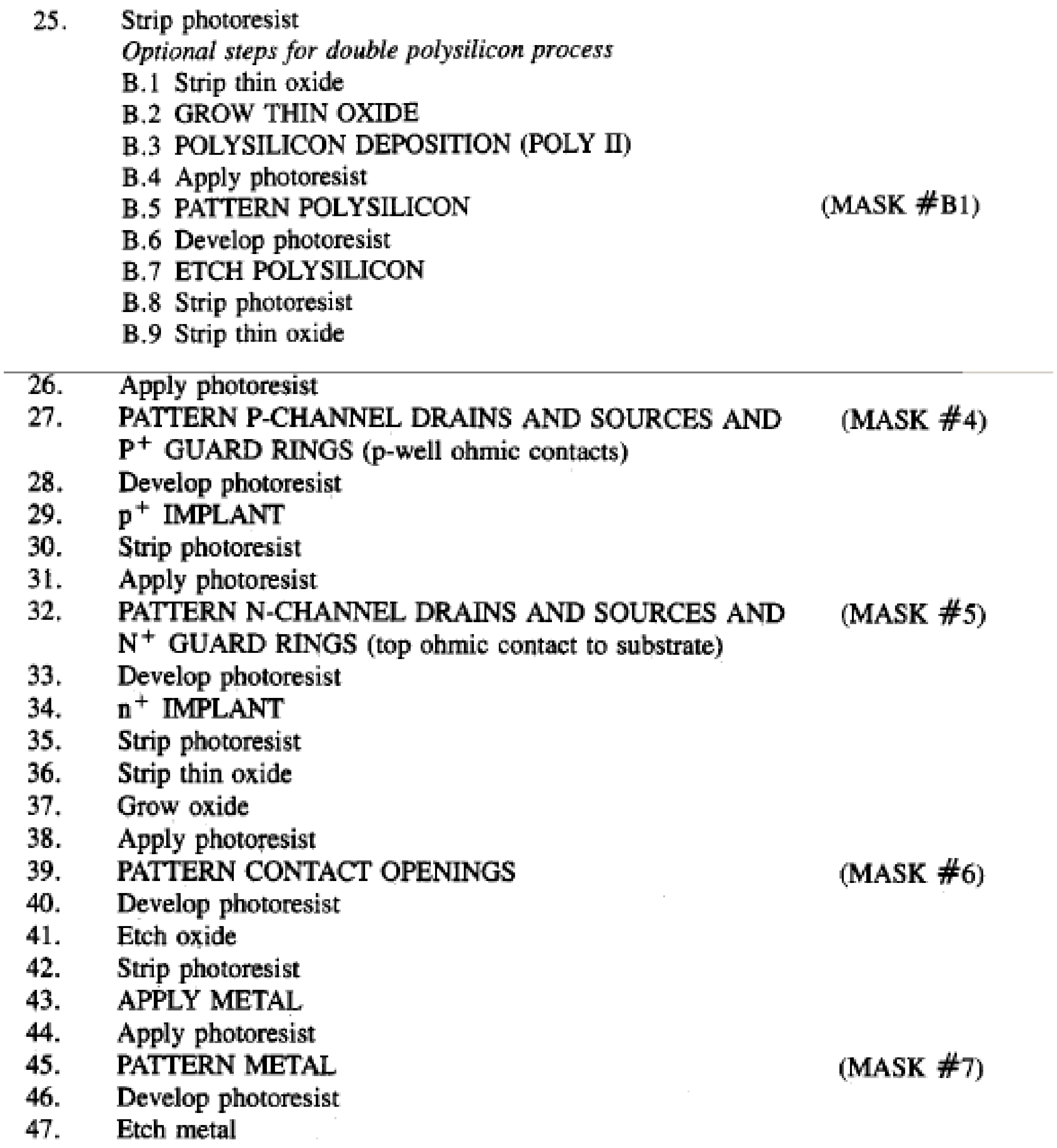
Typical Process Description



Process scenario of major process steps in typical p-well CMOS process[a]

1.	Clean wafer	
2.	GROW THIN OXIDE	
3.	Apply photoresist	
4.	PATTERN P-WELL	(MASK #1)
5.	Develop photoresist	
6.	Deposit and diffuse p-type impurities	
7.	Strip photoresist	
8.	Strip thin oxide	
9.	Grow thin oxide	
10.	Apply layer of Si_3N_4	
11.	Apply photoresist	
12.	PATTERN Si_3N_4 (active area definition)	(MASK #2)
13.	Develop photoresist	
14.	Etch Si_3N_4	
15.	Strip photoresist	
	Optional field threshold voltage adjust	
	A.1 Apply photoresist	
	A.2 PATTERN ANTIMOAT IN SUBSTRATE	(MASK #A1)
	A.3 Develop photoresist	
	A.4 FIELD IMPLANT (n-type)	
	A.5 Strip photoresist	
16.	GROW FIELD OXIDE	
17.	Strip Si_3N_4	
18.	Strip thin oxide	
19.	GROW GATE OXIDE	
20.	POLYSILICON DEPOSITION (POLY I)	
21.	Apply photoresist	
22.	PATTERN POLYSILICON	(MASK #3)
23.	Develop photoresist	
24.	ETCH POLYSILICON	

Typical Process Description (cont)



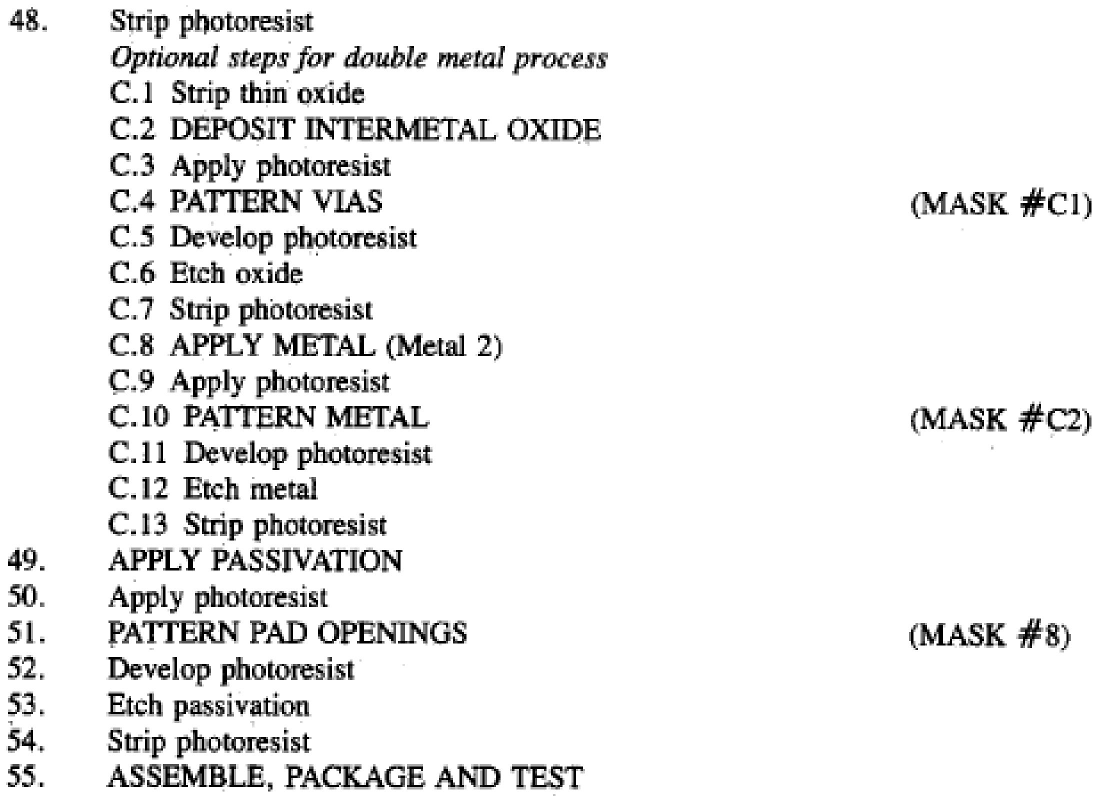
25. Strip photoresist

Optional steps for double polysilicon process

B.1 Strip thin oxide
B.2 GROW THIN OXIDE
B.3 POLYSILICON DEPOSITION (POLY II)
B.4 Apply photoresist
B.5 PATTERN POLYSILICON (MASK #B1)
B.6 Develop photoresist
B.7 ETCH POLYSILICON
B.8 Strip photoresist
B.9 Strip thin oxide

26. Apply photoresist
27. PATTERN P-CHANNEL DRAINS AND SOURCES AND P^+ GUARD RINGS (p-well ohmic contacts) (MASK #4)
28. Develop photoresist
29. p^+ IMPLANT
30. Strip photoresist
31. Apply photoresist
32. PATTERN N-CHANNEL DRAINS AND SOURCES AND N^+ GUARD RINGS (top ohmic contact to substrate) (MASK #5)
33. Develop photoresist
34. n^+ IMPLANT
35. Strip photoresist
36. Strip thin oxide
37. Grow oxide
38. Apply photoresist
39. PATTERN CONTACT OPENINGS (MASK #6)
40. Develop photoresist
41. Etch oxide
42. Strip photoresist
43. APPLY METAL
44. Apply photoresist
45. PATTERN METAL (MASK #7)
46. Develop photoresist
47. Etch metal

Typical Process Description (cont)



48. Strip photoresist

Optional steps for double metal process

C.1 Strip thin oxide

C.2 DEPOSIT INTERMETAL OXIDE

C.3 Apply photoresist

C.4 PATTERN VIAS (MASK #C1)

C.5 Develop photoresist

C.6 Etch oxide

C.7 Strip photoresist

C.8 APPLY METAL (Metal 2)

C.9 Apply photoresist

C.10 PATTERN METAL (MASK #C2)

C.11 Develop photoresist

C.12 Etch metal

C.13 Strip photoresist

49. APPLY PASSIVATION

50. Apply photoresist

51. PATTERN PAD OPENINGS (MASK #8)

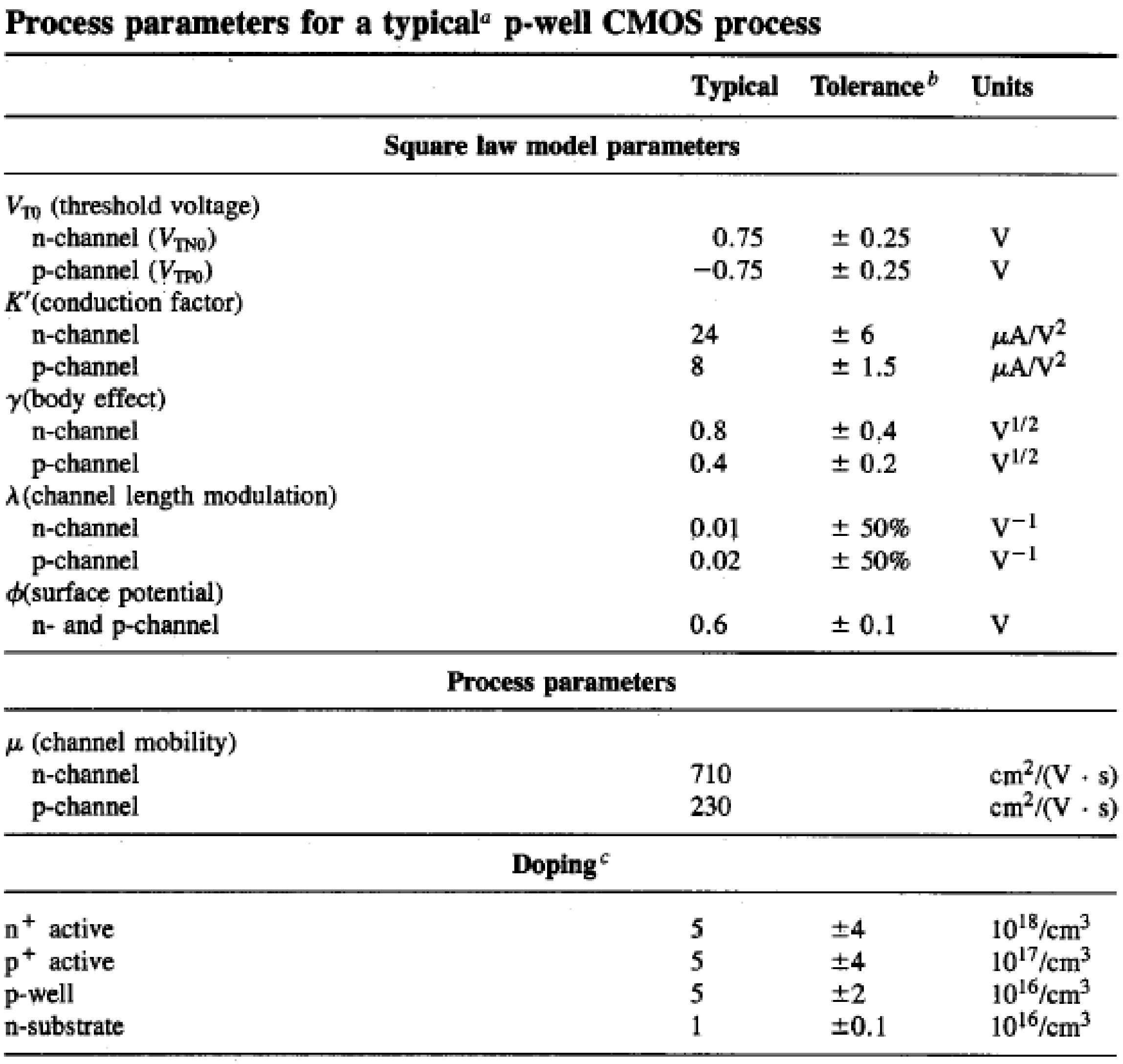
52. Develop photoresist

53. Etch passivation

54. Strip photoresist

55. ASSEMBLE, PACKAGE AND TEST

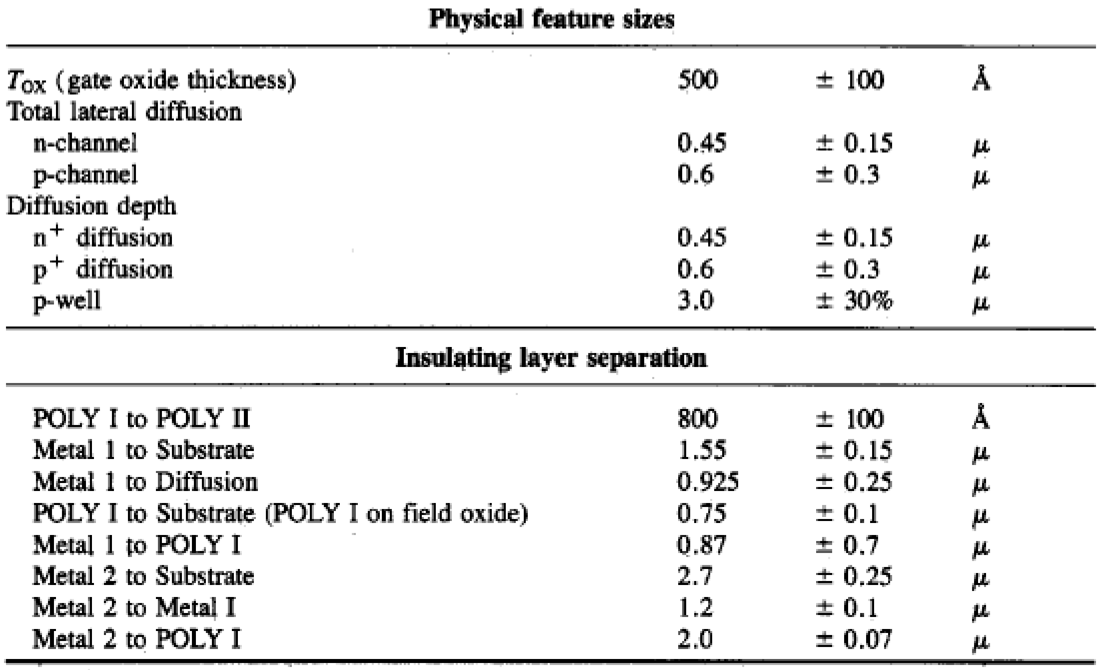
Typical Model Parameters



Process parameters for a typical[a] p-well CMOS process

	Typical	Tolerance[b]	Units
Square law model parameters			
V_{T0} (threshold voltage)			
n-channel (V_{TN0})	0.75	± 0.25	V
p-channel (V_{TP0})	−0.75	± 0.25	V
K' (conduction factor)			
n-channel	24	± 6	$\mu A/V^2$
p-channel	8	± 1.5	$\mu A/V^2$
γ (body effect)			
n-channel	0.8	± 0.4	$V^{1/2}$
p-channel	0.4	± 0.2	$V^{1/2}$
λ (channel length modulation)			
n-channel	0.01	± 50%	V^{-1}
p-channel	0.02	± 50%	V^{-1}
ϕ (surface potential)			
n- and p-channel	0.6	± 0.1	V
Process parameters			
μ (channel mobility)			
n-channel	710		$cm^2/(V \cdot s)$
p-channel	230		$cm^2/(V \cdot s)$
Doping[c]			
n^+ active	5	±4	$10^{18}/cm^3$
p^+ active	5	±4	$10^{17}/cm^3$
p-well	5	±2	$10^{16}/cm^3$
n-substrate	1	±0.1	$10^{16}/cm^3$

Typical Model Parameters (cont)



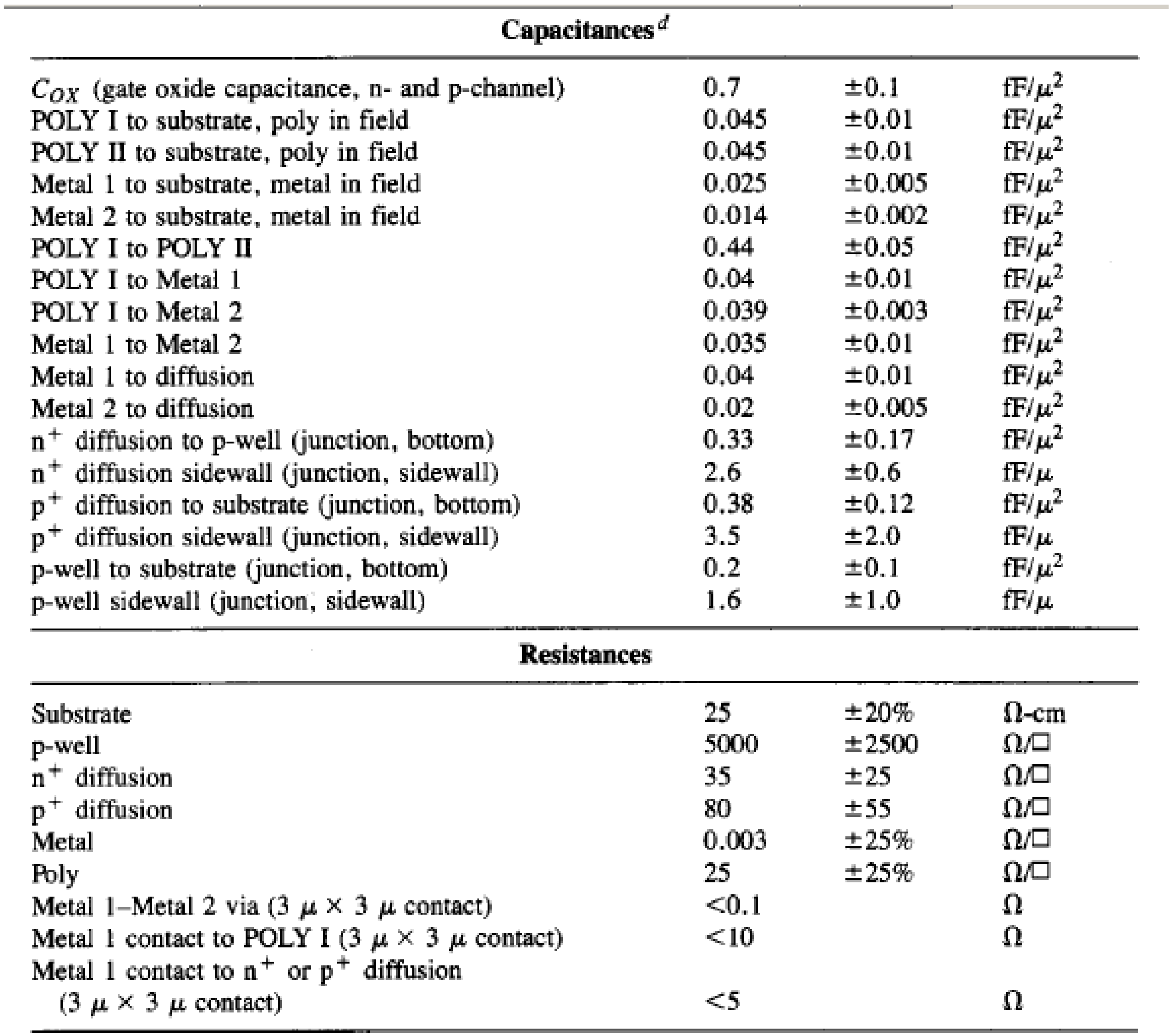
Physical feature sizes

T_{OX} (gate oxide thickness)	500	± 100	Å
Total lateral diffusion			
n-channel	0.45	± 0.15	μ
p-channel	0.6	± 0.3	μ
Diffusion depth			
n^+ diffusion	0.45	± 0.15	μ
p^+ diffusion	0.6	± 0.3	μ
p-well	3.0	± 30%	μ

Insulating layer separation

POLY I to POLY II	800	± 100	Å
Metal 1 to Substrate	1.55	± 0.15	μ
Metal 1 to Diffusion	0.925	± 0.25	μ
POLY I to Substrate (POLY I on field oxide)	0.75	± 0.1	μ
Metal 1 to POLY I	0.87	± 0.7	μ
Metal 2 to Substrate	2.7	± 0.25	μ
Metal 2 to Metal I	1.2	± 0.1	μ
Metal 2 to POLY I	2.0	± 0.07	μ

Typical Model Parameters (cont)



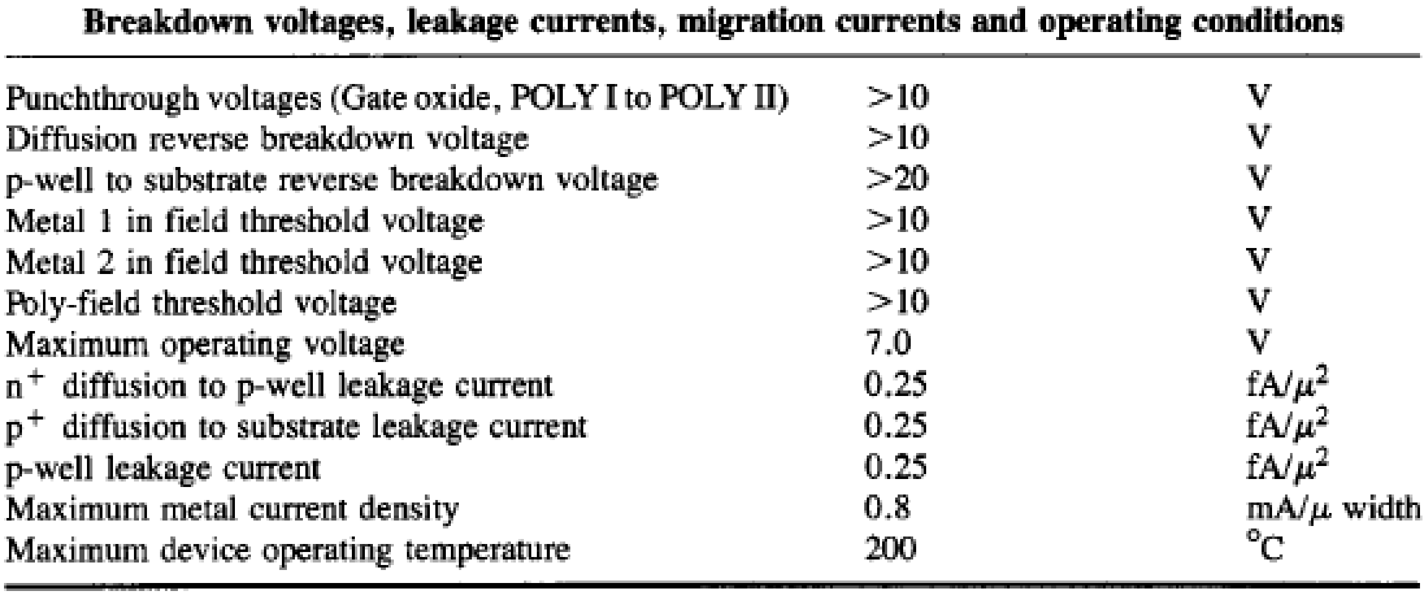
Capacitances^d

C_{OX} (gate oxide capacitance, n- and p-channel)	0.7	±0.1	fF/μ^2
POLY I to substrate, poly in field	0.045	±0.01	fF/μ^2
POLY II to substrate, poly in field	0.045	±0.01	fF/μ^2
Metal 1 to substrate, metal in field	0.025	±0.005	fF/μ^2
Metal 2 to substrate, metal in field	0.014	±0.002	fF/μ^2
POLY I to POLY II	0.44	±0.05	fF/μ^2
POLY I to Metal 1	0.04	±0.01	fF/μ^2
POLY I to Metal 2	0.039	±0.003	fF/μ^2
Metal 1 to Metal 2	0.035	±0.01	fF/μ^2
Metal 1 to diffusion	0.04	±0.01	fF/μ^2
Metal 2 to diffusion	0.02	±0.005	fF/μ^2
n^+ diffusion to p-well (junction, bottom)	0.33	±0.17	fF/μ^2
n^+ diffusion sidewall (junction, sidewall)	2.6	±0.6	fF/μ
p^+ diffusion to substrate (junction, bottom)	0.38	±0.12	fF/μ^2
p^+ diffusion sidewall (junction, sidewall)	3.5	±2.0	fF/μ
p-well to substrate (junction, bottom)	0.2	±0.1	fF/μ^2
p-well sidewall (junction, sidewall)	1.6	±1.0	fF/μ

Resistances

Substrate	25	±20%	Ω-cm
p-well	5000	±2500	Ω/□
n^+ diffusion	35	±25	Ω/□
p^+ diffusion	80	±55	Ω/□
Metal	0.003	±25%	Ω/□
Poly	25	±25%	Ω/□
Metal 1–Metal 2 via (3 μ × 3 μ contact)	<0.1		Ω
Metal 1 contact to POLY I (3 μ × 3 μ contact)	<10		Ω
Metal 1 contact to n^+ or p^+ diffusion (3 μ × 3 μ contact)	<5		Ω

Typical Model Parameters (cont)

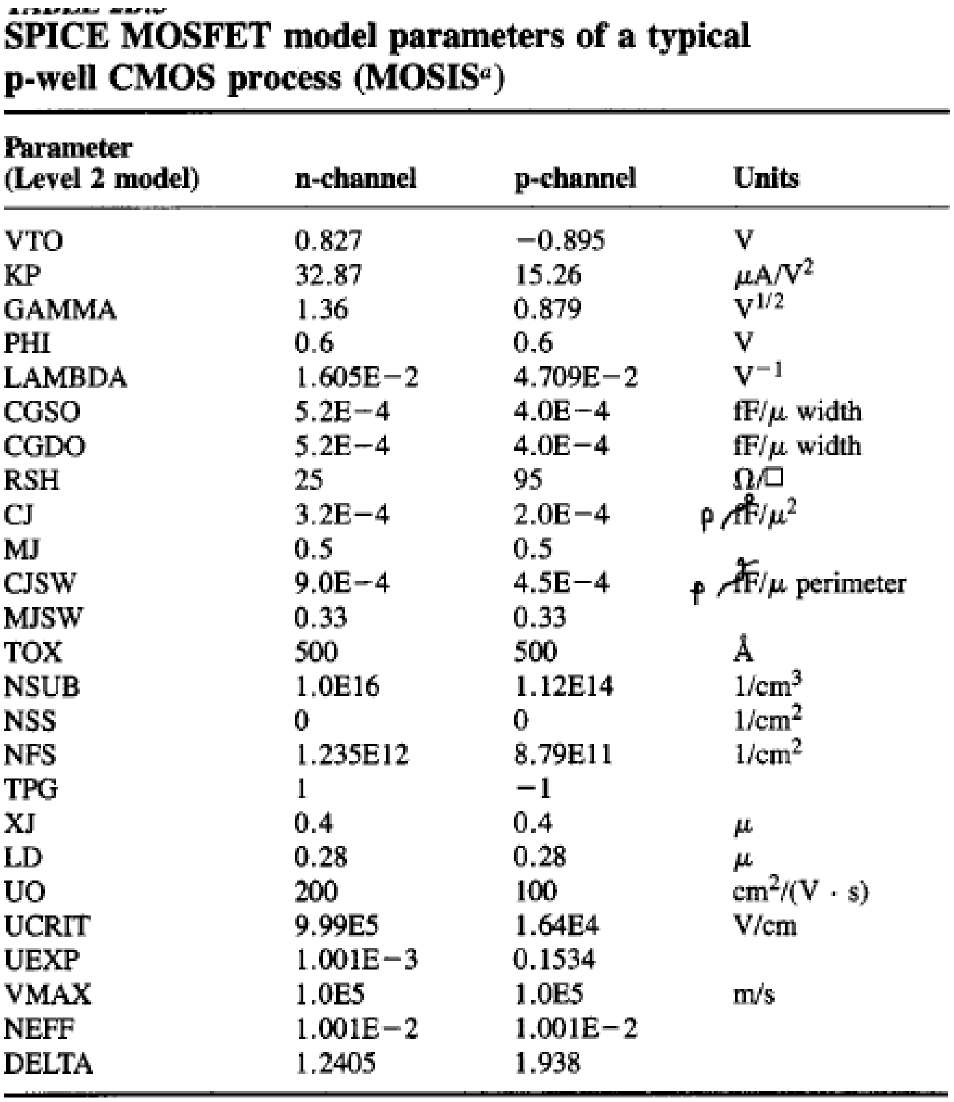


Breakdown voltages, leakage currents, migration currents and operating conditions

Punchthrough voltages (Gate oxide, POLY I to POLY II)	>10	V
Diffusion reverse breakdown voltage	>10	V
p-well to substrate reverse breakdown voltage	>20	V
Metal 1 in field threshold voltage	>10	V
Metal 2 in field threshold voltage	>10	V
Poly-field threshold voltage	>10	V
Maximum operating voltage	7.0	V
n^+ diffusion to p-well leakage current	0.25	fA/μ^2
p^+ diffusion to substrate leakage current	0.25	fA/μ^2
p-well leakage current	0.25	fA/μ^2
Maximum metal current density	0.8	mA/μ width
Maximum device operating temperature	200	°C

Typical Model Parameters (cont)

Level 3 Model (n-ch and p-ch)



SPICE MOSFET model parameters of a typical p-well CMOS process (MOSIS[a])

Parameter (Level 2 model)	n-channel	p-channel	Units
VTO	0.827	−0.895	V
KP	32.87	15.26	$\mu A/V^2$
GAMMA	1.36	0.879	$V^{1/2}$
PHI	0.6	0.6	V
LAMBDA	1.605E−2	4.709E−2	V^{-1}
CGSO	5.2E−4	4.0E−4	fF/μ width
CGDO	5.2E−4	4.0E−4	fF/μ width
RSH	25	95	$\Omega/\square$
CJ	3.2E−4	2.0E−4	p ~~f~~F/μ^2
MJ	0.5	0.5	
CJSW	9.0E−4	4.5E−4	p ~~f~~F/μ perimeter
MJSW	0.33	0.33	
TOX	500	500	Å
NSUB	1.0E16	1.12E14	$1/cm^3$
NSS	0	0	$1/cm^2$
NFS	1.235E12	8.79E11	$1/cm^2$
TPG	1	−1	
XJ	0.4	0.4	μ
LD	0.28	0.28	μ
UO	200	100	$cm^2/(V \cdot s)$
UCRIT	9.99E5	1.64E4	V/cm
UEXP	1.001E−3	0.1534	
VMAX	1.0E5	1.0E5	m/s
NEFF	1.001E−2	1.001E−2	
DELTA	1.2405	1.938	

Typical Model Parameters (cont)

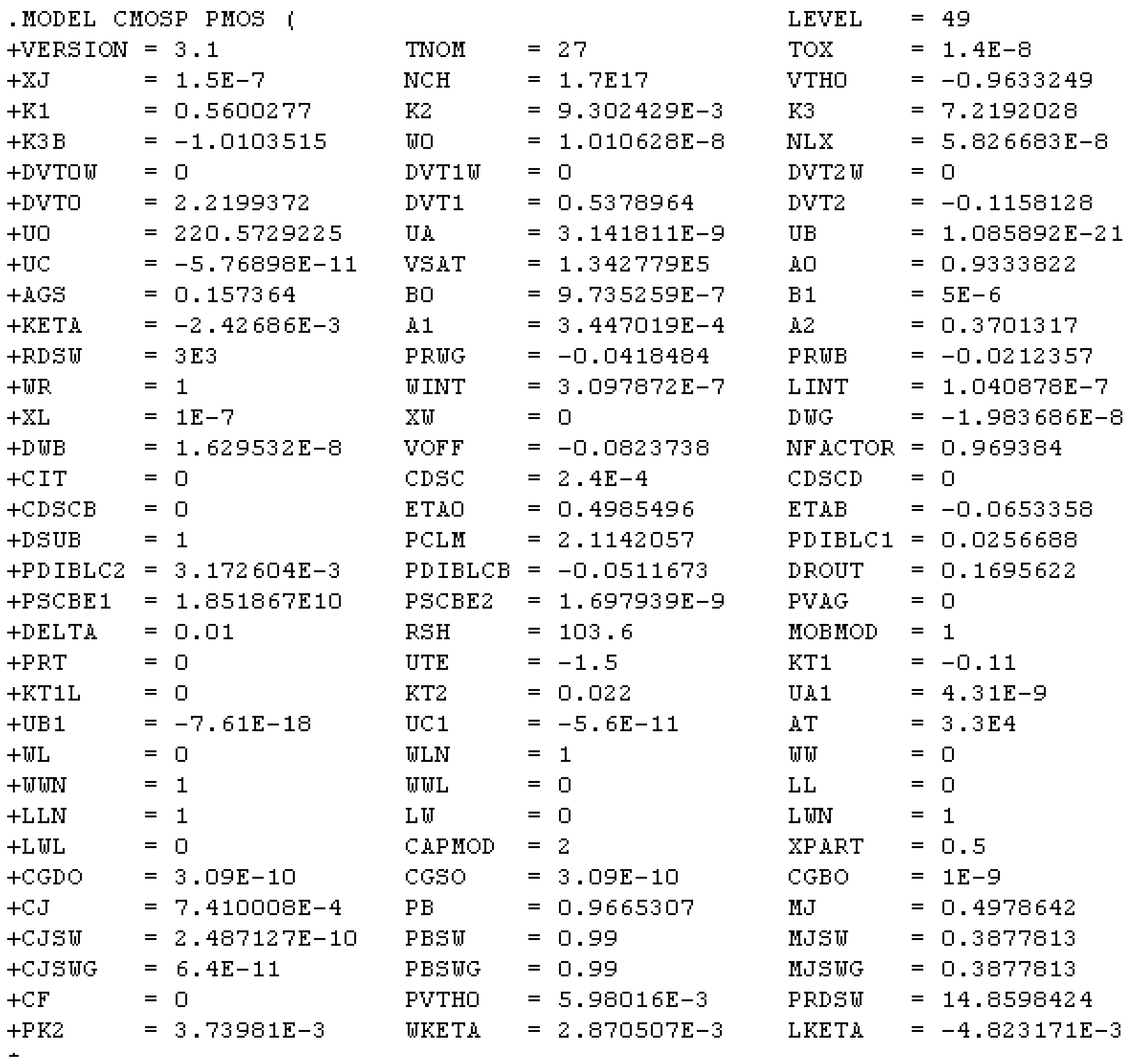
BSIM 4 Model (n-ch)

```
.MODEL CMOSN NMOS (                                 LEVEL    = 49
+VERSION = 3.1             TNOM     = 27            TOX      = 1.4E-8
+XJ      = 1.5E-7          NCH      = 1.7E17        VTH0     = 0.6656437
+K1      = 0.875093        K2       = -0.0943223    K3       = 25.0562441
+K3B     = -8.5140476      W0       = 1.01582E-8    NLX      = 1E-9
+DVT0W   = 0               DVT1W    = 0             DVT2W    = 0
+DVT0    = 2.670658        DVT1     = 0.4282172     DVT2     = -0.1373089
+U0      = 452.3081836     UA       = 3.061716E-13  UB       = 1.515137E-18
+UC      = 1.166279E-11    VSAT     = 1.682414E5    A0       = 0.6297744
+AGS     = 0.1384489       B0       = 2.579158E-6   B1       = 5E-6
+KETA    = -3.615287E-3    A1       = 1.054571E-6   A2       = 0.3379035
+RDSW    = 1.380341E3      PRWG     = 0.0301426     PRWB     = 0.0106493
+WR      = 1               WINT     = 2.594349E-7   LINT     = 7.489566E-8
+XL      = 1E-7            XW       = 0             DWG      = -9.471353E-9
+DWB     = 3.537786E-8     VOFF     = 0             NFACTOR  = 1.0754804
+CIT     = 0               CDSC     = 2.4E-4        CDSCD    = 0
+CDSCB   = 0               ETA0     = 2.332015E-3   ETAB     = -1.531255E-4
+DSUB    = 0.076309        PCLM     = 2.6209353     PDIBLC1  = 1
+PDIBLC2 = 2.23243E-3      PDIBLCB  = -0.0436947    DROUT    = 1.0300278
+PSCBE1  = 6.619472E8      PSCBE2   = 2.968801E-4   PVAG     = 9.970995E-3
+DELTA   = 0.01            RSH      = 80.9          MOBMOD   = 1
+PRT     = 0               UTE      = -1.5          KT1      = -0.11
+KT1L    = 0               KT2      = 0.022         UA1      = 4.31E-9
+UB1     = -7.61E-18       UC1      = -5.6E-11      AT       = 3.3E4
+WL      = 0               WLN      = 1             WW       = 0
+WWN     = 1               WWL      = 0             LL       = 0
+LLN     = 1               LW       = 0             LWN      = 1
+LWL     = 0               CAPMOD   = 2             XPART    = 0.5
+CGDO    = 2.34E-10        CGSO     = 2.34E-10      CGBO     = 1E-9
+CJ      = 4.240724E-4     PB       = 0.9148626     MJ       = 0.4416777
+CJSW    = 3.007134E-10    PBSW     = 0.8           MJSW     = 0.2025106
+CJSWG   = 1.64E-10        PBSWG    = 0.8           MJSWG    = 0.2025106
+CF      = 0               PVTH0    = 0.0526696     PRDSW    = 110.1539295
+PK2     = -0.0283027      WKETA    = -0.0191754    LKETA    = 8.469064E-4
```

98 parameters in this BSIM Model !

Typical Model Parameters (cont)

BSIM 4 Model (p-ch)



```
.MODEL CMOSP PMOS (                                  LEVEL   = 49
+VERSION = 3.1            TNOM    = 27               TOX     = 1.4E-8
+XJ      = 1.5E-7         NCH     = 1.7E17           VTH0    = -0.9633249
+K1      = 0.5600277      K2      = 9.302429E-3      K3      = 7.2192028
+K3B     = -1.0103515     W0      = 1.010628E-8      NLX     = 5.826683E-8
+DVT0W   = 0              DVT1W   = 0                DVT2W   = 0
+DVT0    = 2.2199372      DVT1    = 0.5378964        DVT2    = -0.1158128
+U0      = 220.5729225    UA      = 3.141811E-9      UB      = 1.085892E-21
+UC      = -5.76898E-11   VSAT    = 1.342779E5       A0      = 0.9333822
+AGS     = 0.157364       B0      = 9.735259E-7      B1      = 5E-6
+KETA    = -2.42686E-3    A1      = 3.447019E-4      A2      = 0.3701317
+RDSW    = 3E3            PRWG    = -0.0418484       PRWB    = -0.0212357
+WR      = 1              WINT    = 3.097872E-7      LINT    = 1.040878E-7
+XL      = 1E-7           XW      = 0                DWG     = -1.983686E-8
+DWB     = 1.629532E-8    VOFF    = -0.0823738       NFACTOR = 0.969384
+CIT     = 0              CDSC    = 2.4E-4           CDSCD   = 0
+CDSCB   = 0              ETA0    = 0.4985496        ETAB    = -0.0653358
+DSUB    = 1              PCLM    = 2.1142057        PDIBLC1 = 0.0256688
+PDIBLC2 = 3.172604E-3    PDIBLCB = -0.0511673       DROUT   = 0.1695622
+PSCBE1  = 1.851867E10    PSCBE2  = 1.697939E-9      PVAG    = 0
+DELTA   = 0.01           RSH     = 103.6            MOBMOD  = 1
+PRT     = 0              UTE     = -1.5             KT1     = -0.11
+KT1L    = 0              KT2     = 0.022            UA1     = 4.31E-9
+UB1     = -7.61E-18      UC1     = -5.6E-11         AT      = 3.3E4
+WL      = 0              WLN     = 1                WW      = 0
+WWN     = 1              WWL     = 0                LL      = 0
+LLN     = 1              LW      = 0                LWN     = 1
+LWL     = 0              CAPMOD  = 2                XPART   = 0.5
+CGDO    = 3.09E-10       CGSO    = 3.09E-10         CGBO    = 1E-9
+CJ      = 7.410008E-4    PB      = 0.9665307        MJ      = 0.4978642
+CJSW    = 2.487127E-10   PBSW    = 0.99             MJSW    = 0.3877813
+CJSWG   = 6.4E-11        PBSWG   = 0.99             MJSWG   = 0.3877813
+CF      = 0              PVTH0   = 5.98016E-3       PRDSW   = 14.8598424
+PK2     = 3.73981E-3     WKETA   = 2.870507E-3      LKETA   = -4.823171E-3
+
```

Technology Files

- Design Rules
- Process Flow (Fabrication Technology) (will discuss next)
- Model Parameters (will discuss in substantially more detail after device operation and more advanced models are introduced)

Design Rules

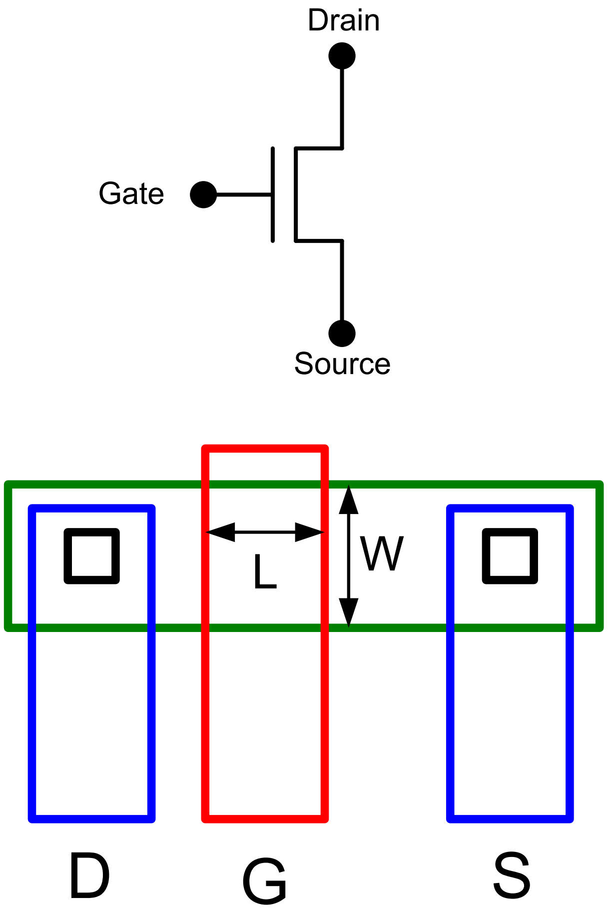
- Give minimum feature sizes, spacing, and other constraints that are acceptable in a process

- Very large number of devices can be reliably made with the design rules of a process

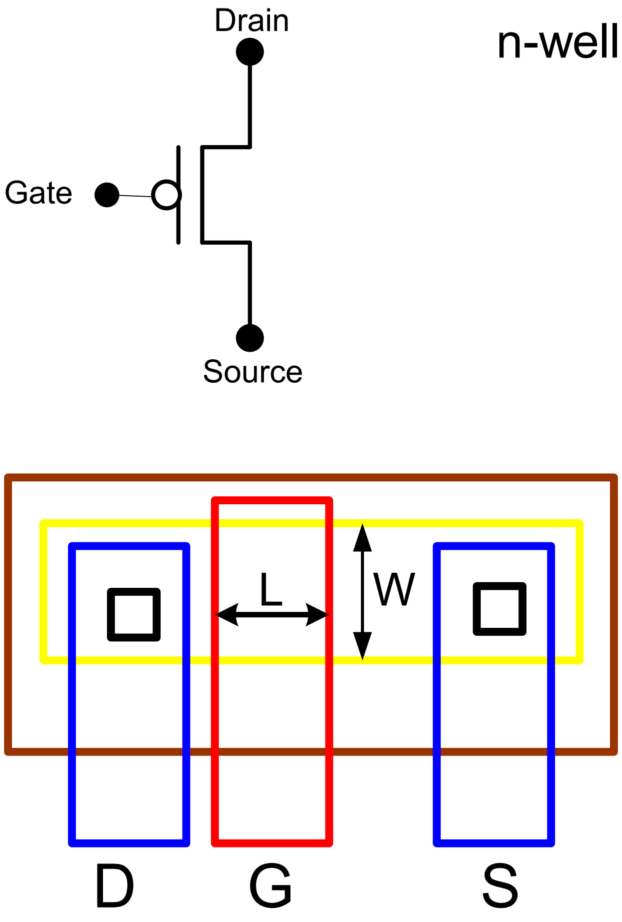
- Yield and performance unpredictable and often low if rules are violated

- Compatible with design rule checker in integrated toolsets

Design Rules and Layout – consider transistors



Layout



Layout

Layer Map

n-well bulk CMOS Process

🟨 p-active

🟩 n-active

🟥 Poly 1

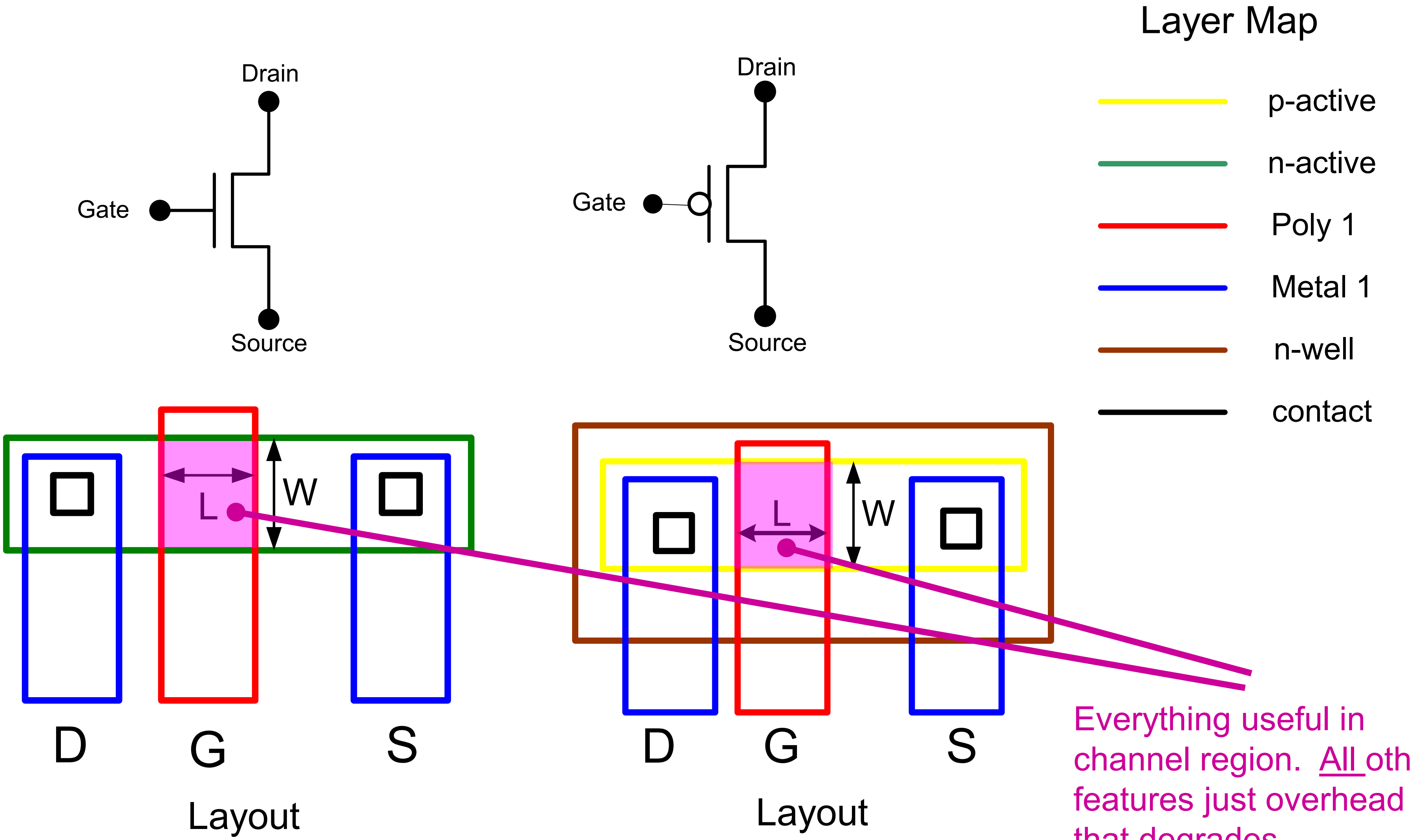
🟦 Metal 1

🟫 n-well

⬛ contact

Layout always represented in a top view in two dimensions

Design Rules and Layout – consider transistors

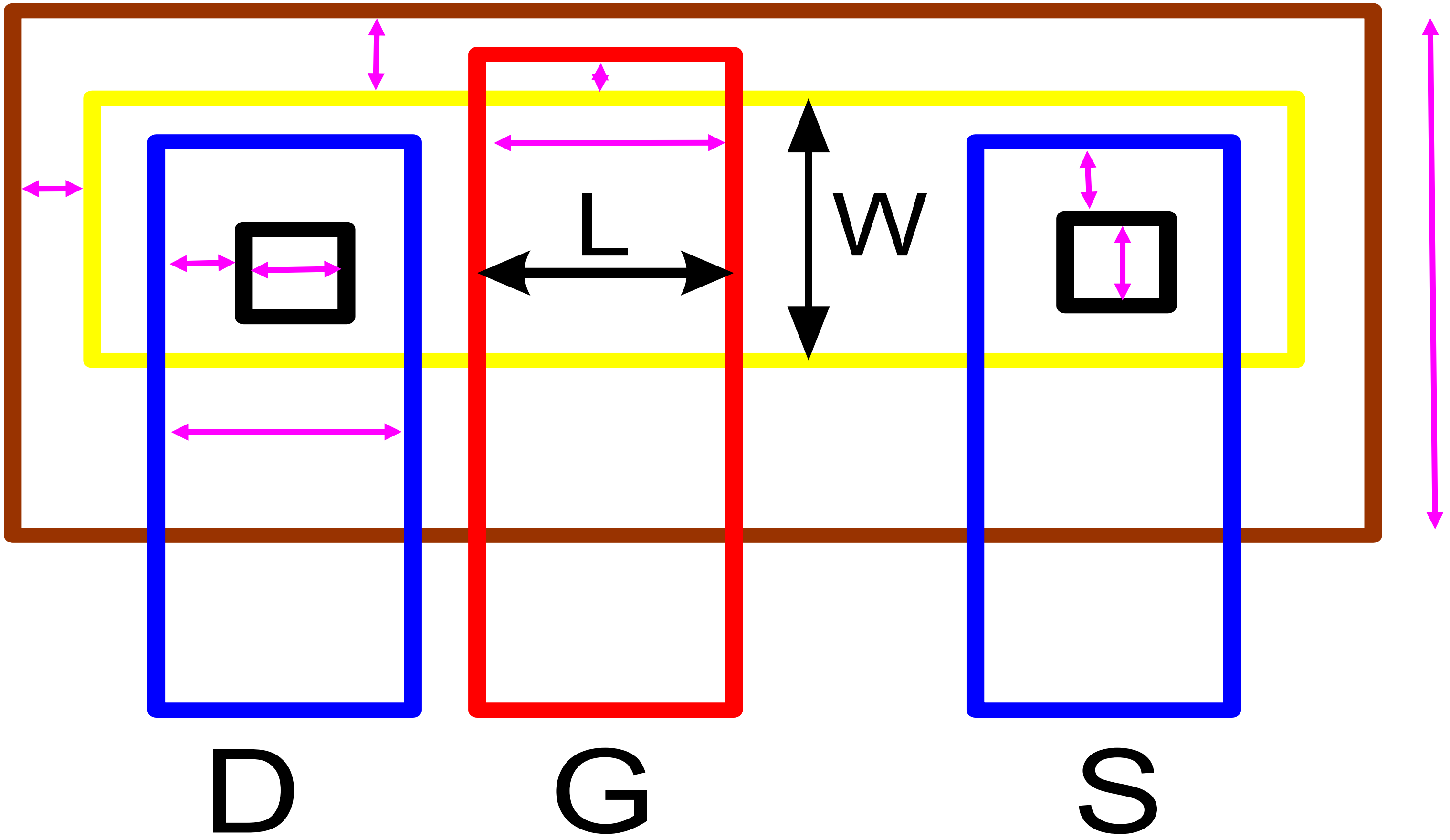


Layer Map

- 🟨 p-active
- 🟩 n-active
- 🟥 Poly 1
- 🟦 Metal 1
- 🟫 n-well
- ⬛ contact

Everything useful in channel region. All other features just overhead that degrades performance

Design Rules

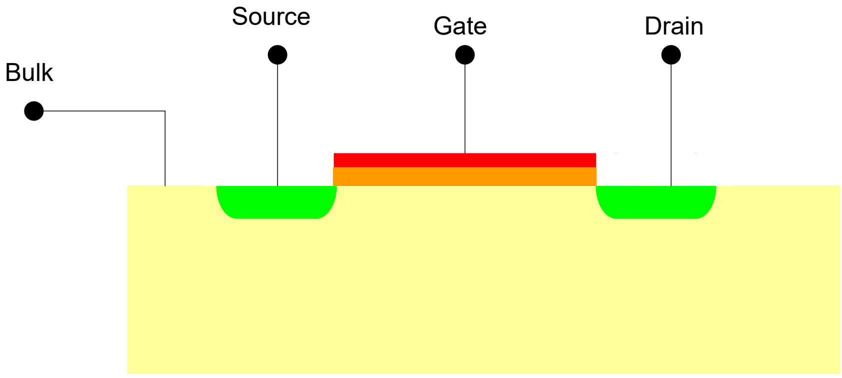


Design rules give minimum feature sizes and spacings

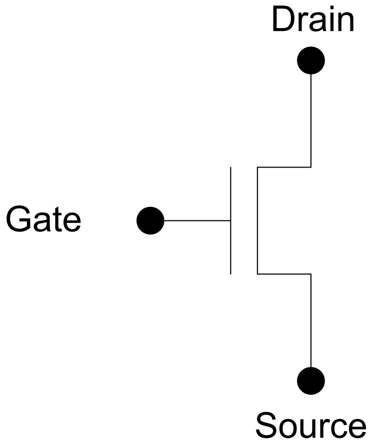
Designers generally do layouts to minimize size of circuit subject to design rule constraints (because yield, cost, and performance usually improve)

MOS Transistor

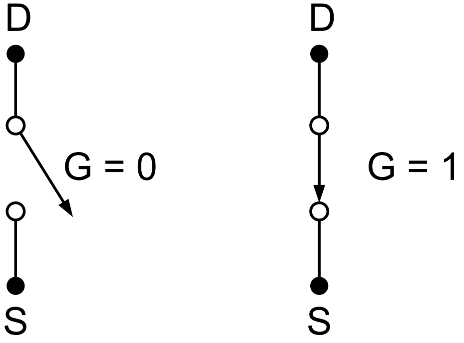
Qualitative Discussion of n-channel Operation



n-channel MOSFET



Equivalent Circuit for n-channel MOSFET

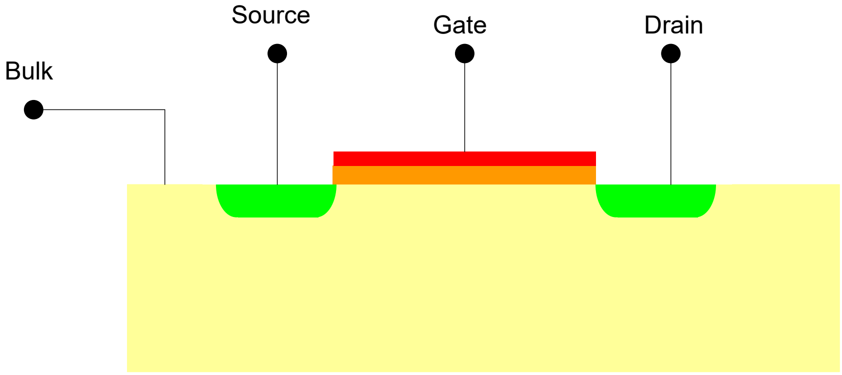


- Source assumed connected to (or close to) ground
- $V_{GS}=0$ denoted as Boolean gate voltage G=0
- $V_{GS}=V_{DD}$ denoted as Boolean gate voltage G=1
- Boolean G is relative to ground potential

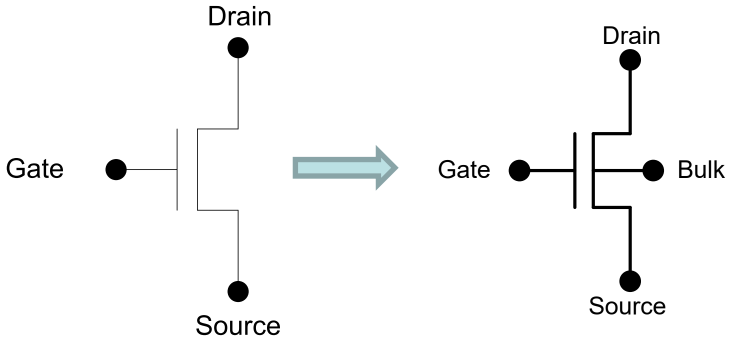
This is the first model we have for the n-channel MOSFET !

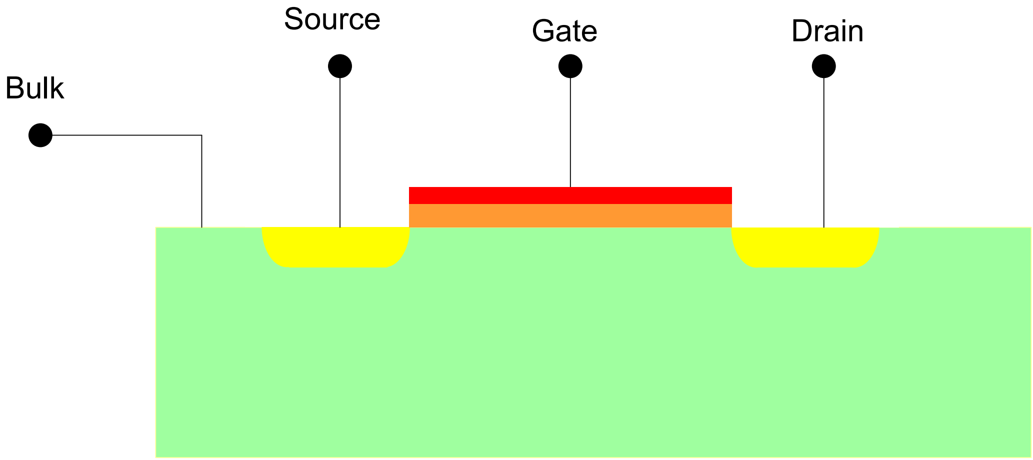
Ideal switch-level model

MOS Transistor

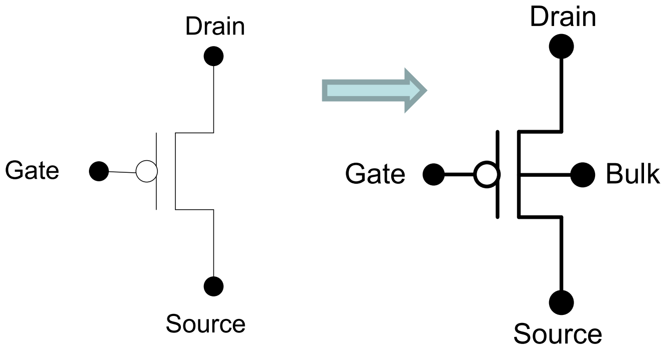


n-channel MOSFET

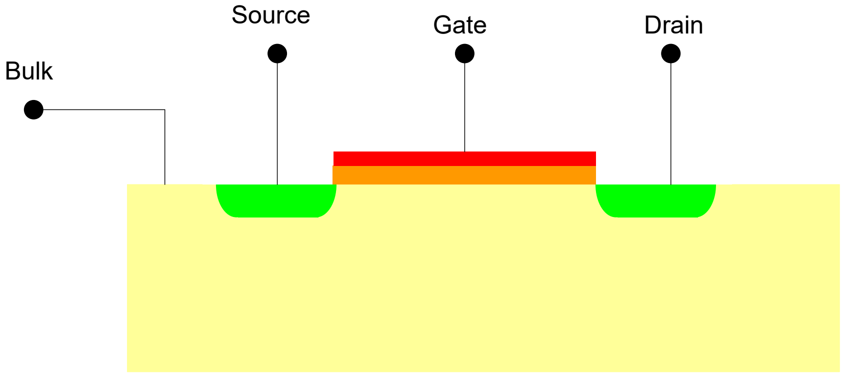




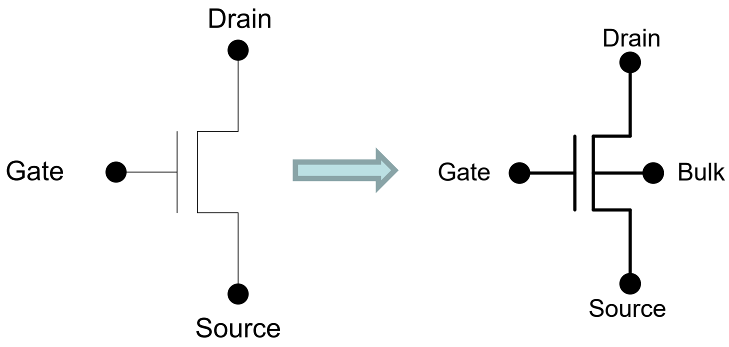
p-channel MOSFET



MOS Transistor Nomenclature



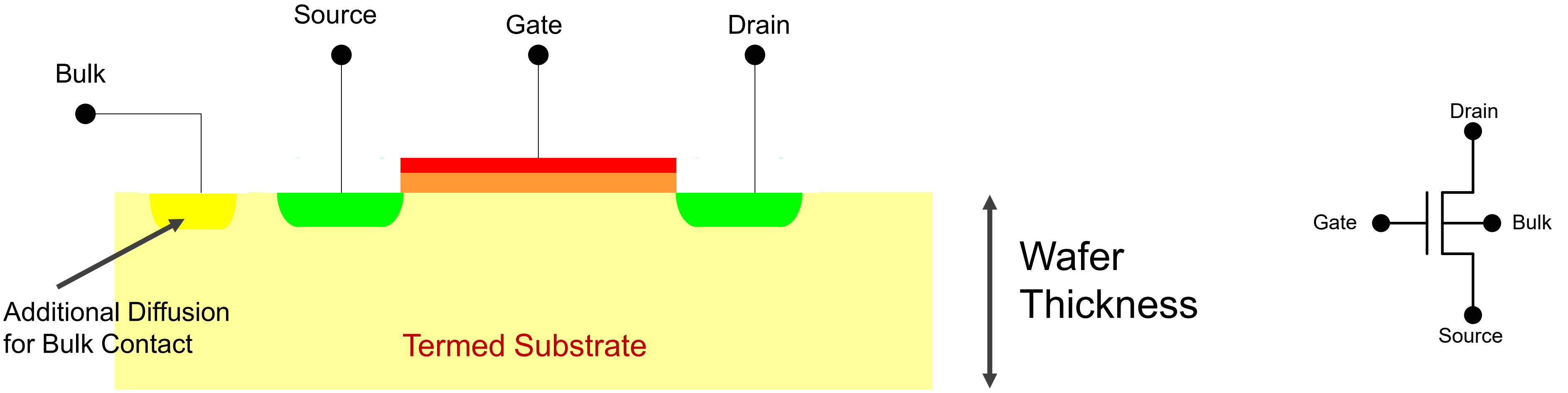
n-channel MOSFET



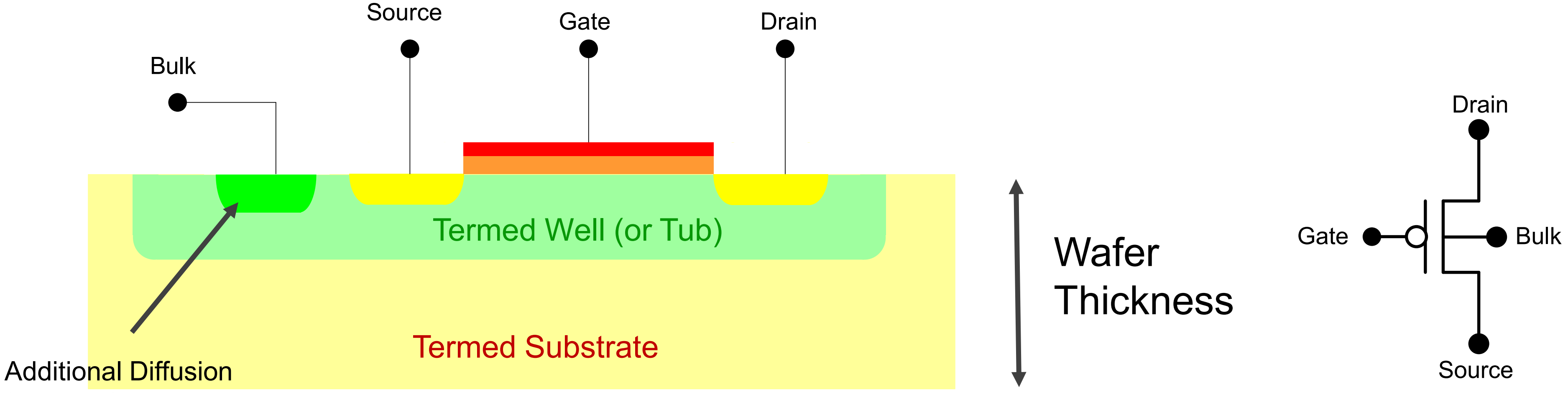
Metal Oxide Semiconductor → MOS

Early processes used metal for the gate, today metal is seldom used but the term MOS transistor is standard even though the gate is no longer metal

MOS Transistor in Bulk CMOS Process

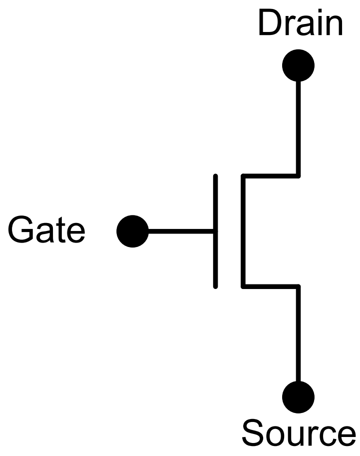


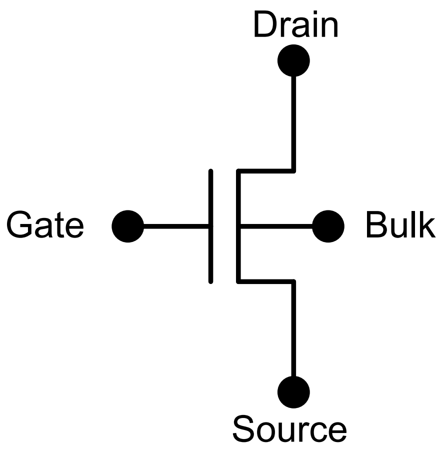
n-channel MOSFET



p-channel MOSFET

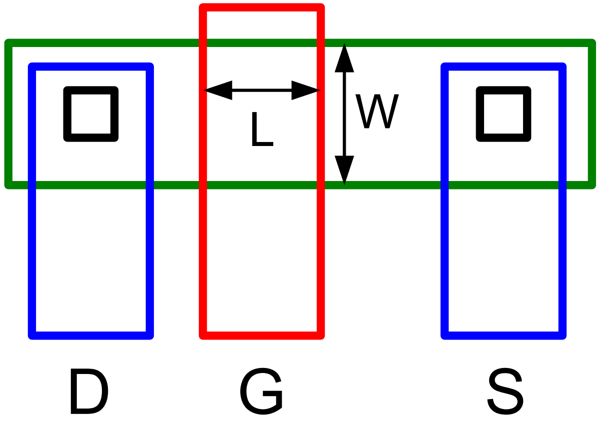
Design Rules and Layout – consider transistors

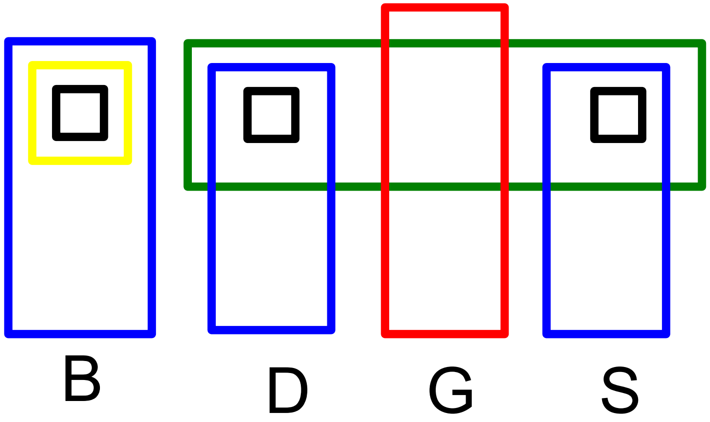




Layer Map

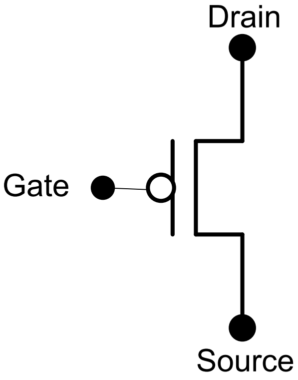
- 🟨 p-active
- 🟩 n-active
- 🟥 Poly 1
- 🟦 Metal 1
- 🟫 n-well
- ⬛ contact

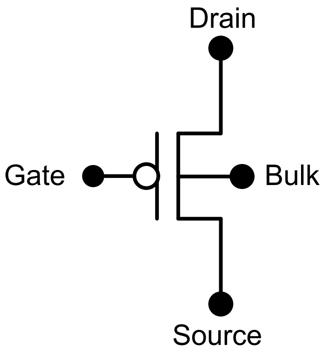




- Bulk connection needed
- Single bulk connection can often be used for several (many) transistors

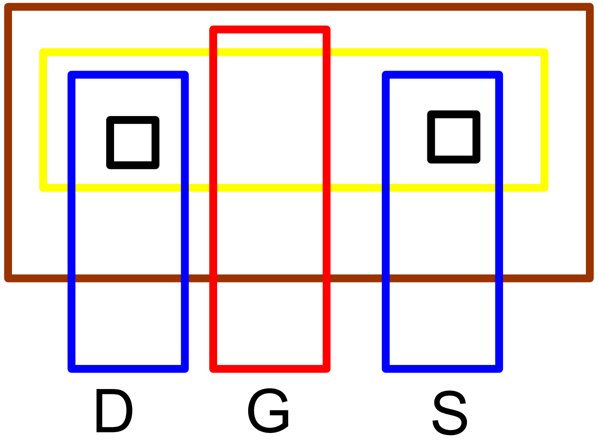
Design Rules and Layout – consider transistors

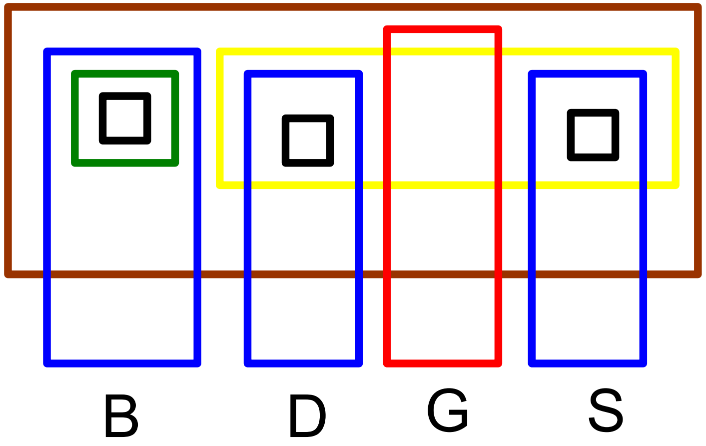




Layer Map

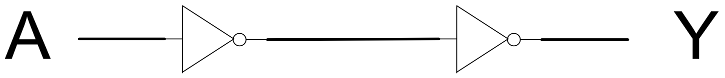
🟨 p-active
🟩 n-active
🟥 Poly 1
🟦 Metal 1
🟫 n-well
⬛ contact



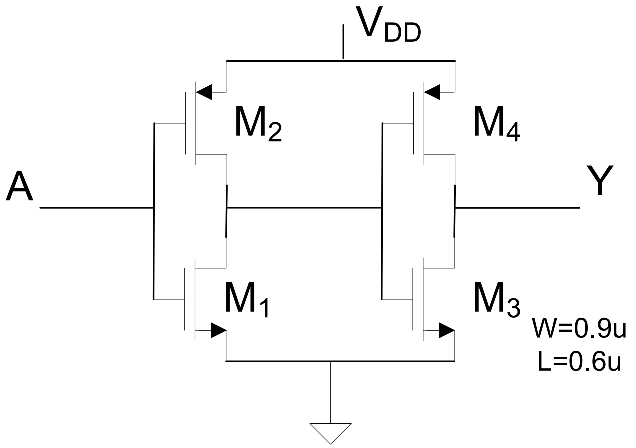


- Bulk connection needed
- Single bulk connection can often be used for several (many) transistors if they share the same well

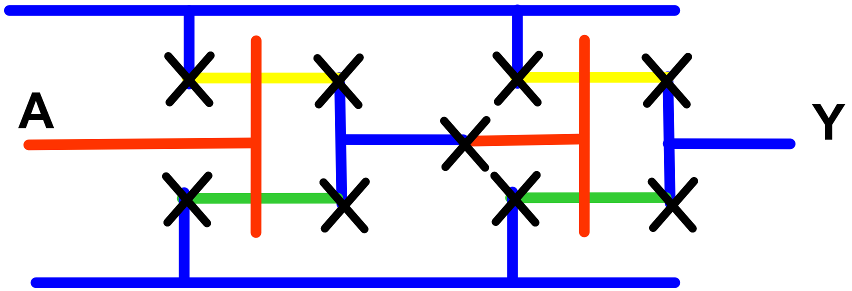
Design Rules and Layout (example)



Logic Circuit

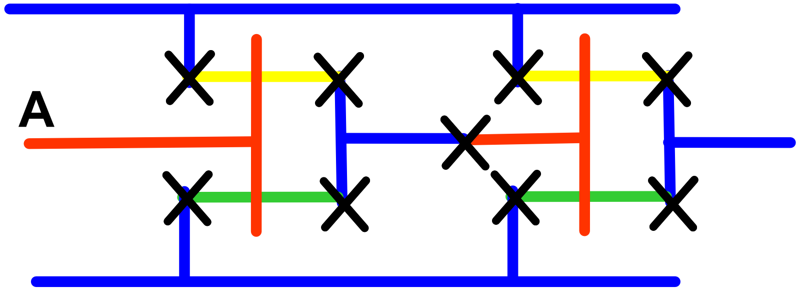


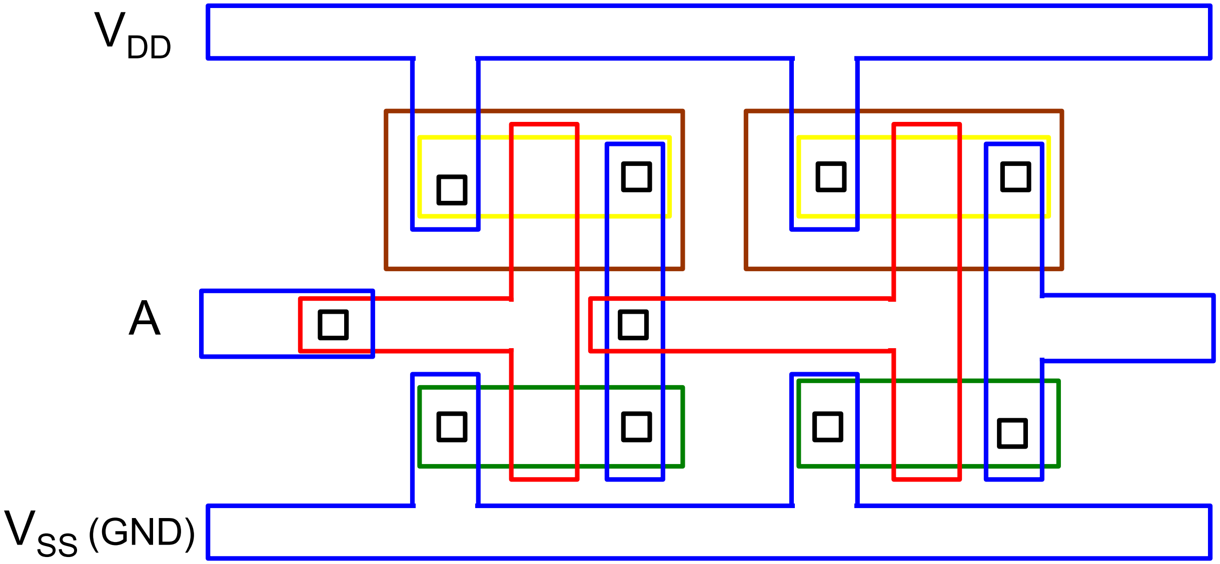
Circuit Schematic (Including Device Sizing)



Stick Diagram

Design Rules (example)



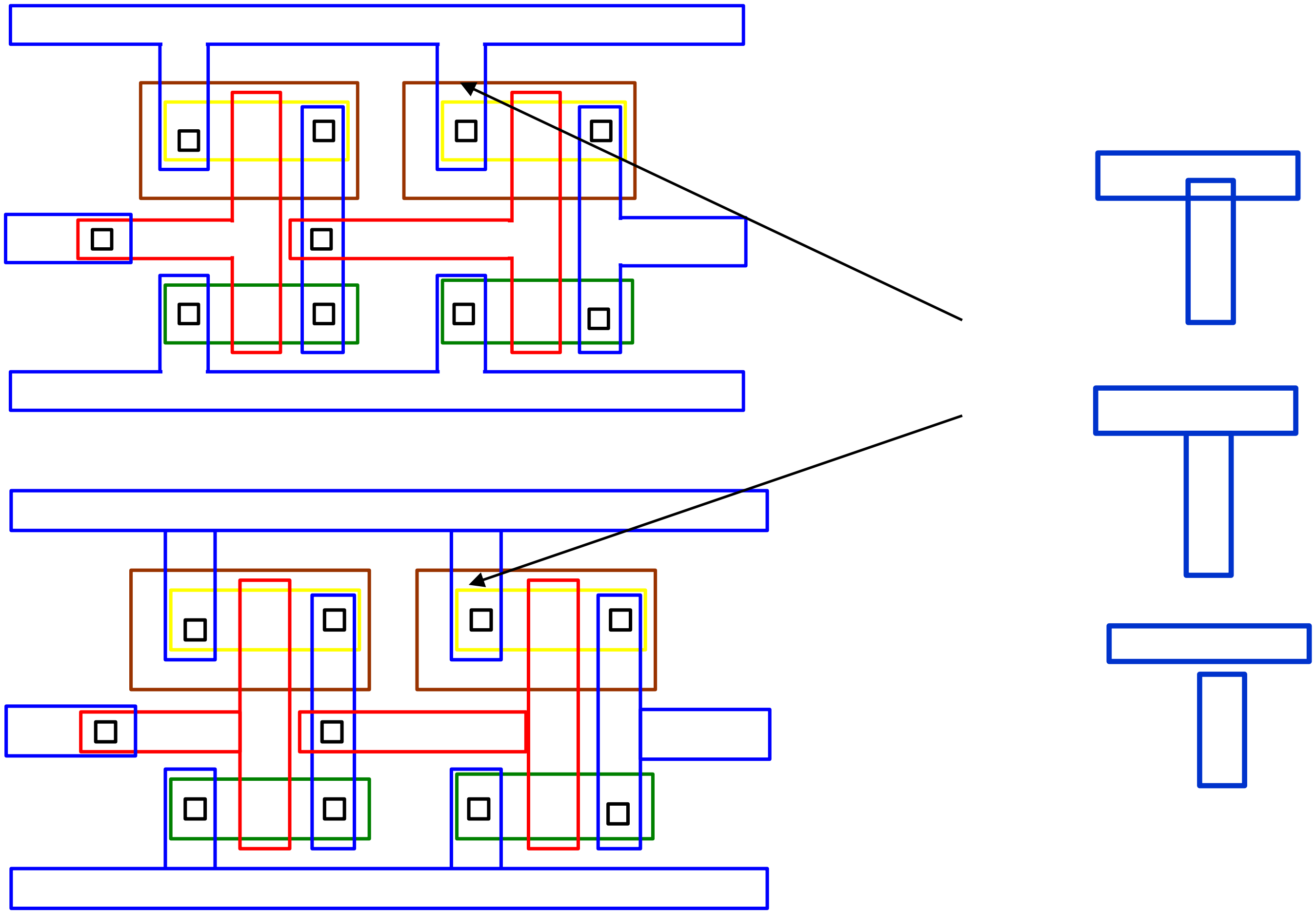


Layout

Layer Map

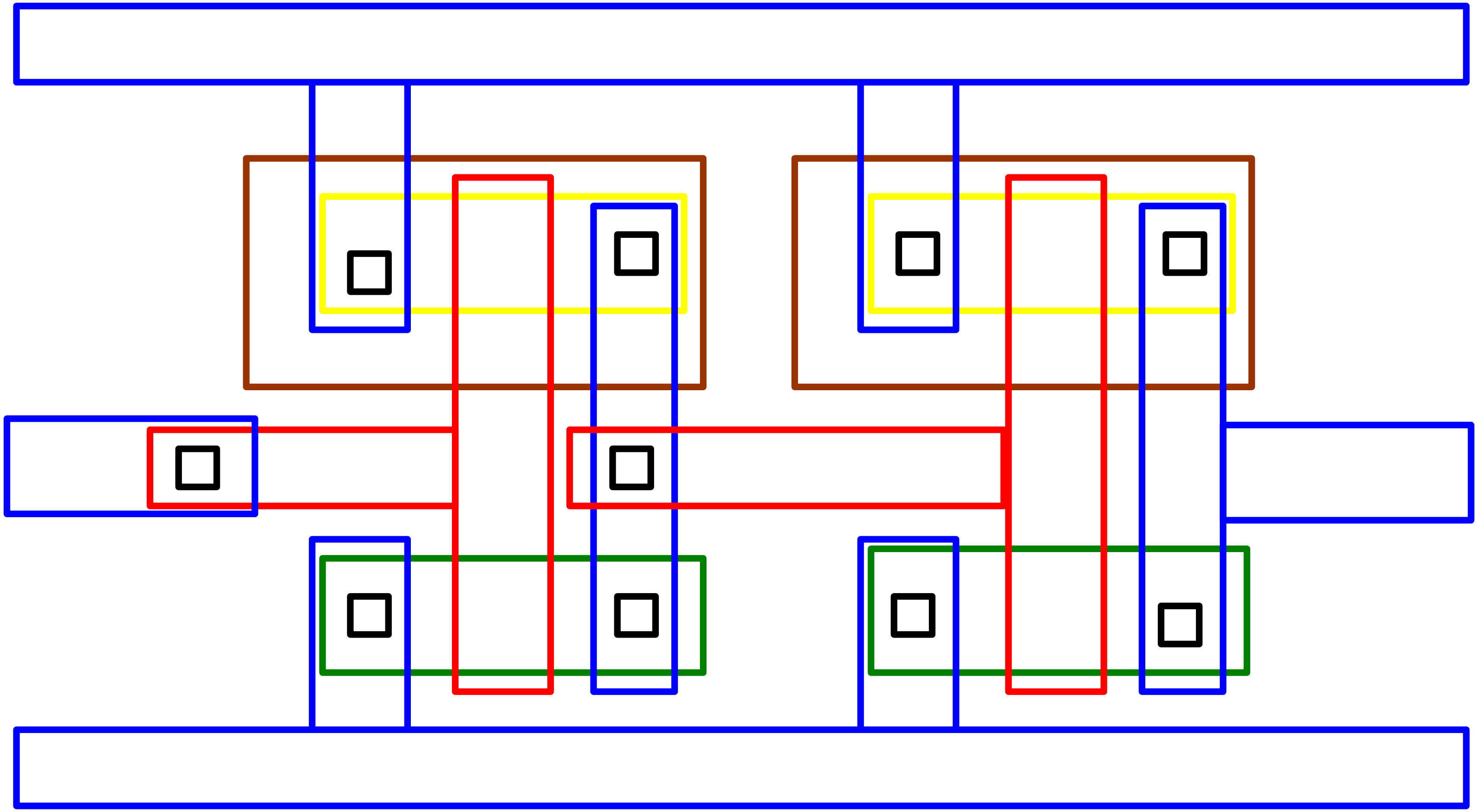
- 🟨 p-active
- 🟩 n-active
- 🟥 Poly 1
- 🟦 Metal 1
- 🟫 n-well
- ⬛ contact

Design Rules (example)



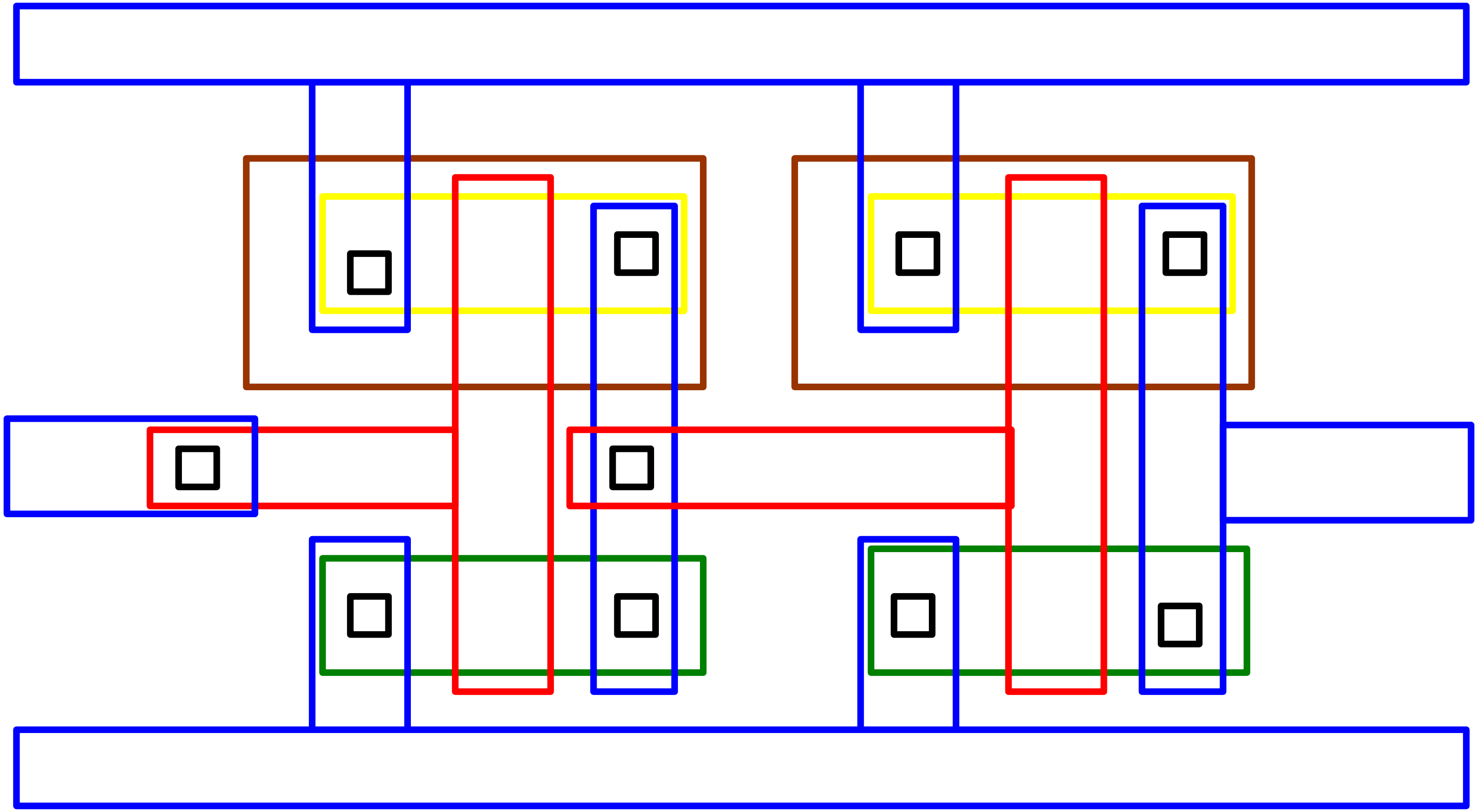
- Polygons in Geometric Description File (GDF) merged (when driving the pattern generator that makes the masks)
- Separate rectangles generally more convenient to represent
- Good practice to overlap rectangles to avoid break (though such an error would likely be caught with DRC)

Design Rules (example)



- Design rules must be satisfied throughout the design
- DRC runs incrementally during layout in most existing tools to flag most problems
- DRC can catch layout design rule errors but not circuit connection errors

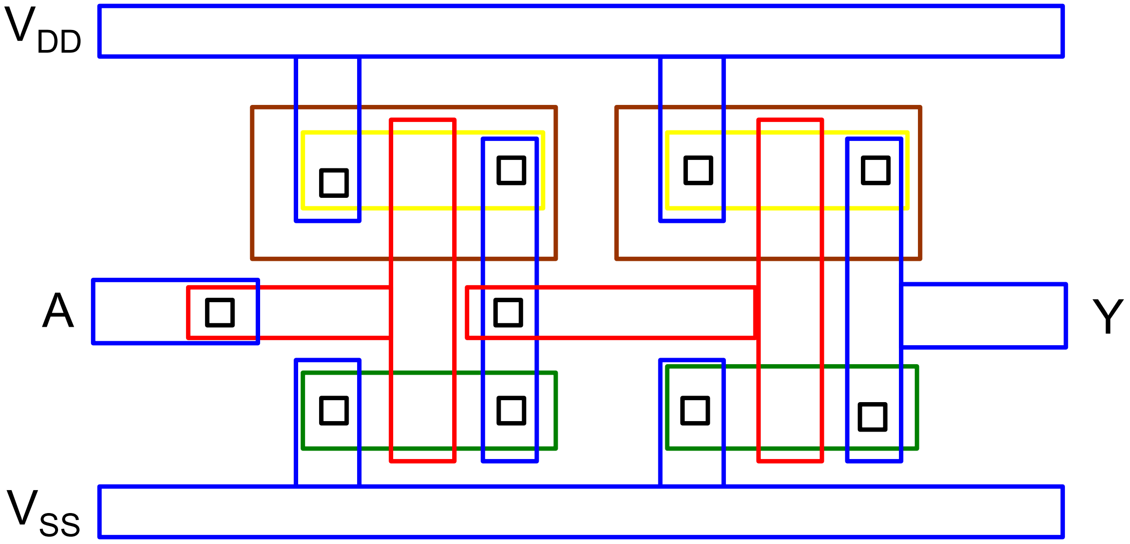
Design Rules (example)

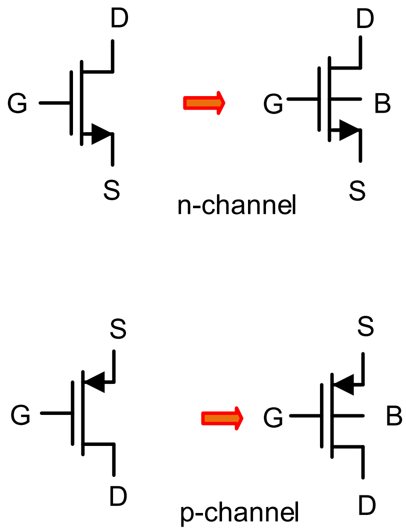


What is wrong with this layout ?

Bulk connections missing!

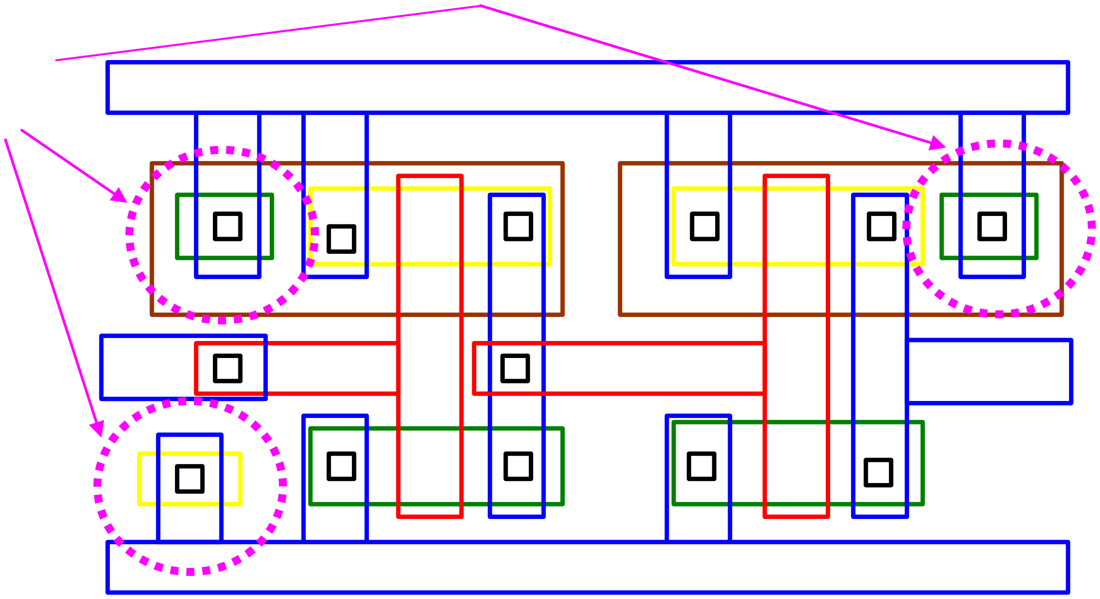
Design Rules (example)



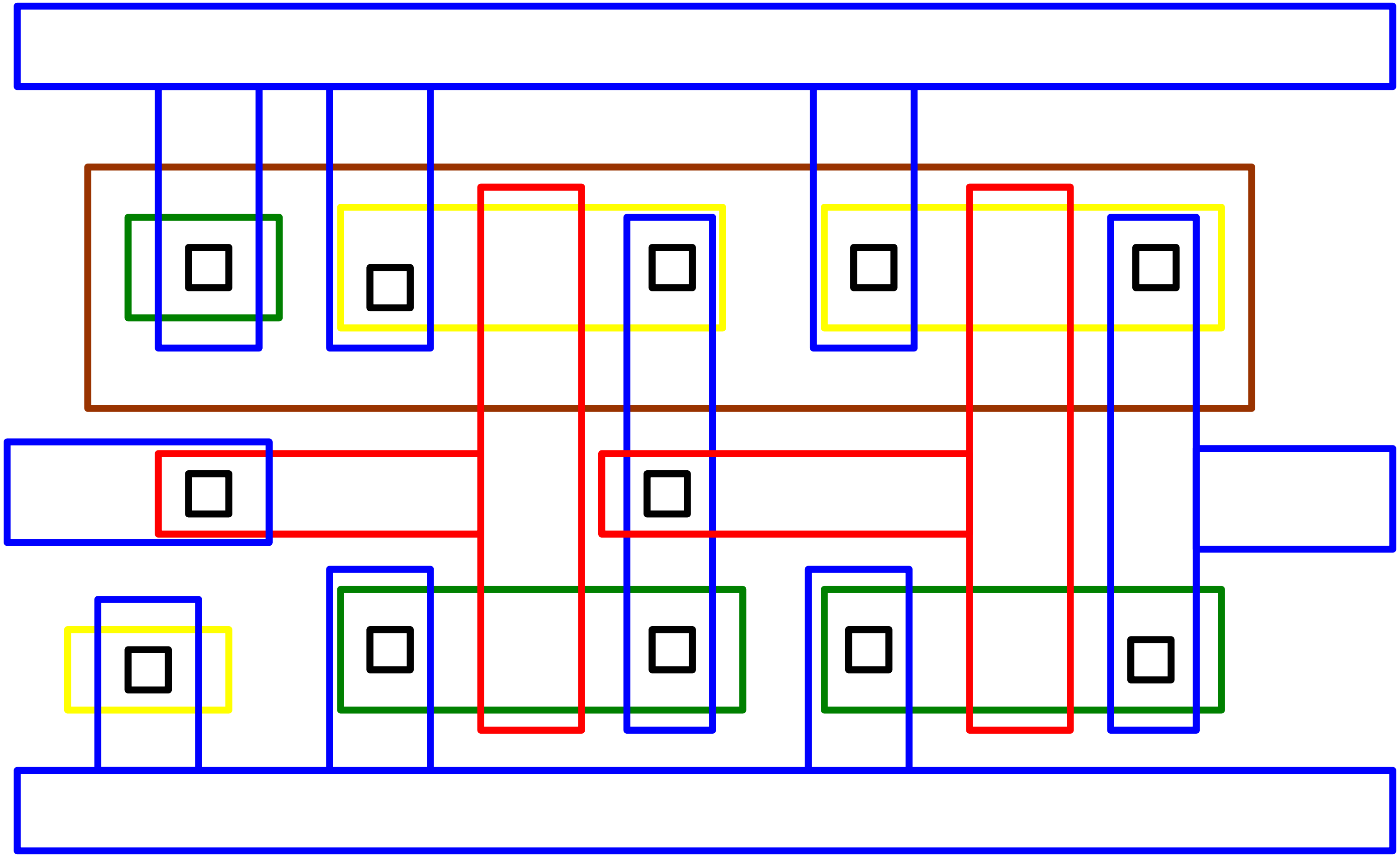


Actually 4-terminal device

- Note diffusions needed for bulk connections
- Note n-well connections increase area a significant amount
- Note n-wells are both connected to V_{DD} in this circuit

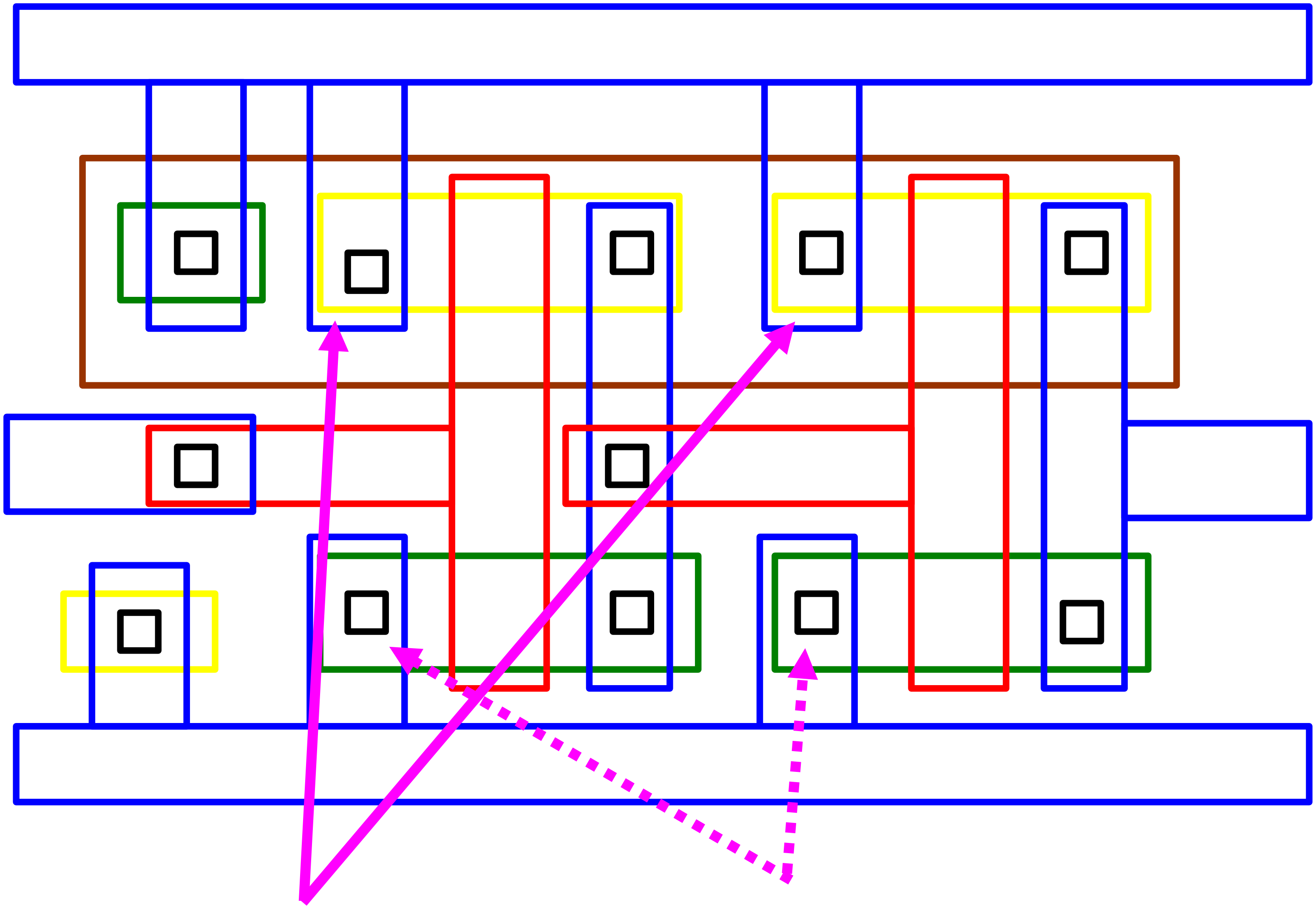


Design Rules (example)



Layout with shared p-well reduces area

Design Rules (example)



Shared p-active can be combined to reduce area

Shared n-active can be combined to reduce area

Design Rules

- Design rules can be given in absolute dimensions for every rule
- Design rules can be parameterized and given relative to a parameter
  - Makes movement from one process to another more convenient
  - Easier for designer to remember
  - Some penalty in area efficiency
  - Often termed λ-based design rules
  - Typically λ is ½ the minimum feature size in a process

Design Rules

- See www.MOSIS.com for design rules
- Some of these files are on class WEB site
  - SCMOS Rules Updated Sept 2005.pdf
  - Mosis Rules Pictorial.pdf

Under New Management, ***MOSIS welcomes New Director.***

MOSIS is pleased to announce a collaboration with the ***Intel Custom Foundry****. MOSIS is committed to providing foundry access to key technologies for our customers. The primary Foundries which The MOSIS Service supports are TSMC, GlobalFoundries, Intel and On Semi. Please see the Intel collaboration* ***press release****.*

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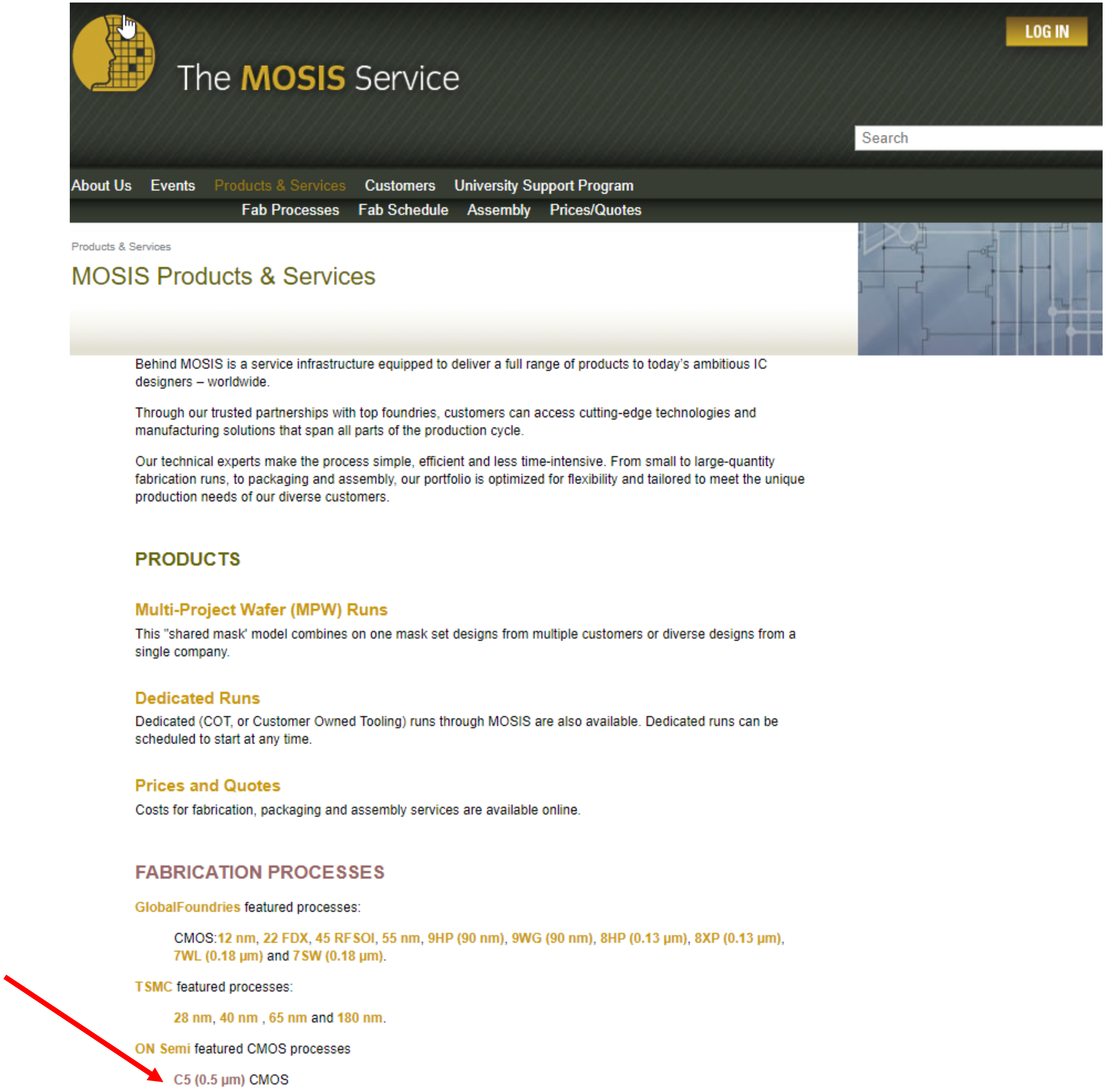
Updated Sept 13 2019



MOSIS Products & Services

Behind MOSIS is a service infrastructure equipped to deliver a full range of products to today's ambitious IC designers – worldwide.

Through our trusted partnerships with top foundries, customers can access cutting-edge technologies and manufacturing solutions that span all parts of the production cycle.

Our technical experts make the process simple, efficient and less time-intensive. From small to large-quantity fabrication runs, to packaging and assembly, our portfolio is optimized for flexibility and tailored to meet the unique production needs of our diverse customers.

PRODUCTS

Multi-Project Wafer (MPW) Runs

This "shared mask' model combines on one mask set designs from multiple customers or diverse designs from a single company.

Dedicated Runs

Dedicated (COT, or Customer Owned Tooling) runs through MOSIS are also available. Dedicated runs can be scheduled to start at any time.

Prices and Quotes

Costs for fabrication, packaging and assembly services are available online.

FABRICATION PROCESSES

GlobalFoundries featured processes:

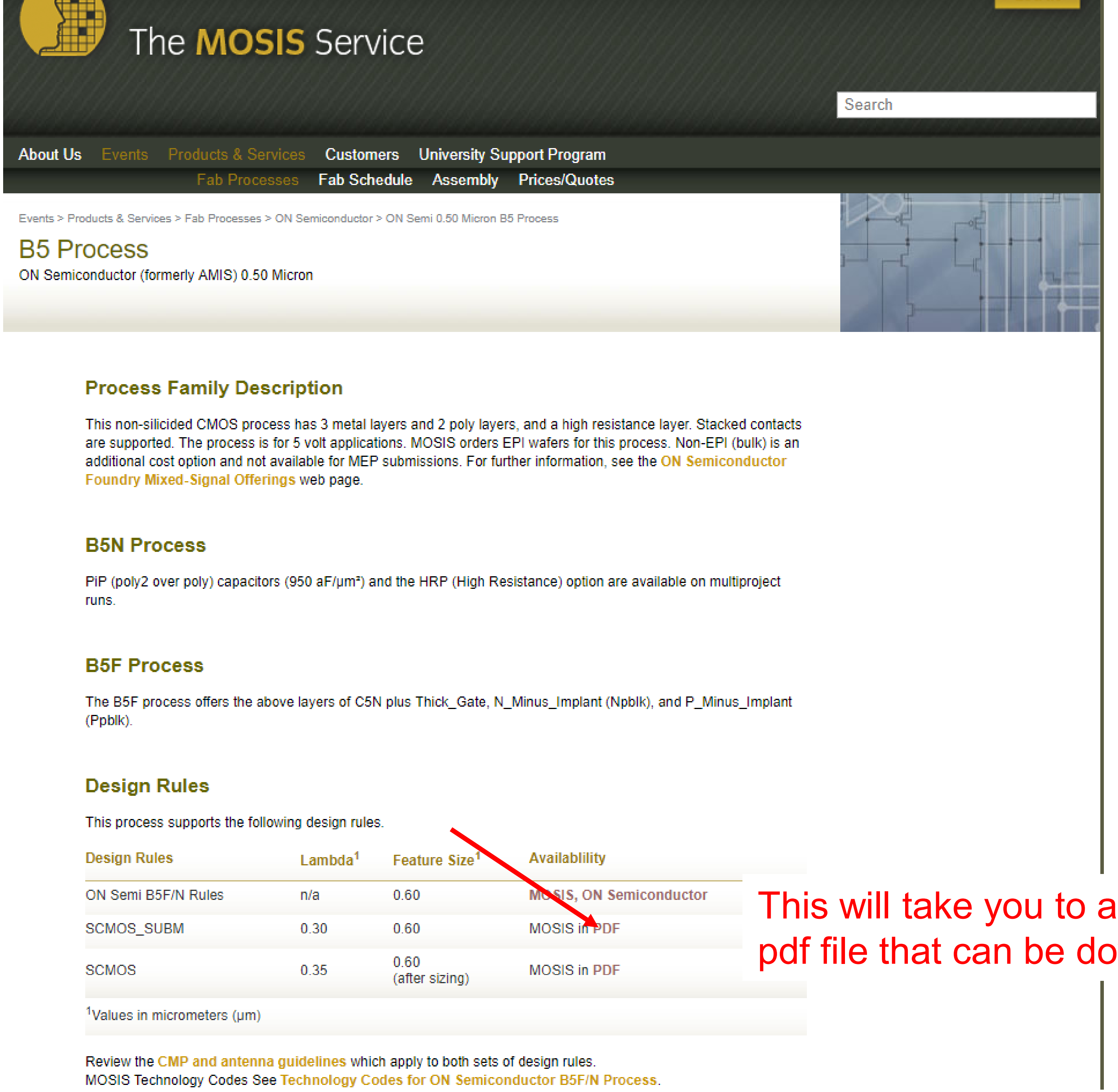
CMOS:12 nm, 22 FDX, 45 RFSOI, 55 nm, 9HP (90 nm), 9WG (90 nm), 8HP (0.13 µm), 8XP (0.13 µm), 7WL (0.18 µm) and 7SW (0.18 µm).

TSMC featured processes:

28 nm, 40 nm , 65 nm and 180 nm.

ON Semi featured CMOS processes

C5 (0.5 µm) CMOS



Events > Products & Services > Fab Processes > ON Semiconductor > ON Semi 0.50 Micron B5 Process

B5 Process

ON Semiconductor (formerly AMIS) 0.50 Micron

Process Family Description

This non-silicided CMOS process has 3 metal layers and 2 poly layers, and a high resistance layer. Stacked contacts are supported. The process is for 5 volt applications. MOSIS orders EPI wafers for this process. Non-EPI (bulk) is an additional cost option and not available for MEP submissions. For further information, see the ON Semiconductor Foundry Mixed-Signal Offerings web page.

B5N Process

PiP (poly2 over poly) capacitors (950 aF/µm²) and the HRP (High Resistance) option are available on multiproject runs.

B5F Process

The B5F process offers the above layers of C5N plus Thick_Gate, N_Minus_Implant (Npblk), and P_Minus_Implant (Ppblk).

Design Rules

This process supports the following design rules.

Design Rules	Lambda[1]	Feature Size[1]	Availablility
ON Semi B5F/N Rules	n/a	0.60	MOSIS, ON Semiconductor
SCMOS_SUBM	0.30	0.60	MOSIS in PDF
SCMOS	0.35	0.60 (after sizing)	MOSIS in PDF

[1] Values in micrometers (µm)

Review the CMP and antenna guidelines which apply to both sets of design rules.
MOSIS Technology Codes See Technology Codes for ON Semiconductor B5F/N Process.

This will take you to a 54 page pdf file that can be downloaded

Examples in slides

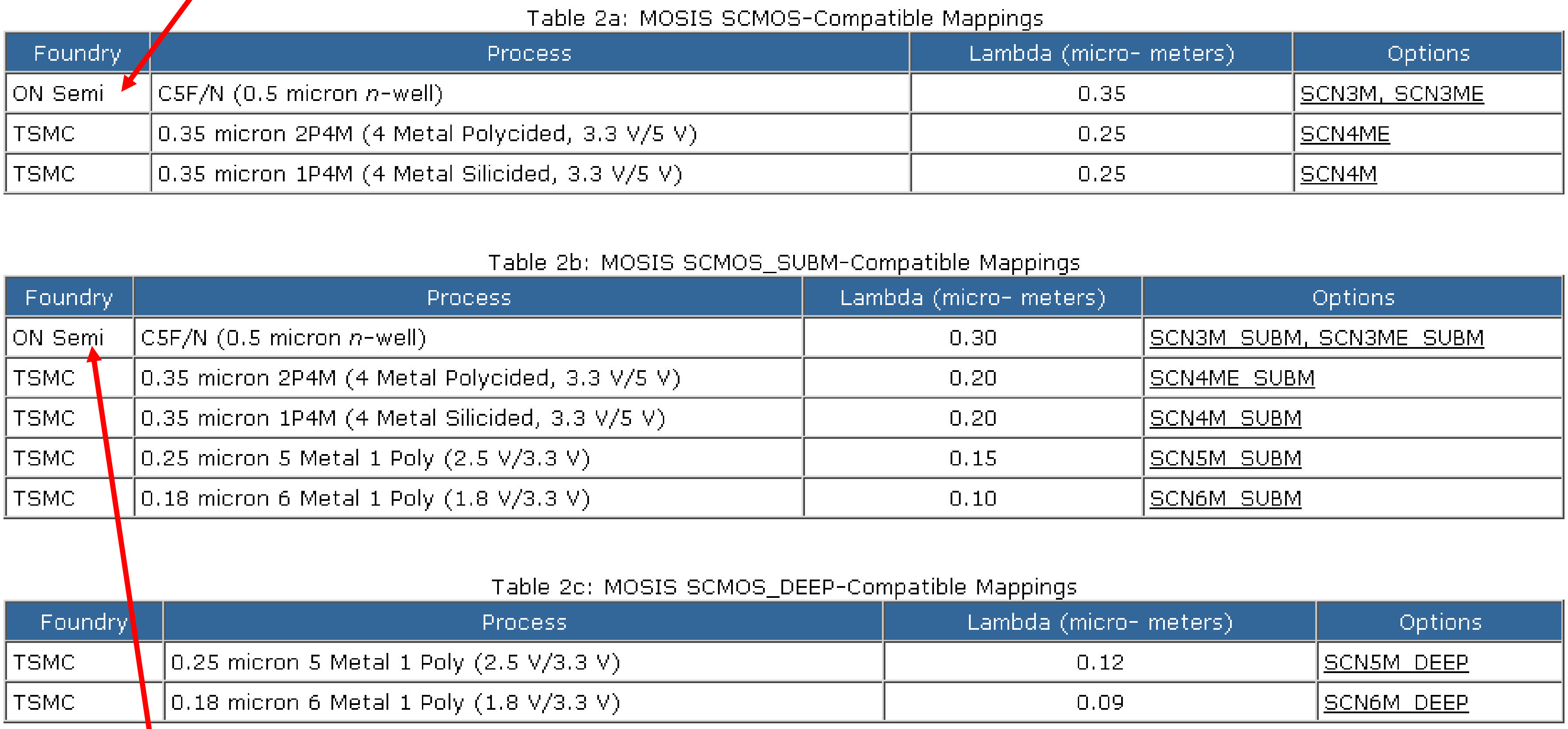


Table 2a: MOSIS SCMOS-Compatible Mappings

Foundry	Process	Lambda (micro- meters)	Options
ON Semi	C5F/N (0.5 micron *n*-well)	0.35	SCN3M, SCN3ME
TSMC	0.35 micron 2P4M (4 Metal Polycided, 3.3 V/5 V)	0.25	SCN4ME
TSMC	0.35 micron 1P4M (4 Metal Silicided, 3.3 V/5 V)	0.25	SCN4M

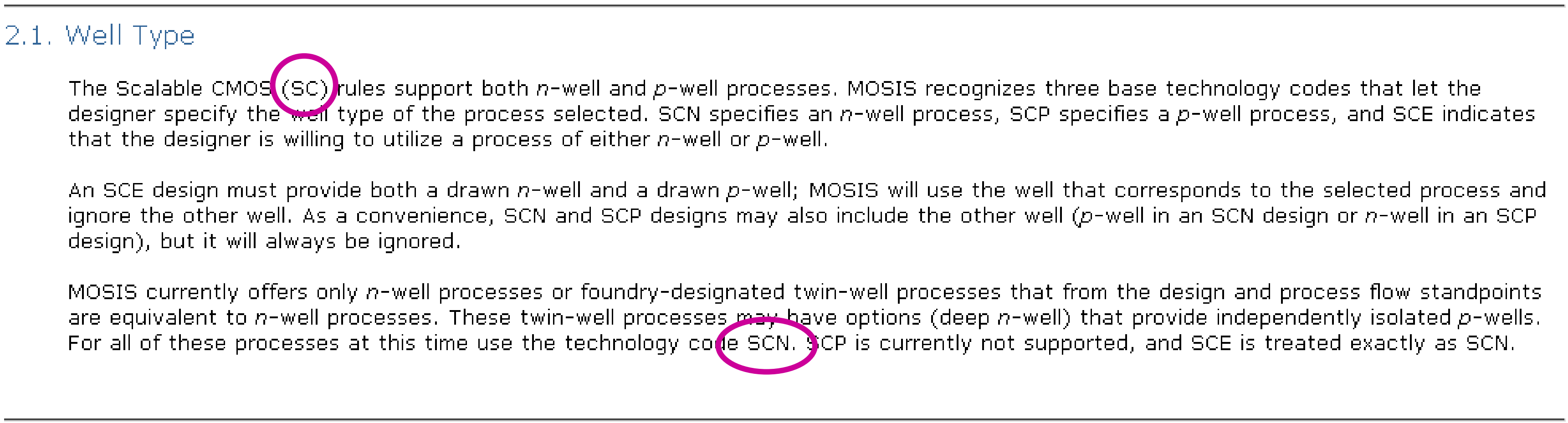
Table 2b: MOSIS SCMOS_SUBM-Compatible Mappings

Foundry	Process	Lambda (micro- meters)	Options
ON Semi	C5F/N (0.5 micron *n*-well)	0.30	SCN3M_SUBM, SCN3ME_SUBM
TSMC	0.35 micron 2P4M (4 Metal Polycided, 3.3 V/5 V)	0.20	SCN4ME_SUBM
TSMC	0.35 micron 1P4M (4 Metal Silicided, 3.3 V/5 V)	0.20	SCN4M_SUBM
TSMC	0.25 micron 5 Metal 1 Poly (2.5 V/3.3 V)	0.15	SCN5M_SUBM
TSMC	0.18 micron 6 Metal 1 Poly (1.8 V/3.3 V)	0.10	SCN6M_SUBM

Table 2c: MOSIS SCMOS_DEEP-Compatible Mappings

Foundry	Process	Lambda (micro- meters)	Options
TSMC	0.25 micron 5 Metal 1 Poly (2.5 V/3.3 V)	0.12	SCN5M_DEEP
TSMC	0.18 micron 6 Metal 1 Poly (1.8 V/3.3 V)	0.09	SCN6M_DEEP

Our labs and class projects

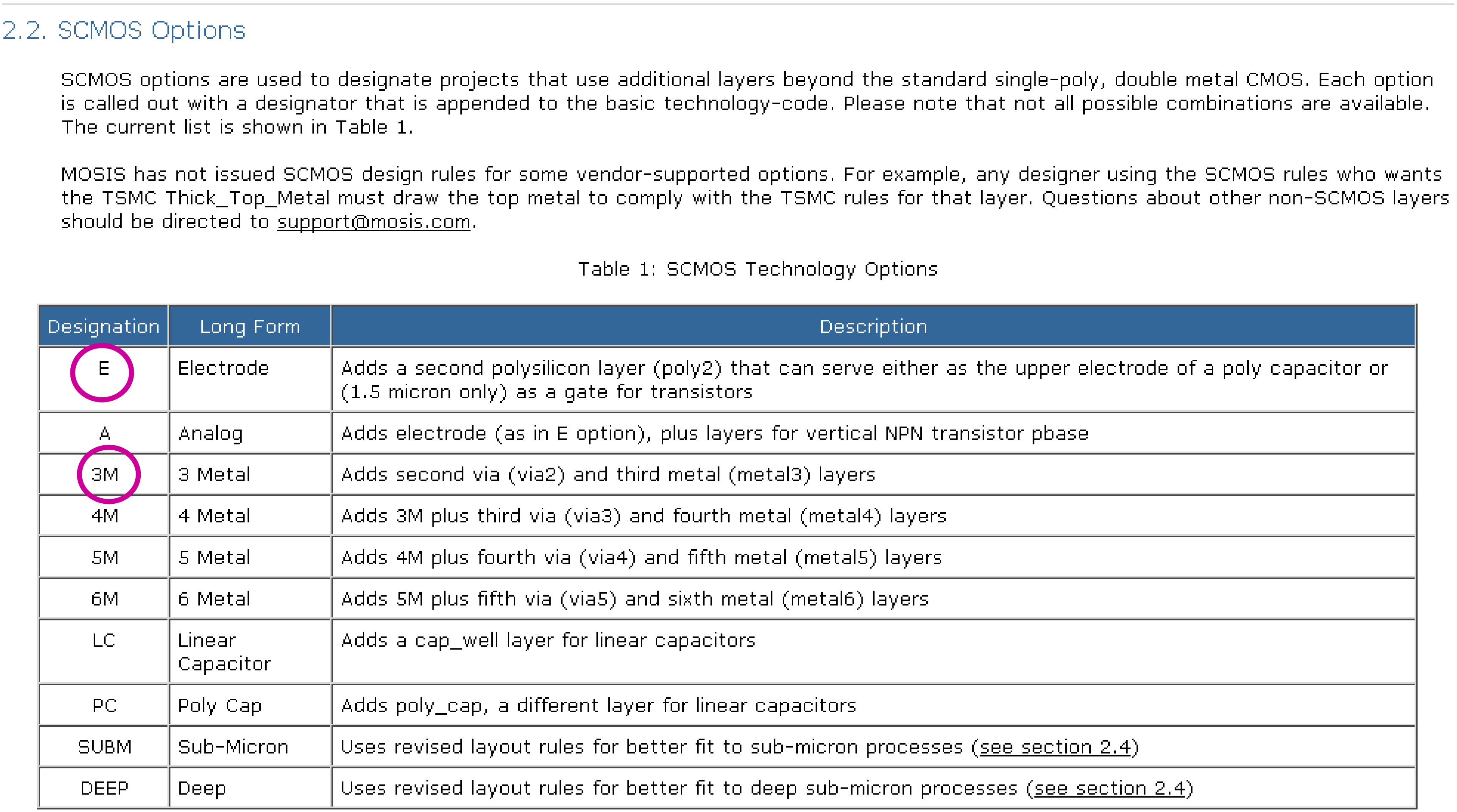


2.1. Well Type

The Scalable CMOS (SC) rules support both *n*-well and *p*-well processes. MOSIS recognizes three base technology codes that let the designer specify the well type of the process selected. SCN specifies an *n*-well process, SCP specifies a *p*-well process, and SCE indicates that the designer is willing to utilize a process of either *n*-well or *p*-well.

An SCE design must provide both a drawn *n*-well and a drawn *p*-well; MOSIS will use the well that corresponds to the selected process and ignore the other well. As a convenience, SCN and SCP designs may also include the other well (*p*-well in an SCN design or *n*-well in an SCP design), but it will always be ignored.

MOSIS currently offers only *n*-well processes or foundry-designated twin-well processes that from the design and process flow standpoints are equivalent to *n*-well processes. These twin-well processes may have options (deep *n*-well) that provide independently isolated *p*-wells. For all of these processes at this time use the technology code SCN. SCP is currently not supported, and SCE is treated exactly as SCN.



2.2. SCMOS Options

SCMOS options are used to designate projects that use additional layers beyond the standard single-poly, double metal CMOS. Each option is called out with a designator that is appended to the basic technology-code. Please note that not all possible combinations are available. The current list is shown in Table 1.

MOSIS has not issued SCMOS design rules for some vendor-supported options. For example, any designer using the SCMOS rules who wants the TSMC Thick_Top_Metal must draw the top metal to comply with the TSMC rules for that layer. Questions about other non-SCMOS layers should be directed to support@mosis.com.

Table 1: SCMOS Technology Options

Designation	Long Form	Description
[✓ E]	Electrode	Adds a second polysilicon layer (poly2) that can serve either as the upper electrode of a poly capacitor or (1.5 micron only) as a gate for transistors
A	Analog	Adds electrode (as in E option), plus layers for vertical NPN transistor pbase
[✓ 3M]	3 Metal	Adds second via (via2) and third metal (metal3) layers
4M	4 Metal	Adds 3M plus third via (via3) and fourth metal (metal4) layers
5M	5 Metal	Adds 4M plus fourth via (via4) and fifth metal (metal5) layers
6M	6 Metal	Adds 5M plus fifth via (via5) and sixth metal (metal6) layers
LC	Linear Capacitor	Adds a cap_well layer for linear capacitors
PC	Poly Cap	Adds poly_cap, a different layer for linear capacitors
SUBM	Sub-Micron	Uses revised layout rules for better fit to sub-micron processes (see section 2.4)
DEEP	Deep	Uses revised layout rules for better fit to deep sub-micron processes (see section 2.4)

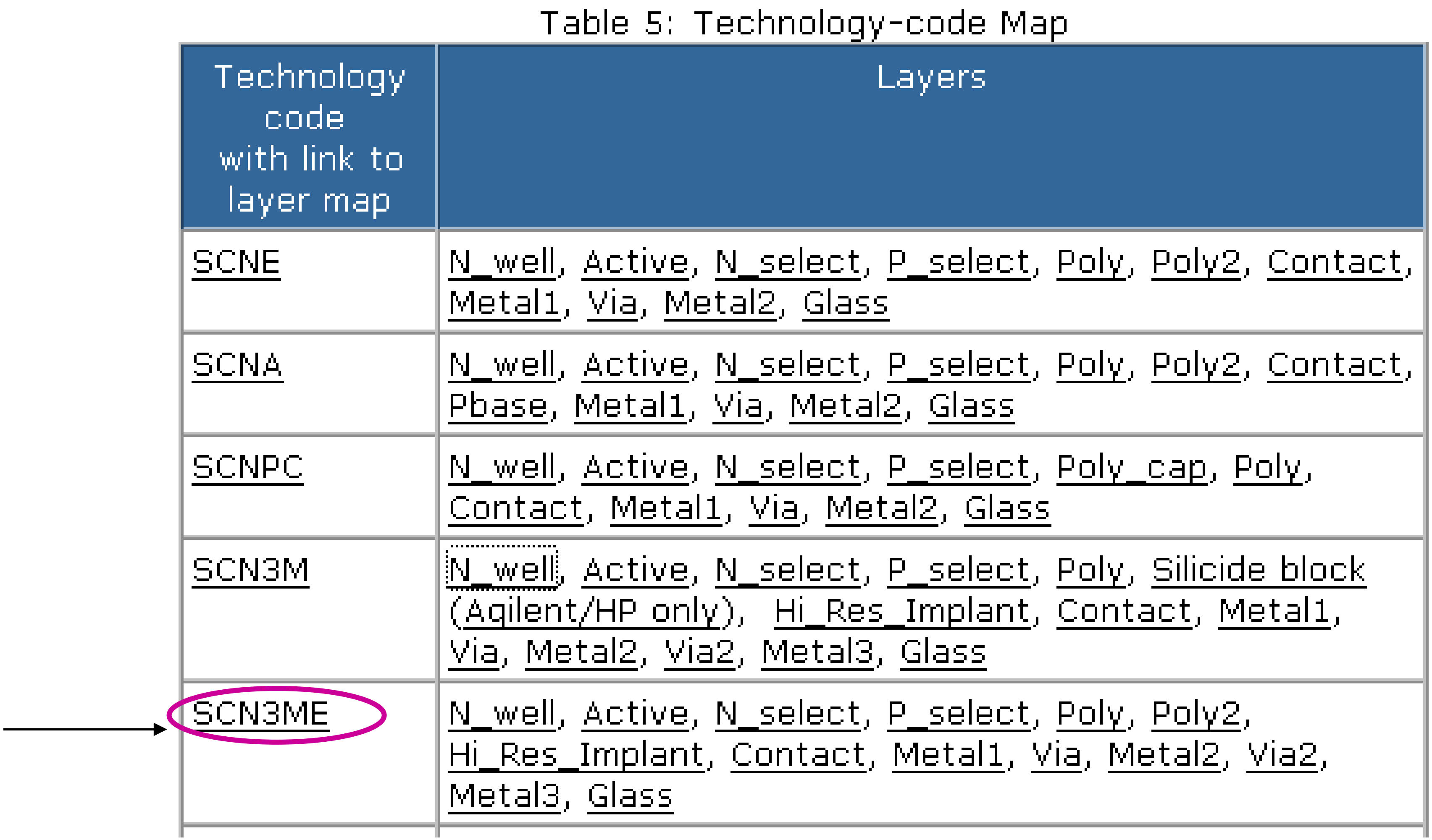
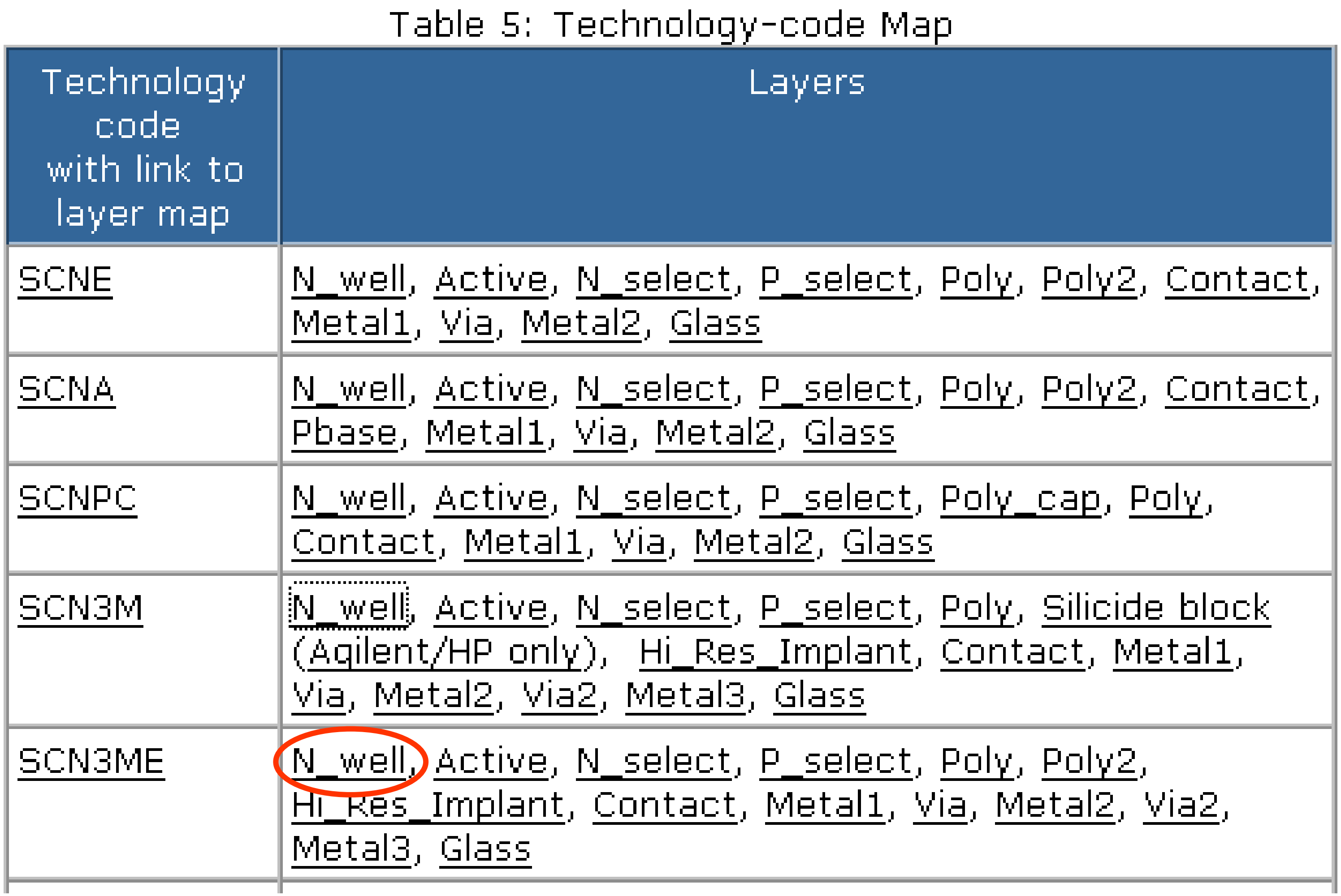


Table 5: Technology-code Map

Technology code with link to layer map	Layers
SCNE	N_well, Active, N_select, P_select, Poly, Poly2, Contact, Metal1, Via, Metal2, Glass
SCNA	N_well, Active, N_select, P_select, Poly, Poly2, Contact, Pbase, Metal1, Via, Metal2, Glass
SCNPC	N_well, Active, N_select, P_select, Poly_cap, Poly, Contact, Metal1, Via, Metal2, Glass
SCN3M	N_well, Active, N_select, P_select, Poly, Silicide block (Agilent/HP only), Hi_Res_Implant, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass
SCN3ME	N_well, Active, N_select, P_select, Poly, Poly2, Hi_Res_Implant, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass



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SCNPC	N_well, Active, N_select, P_select, Poly_cap, Poly, Contact, Metal1, Via, Metal2, Glass
SCN3M	N_well, Active, N_select, P_select, Poly, Silicide block (Agilent/HP only), Hi_Res_Implant, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass
SCN3ME	N_well, Active, N_select, P_select, Poly, Poly2, Hi_Res_Implant, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass

SCMOS Layout Rules - Well

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
1.1	Minimum width	10	12	12
1.2	Minimum spacing between wells at different potential	9 [1]	18 [2]	18
1.3	Minimum spacing between wells at same potential	6 [3]	6 [4]	6
1.4	Minimum spacing between wells of different type (if both are drawn)	0	0	0

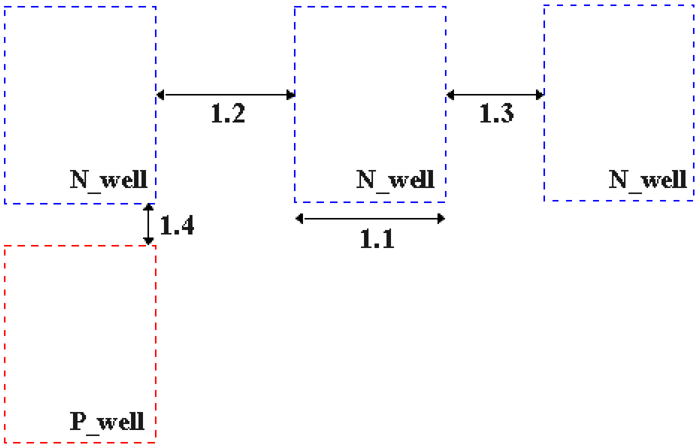
Exceptions for AMIS C30 0.35 micron process:

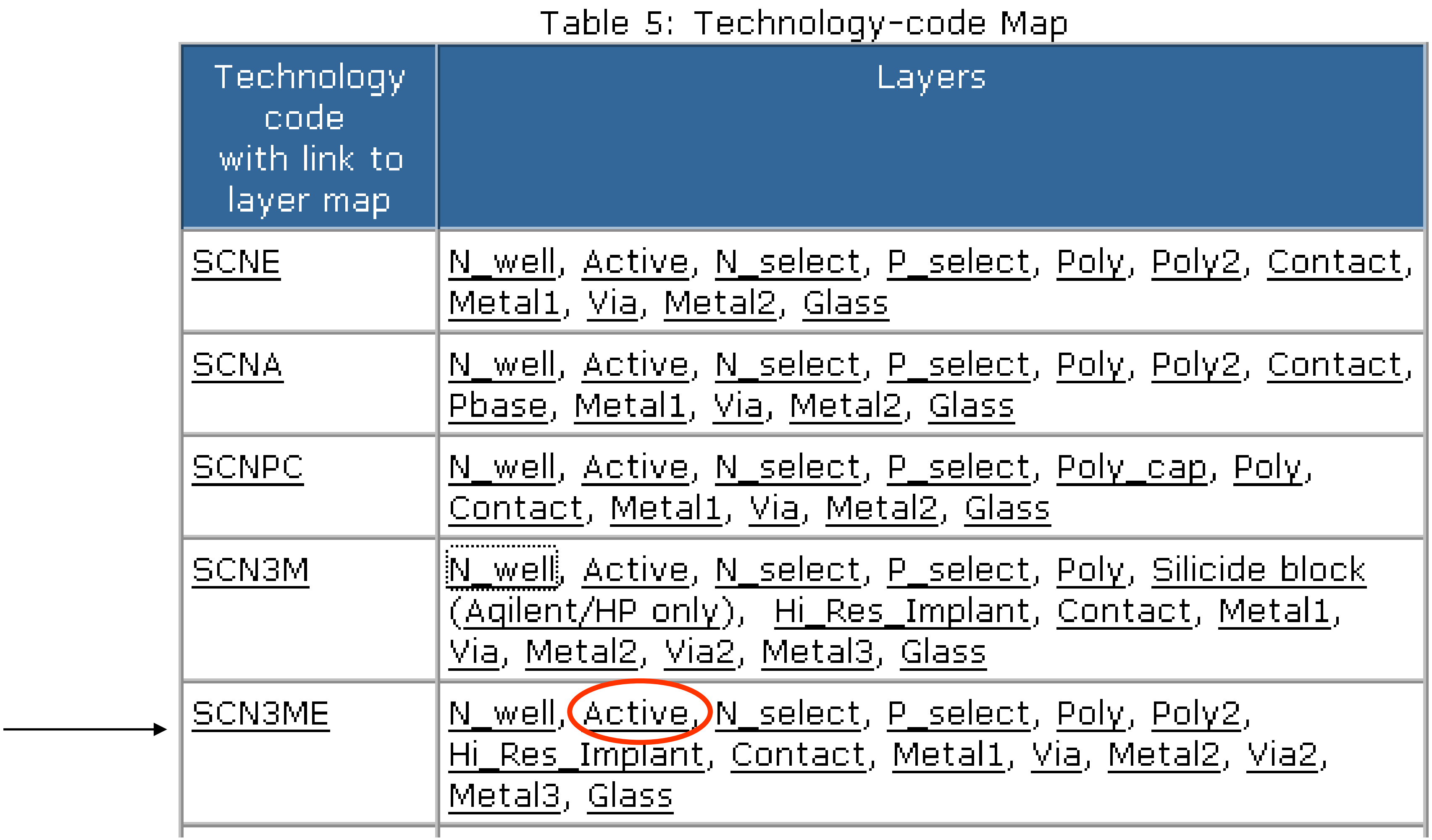
[1] Use lambda=16 for rule 1.2 only when using SCN4M or SCN4ME

[2] Use lambda=21 for rule 1.2 only when using SCN4M_SUBM or SCN4ME_SUBM

[3] Use lambda=8 for rule 1.3 only when using SCN4M or SCN4ME

[4] Use lambda=11 for rule 1.3 only when using SCN4M_SUBM or SCN4ME_SUBM





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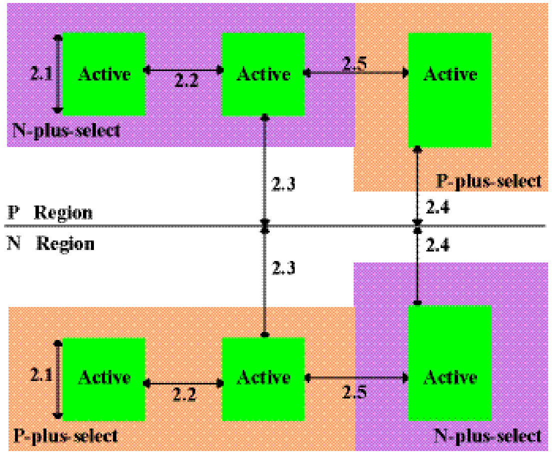
SCNA	N_well, Active, N_select, P_select, Poly, Poly2, Contact, Pbase, Metal1, Via, Metal2, Glass
SCNPC	N_well, Active, N_select, P_select, Poly_cap, Poly, Contact, Metal1, Via, Metal2, Glass
SCN3M	N_well, Active, N_select, P_select, Poly, Silicide block (Agilent/HP only), Hi_Res_Implant, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass
SCN3ME	N_well, Active, N_select, P_select, Poly, Poly2, Hi_Res_Implant, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass

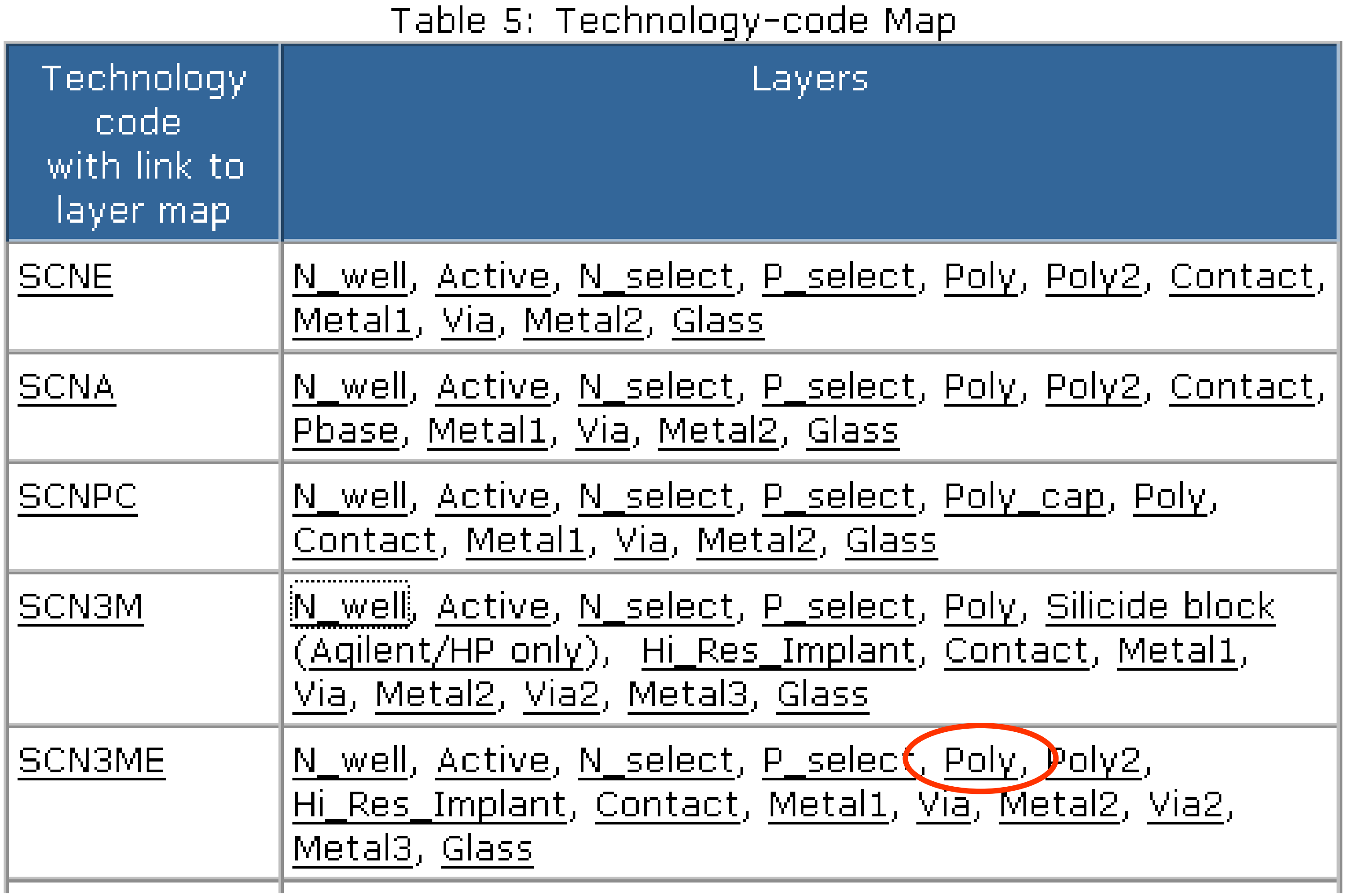
SCMOS Layout Rules - Active

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
2.1	Minimum width	3 *	3 *	3
2.2	Minimum spacing	3	3	3
2.3	Source/drain active to well edge	5	6	6
2.4	Substrate/well contact active to well edge	3	3	3
2.5	Minimum spacing between non-abutting active of different implant. Abutting active ("split-active") is illustrated under Select Layout Rules.	4	4	4

* Note: For analog and critical digital designs, MOSIS recommends the following minimum MOS channel widths (active under poly) for AMIS designs. Narrower devices, down to design rule minimum, will be functional, but their electrical characteristics will not scale, and their performance is not predictable from MOSIS SPICE parameters.

Process	Design Technology	Design Lambda (micrometers)	Minimum Width (lambda)
AMI_ABN	SCNA, SCNE	0.80	5
AMI_C5F/N	SCN3M, SCN3ME	0.35	9
AMI_C5F/N	SCN3M_SUBM, SCN3ME_SUBM	0.30	10





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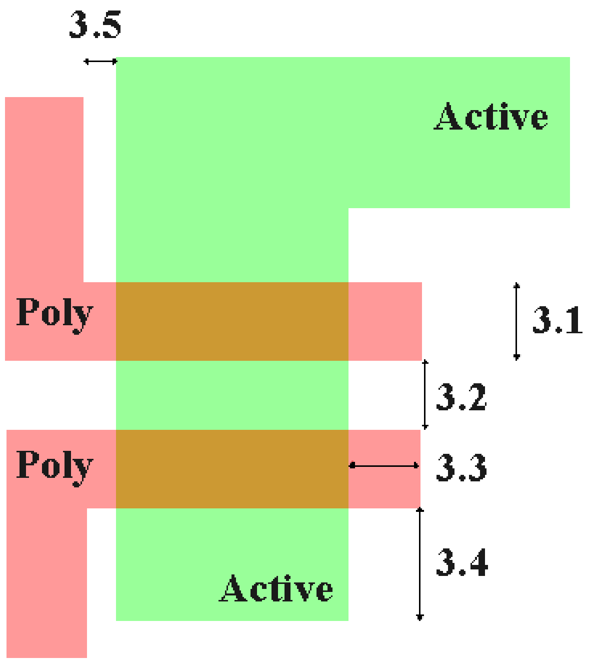
SCNPC	N_well, Active, N_select, P_select, Poly_cap, Poly, Contact, Metal1, Via, Metal2, Glass
SCN3M	N_well, Active, N_select, P_select, Poly, Silicide block (Agilent/HP only), Hi_Res_Implant, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass
SCN3ME	N_well, Active, N_select, P_select, Poly, Poly2, Hi_Res_Implant, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass

SCMOS Layout Rules - Poly

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
3.1	Minimum width	2	2	2
3.2	Minimum spacing over field	2	3	3
3.2.a	Minimum spacing over active	2	3	4
3.3	Minimum gate extension of active	2	2	2.5
3.4	Minimum active extension of poly	3	3	4
3.5	Minimum field poly to active	1	1	1



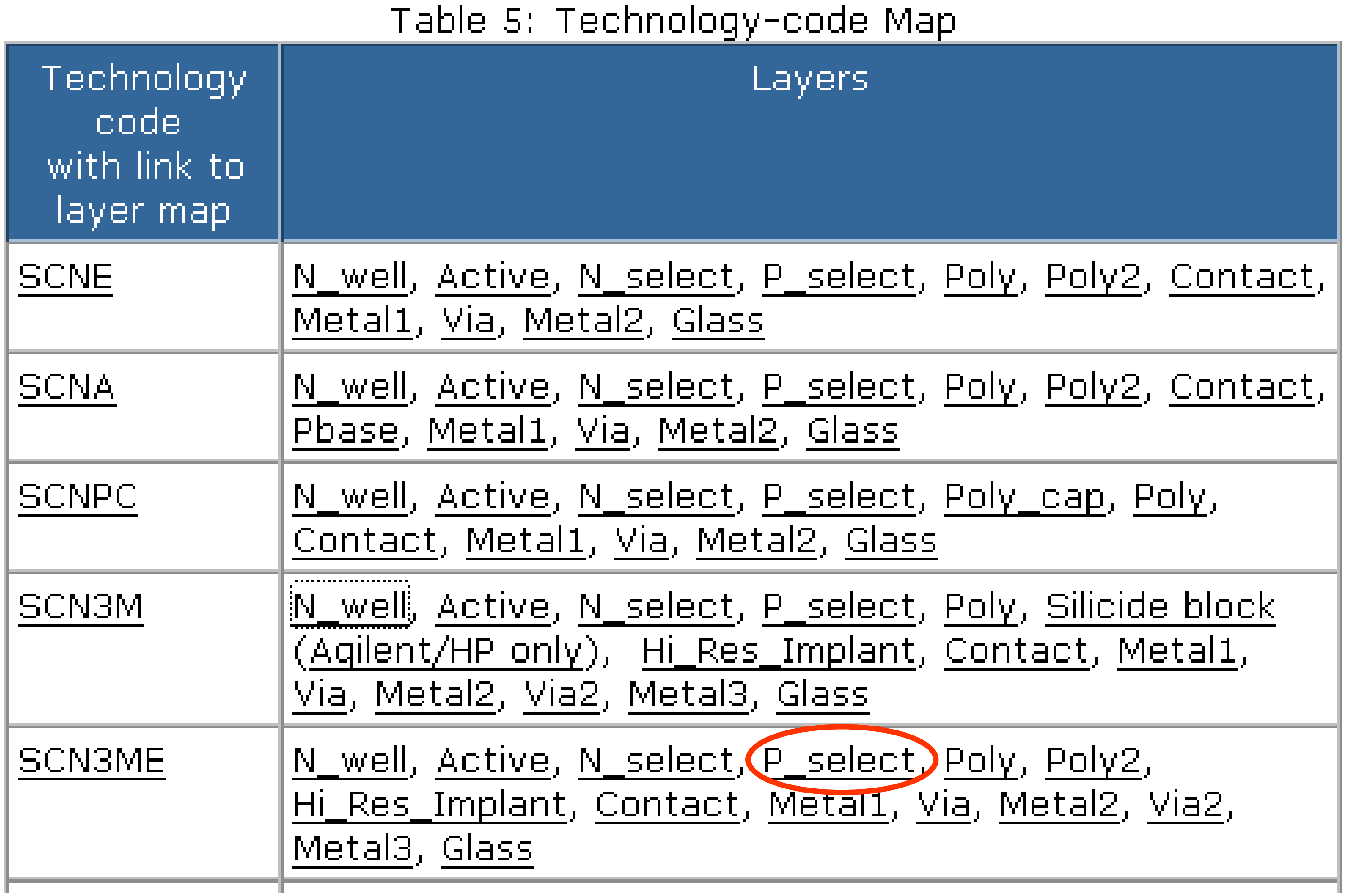


Table 5: Technology-code Map

Technology code with link to layer map	Layers
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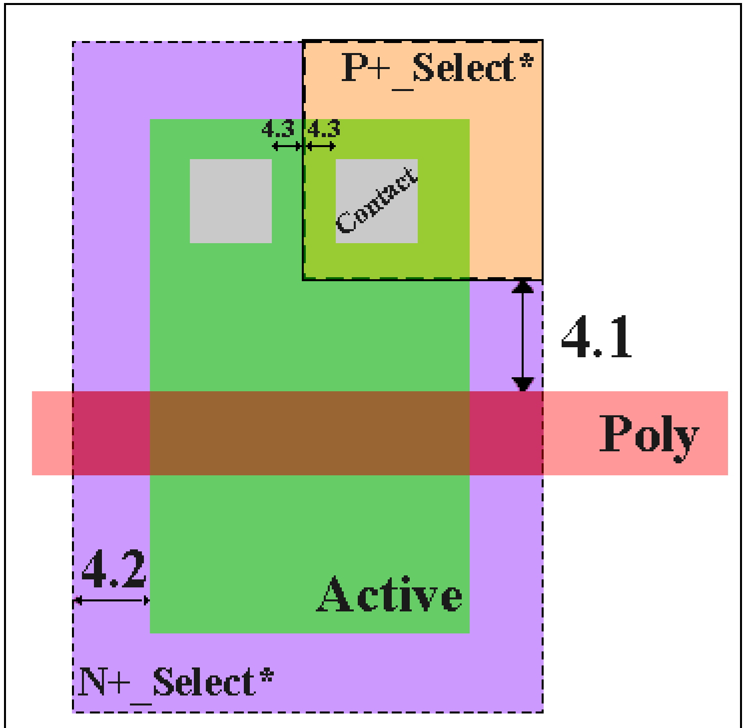
SCNPC	N_well, Active, N_select, P_select, Poly_cap, Poly, Contact, Metal1, Via, Metal2, Glass
SCN3M	N_well, Active, N_select, P_select, Poly, Silicide block (Agilent/HP only), Hi_Res_Implant, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass
SCN3ME	N_well, Active, N_select, P_select, Poly, Poly2, Hi_Res_Implant, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass

SCMOS Layout Rules - Select

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
4.1	Minimum select spacing to channel of transistor to ensure adequate source/drain width	3	3	3
4.2	Minimum select overlap of active	2	2	2
4.3	Minimum select overlap of contact	1	1	1.5
4.4	Minimum select width and spacing (Note: P-select and N-select may be coincident, but must *not* overlap) (not illustrated)	2	2	4



*The same rules apply with N+_Select and P+_Select reversed.

Stay Safe and Stay Healthy !

End of Lecture 8