EE 330
Lecture 8
IC Fabrication Technology
Part II
  - Masking
  - Photolithography
  - Deposition
  - Etching
  - Diffusion
  - Oxidation
Review from Last Time

MOS Transistor

- Gate
- Source
- Drain
- Bulk

p-channel MOSFET

- Lightly-doped n-type (5x10^{16}/cm^3 range)
- More heavily-doped p-type (10^{18}/cm^3 range)
- Lightly doped p-type (10^{15}/cm^3 range)
Review from Last Time

Generic Process Flow

- Wafer Fabrication
- Mask Fabrication
- Epitaxy
- Grow or Apply
- Photoresist
- Deposit or Implant
- Etch
- Strip
- Planarization
- Wafer Probe
- Wafer Dicing
- Die Attach
- Wire Attach (bonding)
- Package
- Test
- Ship

Front End

Back End
IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Etching
- Diffusion
- Oxidation
- Epitaxy
- Polysilicon
- Contacts, Interconnect and Metalization
- Planarization
MOS Transistor

n-type
n+-type
p-type
p+-type
SiO₂ (insulator)
POLY (conductor)

Drain
Gate
Source

n-channel MOSFET
MOS Transistor

p-channel MOSFET

Review
n-channel MOS transistor in Bulk CMOS n-well process with bulk contact

p-substrate serves as the BULK for n-channel devices
p-channel MOS transistor in Bulk CMOS n-well process with bulk contact and well (tub)

Serves as the BULK for p-channel devices
MOS Transistor

• Single-crystalline silicon
  − Serves as physical support member
  − Lightly doped
  − Vertical dimensions are not linearly depicted
  − Often termed the Bulk
MOS Transistor

- Single-crystalline silicon
  - Serves as physical support member
  - Lightly doped
  - Vertical dimensions are not linearly depicted
  - Often termed the BULK
MOS Transistor

- Single-crystalline silicon
  - Serves as physical support member
  - Lightly doped (p-doping in the $10^{15}/\text{cm}^3$ range, silicon in the $2.2\times10^{22}/\text{cm}^3$ range)
  - Vertical dimensions are not linearly depicted
  - Often termed the BULK

- More heavily doped ($10^{17}/\text{cm}^3$ range)

- Conductor (usually polysilicon)

- Thin insulator (10A to 50A range)
p-channel MOSFET

Lightly-doped n-type
(5x10^{16}/cm^3 range)

More heavily-doped p-type
(10^{18}/cm^3 range)

Lightly doped p-type
(10^{15}/cm^3 range)
Crystal Preparation

• Large crystal is grown (pulled)
  – 12 inches (300mm) in diameter and 1 to 2 m long
  – Sliced to 250μm to 500μm thick
    • Prefer to be much thinner but thickness needed for mechanical integrity
  – 4 to 8 cm/hr pull rate
  – T=1430 °C

• Crystal is sliced to form wafers
• Cost for 12” wafer around $200
• 5 companies provide 90% of worlds wafers
• Somewhere around 400,000 12in wafers/month
Crystal Preparation

12 in
1 to 2 m
250µm to 500µm

Lightly-doped silicon
Excellent crystalline structure

Some predict newer FABs to be at 450mm (18in) by 2020 but uncertain whether it will happen.
Crystal Preparation

From www.infras.com
Crystal Preparation

Source: WEB
Crystal Preparation

- Seed
- Single Silicon Crystal
- Quartz Crucible
- Water Cooled Chamber
- Heat Shield
- Carbon Heater
- Graphite Crucible
- Crucible Support
- Spill Tray
- Electrode

Source: WEB
Crystal Preparation

Source: WEB
Crystal Preparation

A section of 300mm ingot is loaded into a wire saw

Source: WEB
Crystal Preparation

Source: WEB
Masking

• Use masks or reticles to define features on a wafer
  – Masks same size as wafer
  – Reticles used for projection
  – Reticle much smaller (but often termed mask)
  – Reticles often of quartz with chrome
  – Quality of reticle throughout life of use is critical
  – Single IC may require 20 or more reticles
  – Cost of “mask set” now exceeds $1 million for state of the art processes
  – Average usage 500 to 1500 times
  – Mask costs exceeding 50% of total fabrication costs in sub 100nm processes
  – Serve same purpose as a negative (or positive) in a photographic process
  – Usually use 4X optical reduction - exposure area approx. 860mm²
    (now through 2022 ITRS 2007 litho, Table LITH3a)
Step and Repeat (stepper) used to image across wafer
Masking

Exposure through reticle
Masking

Mask Features
Mask Features Intentionally Distorted to Compensate for Wavelength Limitations in Small Features
IC Fabrication Technology

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Photolithographic Process

• Photoresist
  – Viscous Liquid
  – Uniform Application Critical (spinner)
  – Baked to harden
  – Approx 1μ thick
  – Non-Selective
  – Types
    • Negative – unexposed material removed when developed
    • Positive-exposed material removed when developed
    • Thickness about 450nm in 90nm process (ITRS 2007 Litho)

• Exposure
  – Projection through reticle with stepper (scanners becoming popular)
  – Alignment is critical !!
  – E-Bean Exposures
    • Eliminate need fro reticle
    • Capacity very small

Stepper: Optics fixed, wafer steps in fixed increments
Scanner: Wafer steps in fixed increments and during exposure both optics and wafer are moved to increase effective reticle size
Steppers

Stepper costs in the $10M range with thru-put of around 100 wafers/hour
Steppers
Mask Alignment

Correctly Aligned
Mask Alignment

Alignment Errors

ΔX

ΔY

ΔX

ΔY
Mask Alignment

Other alignment marks  (http://www.mems-exchange.org/users/masks/intro-equipment.html)
IC Fabrication Technology

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Deposition

• Application of something to the surface of the silicon wafer or substrate
  – Layers 15A to 20u thick

• Methods
  – Physical Vapor Deposition (nonselective)
    • Evaporation/Condensation
    • Sputtering (better host integrity)
  – Chemical Vapor Deposition (nonselective)
    • Reaction of 2 or more gases with solid precipitate
    • Reduction by heating creates solid precipitate (pyrolytic)
  – Screening (selective)
    • For thick films
    • Low Tech, not widely used today
Deposition

Example: Chemical Vapor Deposition

Silane (SiH$_4$) is a gas (toxic and spontaneously combustible in air) at room temperature but breaks down into Si and H$_2$ above 400$^\circ$C so can be used to deposit Si.

\[ \text{SiH}_4 \rightarrow \text{Si} + 2\text{H}_2 \]
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Implantation

Application of impurities into the surface of the silicon wafer or substrate

- Individual atoms are first ionized (so they can be accelerated)
- Impinge on the surface and burry themselves into the upper layers
- Often very shallow but with high enough energy can go modestly deep
- Causes damage to target on impact
- Annealing heals most of the damage
- Very precise control of impurity numbers is possible
- Very high energy required
- High-end implanters considered key technology for national security
Ion Implantation Process

From http://www.casetechnology.com/implanter
Ion Implantation Process

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Ion Implanter

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End of Lecture 8