EE 330
Lecture 8
IC Fabrication Technology
Part II
- Masking
- Photolithography
- Deposition
? - Etching
? - Diffusion
Technology Files

• Provide Information About Process
  – Process Flow (Fabrication Technology)
  – Model Parameters
  – Design Rules
• Serve as Interface Between Design Engineer and Process Engineer
• Insist on getting information that is deemed important for a design
  – Limited information available in academia
  – Foundries often sensitive to who gets access to information
  – Customer success and satisfaction is critical to foundries
Design Rules

- Give minimum feature sizes, spacing, and other constraints that are acceptable in a process
- Very large number of devices can be reliably made with the design rules of a process
- Yield and performance unpredictable and often low if rules are violated
- Compatible with design rule checker in integrated toolsets
Design rules give minimum feature sizes and spacings

Review from Last Time
Each transistor is a 4-terminal device
Bulk connection needed
### SCMOS Layout Rules - Poly

| Rule | Description                               | Lambda
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>3.1</td>
<td>Minimum width</td>
<td>SCMOS: 2</td>
</tr>
<tr>
<td>3.2</td>
<td>Minimum spacing over field</td>
<td>SCMOS: 2</td>
</tr>
<tr>
<td>3.2.a</td>
<td>Minimum spacing over active</td>
<td>SCMOS: 2</td>
</tr>
<tr>
<td>3.3</td>
<td>Minimum gate extension of active</td>
<td>SCMOS: 2</td>
</tr>
<tr>
<td>3.4</td>
<td>Minimum active extension of poly</td>
<td>SCMOS: 3</td>
</tr>
<tr>
<td>3.5</td>
<td>Minimum field poly to active</td>
<td>SCMOS: 1</td>
</tr>
</tbody>
</table>

**Diagram:**

- **Rule 3.5:** Minimum field poly to active
- **Rule 3.1:** Minimum width
- **Rule 3.2:** Minimum spacing over field
- **Rule 3.2.a:** Minimum spacing over active
- **Rule 3.3:** Minimum gate extension of active
- **Rule 3.4:** Minimum active extension of poly

- Poly
- Active
Review from Last Time

Design Rules

• We use MOSIS fabrication services

• Most universities do the same

• See www.MOSIS.com for design rules
Examples in slides

Table 2a: MOSIS SCMOS-Compatible Mappings

<table>
<thead>
<tr>
<th>Foundry</th>
<th>Process</th>
<th>Lambda (micro-meters)</th>
<th>Options</th>
</tr>
</thead>
<tbody>
<tr>
<td>ON Semi</td>
<td>C5F/N (0.5 micron n-well)</td>
<td>0.35</td>
<td>SCN3M, SCN3ME</td>
</tr>
<tr>
<td>TSMC</td>
<td>0.35 micron 2P4M (4 Metal Polycided, 3.3 V/5 V)</td>
<td>0.25</td>
<td>SCN4ME</td>
</tr>
<tr>
<td>TSMC</td>
<td>0.35 micron 1P4M (4 Metal Silicided, 3.3 V/5 V)</td>
<td>0.25</td>
<td>SCN4M</td>
</tr>
</tbody>
</table>

Table 2b: MOSIS SCMOS_SUBM-Compatible Mappings

<table>
<thead>
<tr>
<th>Foundry</th>
<th>Process</th>
<th>Lambda (micro-meters)</th>
<th>Options</th>
</tr>
</thead>
<tbody>
<tr>
<td>ON Semi</td>
<td>C5F/N (0.5 micron n-well)</td>
<td>0.30</td>
<td>SCN3M_SUBM, SCN3ME_SUBM</td>
</tr>
<tr>
<td>TSMC</td>
<td>0.35 micron 2P4M (4 Metal Polycided, 3.3 V/5 V)</td>
<td>0.20</td>
<td>SCN4ME_SUBM</td>
</tr>
<tr>
<td>TSMC</td>
<td>0.35 micron 1P4M (4 Metal Silicided, 3.3 V/5 V)</td>
<td>0.20</td>
<td>SCN4M_SUBM</td>
</tr>
<tr>
<td>TSMC</td>
<td>0.25 micron 5 Metal 1 Poly (2.5 V/3.3 V)</td>
<td>0.15</td>
<td>SCN5M_SUBM</td>
</tr>
<tr>
<td>TSMC</td>
<td>0.18 micron 6 Metal 1 Poly (1.8 V/3.3 V)</td>
<td>0.10</td>
<td>SCN6M_SUBM</td>
</tr>
</tbody>
</table>

Table 2c: MOSIS SCMOS_DEEP-Compatible Mappings

<table>
<thead>
<tr>
<th>Foundry</th>
<th>Process</th>
<th>Lambda (micro-meters)</th>
<th>Options</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSMC</td>
<td>0.25 micron 5 Metal 1 Poly (2.5 V/3.3 V)</td>
<td>0.12</td>
<td>SCN5M_DEEP</td>
</tr>
<tr>
<td>TSMC</td>
<td>0.18 micron 6 Metal 1 Poly (1.8 V/3.3 V)</td>
<td>0.09</td>
<td>SCN6M_DEEP</td>
</tr>
</tbody>
</table>

Our labs and class projects
2.2. SCMOS Options

SCMOS options are used to designate projects that use additional layers beyond the standard single-poly, double metal CMOS. Each option is called out with a designator that is appended to the basic technology-code. Please note that not all possible combinations are available. The current list is shown in Table 1.

MOSIS has not issued SCMOS design rules for some vendor-supported options. For example, any designer using the SCMOS rules who wants the TSMC Thick_Top_Metal must draw the top metal to comply with the TSMC rules for that layer. Questions about other non-SCMOS layers should be directed to support@moss.com.

Table 1: SCMOS Technology Options

<table>
<thead>
<tr>
<th>Designation</th>
<th>Long Form</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>E</td>
<td>Electrode</td>
<td>Adds a second polysilicon layer (poly2) that can serve either as the upper electrode of a poly capacitor or (1.5 micron only) as a gate for transistors</td>
</tr>
<tr>
<td>A</td>
<td>Analog</td>
<td>Adds electrode (as in E option), plus layers for vertical NPN transistor pbase</td>
</tr>
<tr>
<td>3M</td>
<td>3 Metal</td>
<td>Adds second via (via2) and third metal (metal3) layers</td>
</tr>
<tr>
<td>4M</td>
<td>4 Metal</td>
<td>Adds 3M plus third via (via3) and fourth metal (metal4) layers</td>
</tr>
<tr>
<td>5M</td>
<td>5 Metal</td>
<td>Adds 4M plus fourth via (via4) and fifth metal (metal5) layers</td>
</tr>
<tr>
<td>6M</td>
<td>6 Metal</td>
<td>Adds 5M plus fifth via (via5) and sixth metal (metal6) layers</td>
</tr>
<tr>
<td>LC</td>
<td>Linear Capacitor</td>
<td>Adds a cap_well layer for linear capacitors</td>
</tr>
<tr>
<td>PC</td>
<td>Poly Cap</td>
<td>Adds poly_cap, a different layer for linear capacitors</td>
</tr>
<tr>
<td>SUBM</td>
<td>Sub-Micron</td>
<td>Uses revised layout rules for better fit to sub-micron processes (see section 2.4)</td>
</tr>
<tr>
<td>DEEP</td>
<td>Deep</td>
<td>Uses revised layout rules for better fit to deep sub-micron processes (see section 2.4)</td>
</tr>
<tr>
<td>Technology code with link to layer map</td>
<td>Layers</td>
<td></td>
</tr>
<tr>
<td>--------------------------------------</td>
<td>--------</td>
<td></td>
</tr>
<tr>
<td>SCNE</td>
<td>N_well, Active, N_select, P_select, Poly, Poly2, Contact, Metal1, Via, Metal2, Glass</td>
<td></td>
</tr>
<tr>
<td>SCNA</td>
<td>N_well, Active, N_select, P_select, Poly, Poly2, Contact, Pbase, Metal1, Via, Metal2, Glass</td>
<td></td>
</tr>
<tr>
<td>SCNPC</td>
<td>N_well, Active, N_select, P_select, Poly_cap, Poly, Contact, Metal1, Via, Metal2, Glass</td>
<td></td>
</tr>
<tr>
<td>SCN3M</td>
<td>N_well, Active, N_select, P_select, Poly, Silicide block (Agilent/HP only), Hi_Res_Implant, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass</td>
<td></td>
</tr>
<tr>
<td>SCN3ME</td>
<td>N_well, Active, N_select, P_select, Poly, Poly2, Hi_Res_Implant, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass</td>
<td></td>
</tr>
<tr>
<td>Technology code with link to layer map</td>
<td>Layers</td>
<td></td>
</tr>
<tr>
<td>---------------------------------------</td>
<td>--------</td>
<td></td>
</tr>
<tr>
<td>SCNE</td>
<td>N_well, Active, N_select, P_select, Poly, Poly2, Contact, Metal1, Via, Metal2, Glass</td>
<td></td>
</tr>
<tr>
<td>SCNA</td>
<td>N_well, Active, N_select, P_select, Poly, Poly2, Contact, Pbase, Metal1, Via, Metal2, Glass</td>
<td></td>
</tr>
<tr>
<td>SCNPC</td>
<td>N_well, Active, N_select, P_select, Poly_cap, Poly, Contact, Metal1, Via, Metal2, Glass</td>
<td></td>
</tr>
<tr>
<td>SCN3M</td>
<td>N_well, Active, N_select, P_select, Poly, Silicide block (Agilent/HP only), Hi_Res_Implant, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass</td>
<td></td>
</tr>
<tr>
<td>SCN3ME</td>
<td>N_well, Active, N_select, P_select, Poly, Poly2, Hi_Res_Implant, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass</td>
<td></td>
</tr>
</tbody>
</table>
### SCMOS Layout Rules - Well

<table>
<thead>
<tr>
<th>Rule</th>
<th>Description</th>
<th>Lambda</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>SCMOS</td>
</tr>
<tr>
<td>1.1</td>
<td>Minimum width</td>
<td>10</td>
</tr>
<tr>
<td>1.2</td>
<td>Minimum spacing between wells at different potential</td>
<td>9 ¹</td>
</tr>
<tr>
<td>1.3</td>
<td>Minimum spacing between wells at same potential</td>
<td>6 ³</td>
</tr>
<tr>
<td>1.4</td>
<td>Minimum spacing between wells of different type (if both are drawn)</td>
<td>0</td>
</tr>
</tbody>
</table>

**Exceptions for AMIS C30 0.35 micron process:**

¹ Use lambda=16 for rule 1.2 only when using SCN4M or SCN4ME

² Use lambda=21 for rule 1.2 only when using SCN4M_SUBM or SCN4ME_SUBM

³ Use lambda=8 for rule 1.3 only when using SCN4M or SCN4ME

⁴ Use lambda=11 for rule 1.3 only when using SCN4M_SUBM or SCN4ME_SUBM
<table>
<thead>
<tr>
<th>Technology code with link to layer map</th>
<th>Layers</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCNE</td>
<td>N_well, Active, N_select, P_select, Poly, Poly2, Contact, Metal1, Via, Metal2, Glass</td>
</tr>
<tr>
<td>SCNA</td>
<td>N_well, Active, N_select, P_select, Poly, Poly2, Contact, Pbase, Metal1, Via, Metal2, Glass</td>
</tr>
<tr>
<td>SCNPC</td>
<td>N_well, Active, N_select, P_select, Poly_cap, Poly, Contact, Metal1, Via, Metal2, Glass</td>
</tr>
<tr>
<td>SCN3M</td>
<td>N_well, Active, N_select, P_select, Poly, Silicide block (Agilent/HP only), Hi_Res_Implant, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass</td>
</tr>
<tr>
<td>SCN3ME</td>
<td>N_well, <strong>Active</strong>, N_select, P_select, Poly, Poly2, Hi_Res_Implant, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass</td>
</tr>
</tbody>
</table>
### SCMOS Layout Rules - Active

<table>
<thead>
<tr>
<th>Rule</th>
<th>Description</th>
<th>Lambda</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>2.1</td>
<td>Minimum width</td>
<td>3 *</td>
<td>3 *</td>
</tr>
<tr>
<td>2.2</td>
<td>Minimum spacing</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>2.3</td>
<td>Source/drain active to well edge</td>
<td>5</td>
<td>6</td>
</tr>
<tr>
<td>2.4</td>
<td>Substrate/well contact active to well edge</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>2.5</td>
<td>Minimum spacing between non-abutting active of different implant. Abutting active (&quot;split-active&quot;) is illustrated under Select Layout Rules.</td>
<td>4</td>
<td>4</td>
</tr>
</tbody>
</table>

* Note: For analog and critical digital designs, MOSIS recommends the following minimum MOS channel widths (active under poly) for AMIS designs. Narrower devices, down to design rule minimum, will be functional, but their electrical characteristics will not scale, and their performance is not predictable from MOSIS SPICE parameters.

<table>
<thead>
<tr>
<th>Process</th>
<th>Design Technology</th>
<th>Design Lambda (micrometers)</th>
<th>Minimum Width (lambda)</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMI_ABH</td>
<td>SCNA, SCNE</td>
<td>0.80</td>
<td>5</td>
</tr>
<tr>
<td>AMI_C5F/N</td>
<td>SCN3M, SCN3ME</td>
<td>0.35</td>
<td>9</td>
</tr>
<tr>
<td>AMI_C5F/N</td>
<td>SCN3M_SUBM, SCN3ME_SUBM</td>
<td>0.30</td>
<td>10</td>
</tr>
</tbody>
</table>

![Diagram showing active regions and spacing rules](image)
<table>
<thead>
<tr>
<th>Technology code with link to layer map</th>
<th>Layers</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCNE</td>
<td>N_well, Active, N_select, P_select, Poly, Poly2, Contact, Metal1, Via, Metal2, Glass</td>
</tr>
<tr>
<td>SCNA</td>
<td>N_well, Active, N_select, P_select, Poly, Poly2, Contact, Pbase, Metal1, Via, Metal2, Glass</td>
</tr>
<tr>
<td>SCNPC</td>
<td>N_well, Active, N_select, P_select, Poly_cap, Poly, Contact, Metal1, Via, Metal2, Glass</td>
</tr>
<tr>
<td>SCN3M</td>
<td>N_well, Active, N_select, P_select, Poly, Silicide block (Agilent/HP only), Hi_Res_Implant, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass</td>
</tr>
<tr>
<td>SCN3ME</td>
<td>N_well, Active, N_select, P_select, Poly, Poly2, Hi_Res_Implant, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass</td>
</tr>
</tbody>
</table>
## SCMOS Layout Rules - Poly

<table>
<thead>
<tr>
<th>Rule</th>
<th>Description</th>
<th>Lambda</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>SCMOS</td>
</tr>
<tr>
<td>3.1</td>
<td>Minimum width</td>
<td>2</td>
</tr>
<tr>
<td>3.2</td>
<td>Minimum spacing over field</td>
<td>2</td>
</tr>
<tr>
<td>3.2.a</td>
<td>Minimum spacing over active</td>
<td>2</td>
</tr>
<tr>
<td>3.3</td>
<td>Minimum gate extension of active</td>
<td>2</td>
</tr>
<tr>
<td>3.4</td>
<td>Minimum active extension of poly</td>
<td>3</td>
</tr>
<tr>
<td>3.5</td>
<td>Minimum field poly to active</td>
<td>1</td>
</tr>
<tr>
<td>Technology code with link to layer map</td>
<td>Layers</td>
<td></td>
</tr>
<tr>
<td>---------------------------------------</td>
<td>---------------------------------------</td>
<td></td>
</tr>
<tr>
<td>SCNE</td>
<td>N_well, Active, N_select, P_select, Poly, Poly2, Contact, Metal1, Via, Metal2, Glass</td>
<td></td>
</tr>
<tr>
<td>SCNA</td>
<td>N_well, Active, N_select, P_select, Poly, Poly2, Contact, Pbase, Metal1, Via, Metal2, Glass</td>
<td></td>
</tr>
<tr>
<td>SCNPC</td>
<td>N_well, Active, N_select, P_select, Poly_cap, Poly, Contact, Metal1, Via, Metal2, Glass</td>
<td></td>
</tr>
<tr>
<td>SCN3M</td>
<td>N_well, Active, N_select, P_select, Poly, Silicide block (Agilent/HP only), Hi_Res_Implant, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass</td>
<td></td>
</tr>
<tr>
<td>SCN3ME</td>
<td>N_well, Active, N_select, P_select, Poly, Poly2, Hi_Res_Implant, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass</td>
<td></td>
</tr>
</tbody>
</table>
### SCMOS Layout Rules - Select

<table>
<thead>
<tr>
<th>Rule</th>
<th>Description</th>
<th>Lambda</th>
<th>Lambda</th>
<th>Lambda</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.1</td>
<td>Minimum select spacing to channel of transistor to ensure adequate source/drain width</td>
<td>3</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>4.2</td>
<td>Minimum select overlap of active</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>4.3</td>
<td>Minimum select overlap of contact</td>
<td>1</td>
<td>1</td>
<td>1.5</td>
</tr>
<tr>
<td>4.4</td>
<td>Minimum select width and spacing</td>
<td>2</td>
<td>2</td>
<td>4</td>
</tr>
</tbody>
</table>

(Note: P-select and N-select may be coincident, but must not overlap) (not illustrated)

*The same rules apply with N+ Select and P+ Select reversed.*
Technology Files

- Design Rules

Process Flow (Fabrication Technology)

- Model Parameters  (will discuss in substantially more detail after device operation and more advanced models are introduced)
IC Fabrication Technology

See Chapter 3 and a little of Chapter 1 of WH
or Chapter 2 GAS for details
Generic Process Flow
IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Etching
- implantation
- Diffusion
- Oxidation
- Epitaxy
- Polysilicon
- Contacts, Interconnect and Metalization
- Planarization
Recall

MOS Transistor

n-type
n+-type
p-type
p+-type
SiO₂ (insulator)
POLY (conductor)

Drain
Gate
Source

n-channel MOSFET

Bulk

A

A'
MOS Transistor

n-type
n+-type
p-type
p+-type
SiO₂ (insulator)
POLY (conductor)
MOS Transistor

n-channel MOS transistor in Bulk CMOS n-well process with bulk contact

p-substrate serves as the BULK for n-channel devices
p-channel MOS transistor in Bulk CMOS n-well process with bulk contact and well (tub)

Serves as the BULK for p-channel devices
- **Single-crystalline silicon**
  - Serves as physical support member
  - Lightly doped
  - Vertical dimensions are not linearly depicted
  - Often termed the Bulk
MOS Transistor

- Single-crystalline silicon
  - Serves as physical support member
  - Lightly doped
  - **Vertical dimensions are not linearly depicted**
  - Often termed the BULK
MOS Transistor

- Single-crystalline silicon
  - Serves as physical support member
  - Lightly doped (p-doping in the $10^{15}$/cm$^3$ range, silicon in the $2.2\times10^{22}$/cm$^3$ range)
  - Vertical dimensions are not linearly depicted
  - Often termed the BULK

- More heavily doped ($10^{17}$/cm$^3$ range)

- Thin insulator (10A to 50A range)

- Conductor (usually polysilicon)

n-channel MOSFET
p-channel MOSFET

- Lightly-doped n-type (5x10^{16}/cm^3 range)
- More heavily-doped p-type (10^{18}/cm^3 range)
- Lightly doped p-type (10^{15}/cm^3 range)
Crystal Preparation

• Large crystal is grown (pulled)
  – 12 inches (300mm) in diameter and 1 to 2 m long
  – Sliced to 250μm to 500μm thick
    • Prefer to be much thinner but thickness needed for mechanical integrity
  – 4 to 8 cm/hr pull rate
  – T=1430 °C

• Crystal is sliced to form wafers
• Cost for 12” wafer around $200
• 5 companies provide 90% of worlds wafers
• Somewhere around 400,000 12in wafers/month
Crystal Preparation

Some predict newer FABs to be at 450mm (18in) by 2020 but uncertain whether it will happen.

Lightly-doped silicon
Excellent crystalline structure
Crystal Preparation

From www.infras.com
Crystal Preparation
Crystal Preparation

Source: WEB
Crystal Preparation

Source: WEB
Crystal Preparation

A section of 300mm ingot is loaded into a wiresaw

Source: WEB
Crystal Preparation
IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Etching
- Diffusion
- Oxidation
- Epitaxy
- Polysilicon
- Contacts, Interconnect and Metalization
- Planarization
Masking

- Use masks or reticles to define features on a wafer
  - Masks same size as wafer
  - Reticles used for projection
  - Reticle much smaller (but often termed mask)
  - Reticles often of quartz with chrome
  - Quality of reticle throughout life of use is critical
  - Single IC may require 20 or more reticles
  - Cost of “mask set” now exceeds $1 million for state of the art processes
  - Average usage 500 to 1500 times
  - Mask costs exceeding 50% of total fabrication costs in sub 100nm processes
  - Serve same purpose as a negative (or positive) in a photographic process
  - Usually use 4X optical reduction - exposure area approx. 860mm$^2$
    (now through 2022 ITRS 2007 litho, Table LITH3a)
Masking

Step and Repeat (stepper) used to image across wafer
Masking

Exposure through reticle
Masking

Mask Features
Masking Features Intentionally Distorted to Compensate for Wavelength Limitations in Small Features
IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
  - Deposition
  - Etching
  - Diffusion
  - Oxidation
  - Epitaxy
  - Polysilicon
  - Contacts, Interconnect and Metalization
  - Planarization
Photolithographic Process

- Photoresist
  - Viscous Liquid
  - Uniform Application Critical (spinner)
  - Baked to harden
  - Approx 1μ thick
  - Non-Selective
  - Types
    - Negative – unexposed material removed when developed
    - Positive-exposed material removed when developed
    - Thickness about 450nm in 90nm process (ITRS 2007 Litho)

- Exposure
  - Projection through reticle with stepper (scanners becoming popular)
  - Alignment is critical !!
  - E-Bean Exposures
    - Eliminate need fro reticle
    - Capacity very small

Stepper: Optics fixed, wafer steps in fixed increments
Scanner: Wafer steps in fixed increments and during exposure both optics and wafer are moved to increase effective reticle size
Steppers

Stepper costs in the $10M range with thru-put of around 100 wafers/hour
Steppers
Mask Alignment

Correctly Aligned
Mask Alignment

Alignment Errors

ΔX

ΔY
Mask Alignment

Other alignment marks  (http://www.mems-exchange.org/users/masks/intro-equipment.html)
IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Implantation
- Etching
- Diffusion
- Oxidation
- Epitaxy
- Polysilicon
- Contacts, Interconnect and Metalization
- Planarization
Deposition

• Application of something to the surface of the silicon wafer or substrate
  – Layers 15A to 20u thick

• Methods
  – Physical Vapor Deposition (nonselective)
    • Evaporation/Condensation
    • Sputtering (better host integrity)
  – Chemical Vapor Deposition (nonselective)
    • Reaction of 2 or more gases with solid precipitate
    • Reduction by heating creates solid precipitate (pyrolytic)
  – Screening (selective)
    • For thick films
    • Low Tech, not widely used today
Deposition

Example: Chemical Vapor Deposition

Silane (SiH$_4$) is a gas (toxic and spontaneously combustible in air) at room temperature but breaks down into Si and H$_2$ above 400°C so can be used to deposit Si.

$$\text{SiH}_4 \rightarrow \text{Si} + 2\text{H}_2$$
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Implantation

Application of impurities into the surface of the silicon wafer or substrate

- Individual atoms are first ionized (so they can be accelerated)
- Impinge on the surface and burry themselves into the upper layers
- Often very shallow but with high enough energy can go modestly deep
- Causes damage to target on impact
- Annealing heals most of the damage
- Very precise control of impurity numbers is possible
- Very high energy required
- High-end implanters considered key technology for national security
Ion Implanter

From http://www.casetechnology.com/implanter
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End of Lecture 8