EE 330
Lecture 9

IC Fabrication Technology
Quiz 8

A 2m silicon crystal is cut into wafers using a wire saw. If the wire diameter is 220um and the wafer thickness is 350um, how many wafers will this 2m crystal provide? In solving this problem you may neglect any wire vibration or abrasive particles used during cutting that would increase the width of the kerf.
And the number is ....
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Quiz 8

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Solution:

\[ n_w = \frac{Pull \ height}{t_{CUT} + t_{wafer}} = \frac{2m}{220\text{um} + 350\text{um}} \]

\[ n_w = \frac{2m}{220\text{um} + 350\text{um}} = 3509 \]
Review from Last Time

IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Implantation
  - Etching
  - Diffusion
  - Oxidation
  - Epitaxy
  - Polysilicon
  - Contacts, Interconnect and Metalization
  - Planarization
Review from Last Time

Crystal Preparation

Source: WEB
Review from Last Time

Masking

• Use masks or reticles to define features on a wafer
  – Masks same size as wafer
  – Reticles used for projection
  – Reticle much smaller (but often termed mask)
  – Reticles often of quartz with chrome
  – Quality of reticle throughout life of use is critical
  – Single IC may require 20 or more reticles
  – Cost of “mask set” now exceeds $1million for state of the art processes
  – Average usage 500 to 1500 times
  – Mask costs exceeding 50% of total fabrication costs in sub 100nm processes
  – Serve same purpose as a negative (or positive) in a photographic process
Photolithographic Process

• Photoresist
  – Viscous Liquid
  – Uniform Application Critical (spinner)
  – Baked to harden
  – Approx 1u thick
  – Non-Selective
  – Types
    • Negative – unexposed material removed when developed
    • Positive-exposed material removed when developed

• Exposure
  – Projection through reticle with stepper
  – Alignment is critical !!
  – E-Bean Exposures
    • Eliminate need for reticle
    • Capacity very small
Deposition

- Application of something to the surface of the silicon wafer or substrate
  - Layers 15A to 20u thick
- Methods
  - Physical Vapor Deposition (nonselective)
    - Evaporation/Condensation
    - Sputtering (better host integrity)
  - Chemical Vapor Deposition (nonselective)
    - Reaction of 2 or more gases with solid precipitate
    - Reduction by heating creates solid precipitate (pyrolytic)
  - Screening (selective)
    - For thick films
    - Low Tech, not widely used today
Implantation

Application of impurities into the surface of the silicon wafer or substrate
- Individual atoms are first ionized (so they can be accelerated)
- Impinge on the surface and burry themselves into the upper layers
- Often very shallow but with high enough energy can go modestly deep
- Causes damage to target on impact
- Annealing heals most of the damage
- Very precise control of impurity numbers is possible
- Very high energy required
- High-end implanters considered key technology for national security
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Etching

Selective Removal of Unwanted Materials

• Wet Etch
  – Inexpensive but under-cutting a problem

• Dry Etch
  – Often termed ion etch or plasma etch
Etching

Note: Vertical Dimensions Generally Orders of Magnitude Smaller Than Lateral Dimensions so Different Vertical and Lateral Scales Will be Used In This Discussion
Etching

Dry etch (anisotropic)

SiO₂

Photoresist

p- Silicon

Desired Physical Features

Dry Etch can provide very well-defined and nearly vertical edges (relative to photoresist patterning)
Etching (limited by photolithographic process)

SiO₂

p⁺ Silicon

Dry etch (anisotropic)

Photoresist

Consider neg photoresist

Over Exposed

Correctly Developed

Over Developed

Under Developed

Under Exposed

Correctly Developed

Over Developed

Under Developed
For Example, the wafer thickness is around 250\(\mu\) and the gate oxide is around 50A (5E-3\(\mu\)) and diffusion depths are around \(\lambda/5\).
Etching

**SiO$_2$**

**Photoresist**

**Undercutting (wet etch)**

**Desired Edges of SiO$_2$ from Mask**

**p-$\text{Si}$ Silicon**

**Isotropic Feature Degradation**

**Edge Movement Due to Over Etch, Over Exposure, or Over-Development**
Etching

**SiO$_2$**

**p$^-$ Silicon**

- Undercutting (wet etch)
- Desired Edges of SiO$_2$ from Mask
- Edge Movement Due to Over Etch, Over Exposure, or Over-Development

SiO$_2$ after photoresist removal
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Diffusion

• Controlled Migration of Impurities
  – Time and Temperature Dependent
  – Both vertical and lateral diffusion occurs
  – Crystal orientation affects diffusion rates in lateral and vertical dimensions
  – Materials Dependent
  – Subsequent Movement
  – Electrical Properties Highly Dependent upon Number and Distribution of Impurities
  – Diffusion at 800°C to 1200°C

• Source of Impurities
  – Deposition
  – Ion Implantation
    • Only a few Å deep
    • More accurate control of doping levels
    • Fractures silicon crystalline structure during implant
    • Annealing occurs during diffusion

• Types of Impurities
  – n-type  Arsenic, Antimony, Phosphorous
  – p-type  Gallium, Aluminum, Boron
Diffusion

Source of Impurities Deposited on Silicon Surface

Before Diffusion

After Diffusion
Diffusion

Source of Impurities Implanted in Silicon Surface

Before Diffusion

After Diffusion
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Oxidation

- SiO₂ is widely used as an insulator
  - Excellent insulator properties
- Used for gate dielectric
  - Gate oxide layers very thin
- Used to separate devices by raising threshold voltage
  - termed field oxide
  - field oxide layers very thick
- Methods of Oxidation
  - Thermal Growth (LOCOS)
    - Consumes host silicon
    - x units of SiO₂ consumes .47x units of Si
    - Undercutting of photoresist
    - Compromises planar surface for thick layers
    - Excellent quality
  - Chemical Vapor Deposition
    - Needed to put SiO₂ on materials other than Si
Oxidation

Thermally Grown SiO\textsubscript{2} - desired growth
Oxidation

Silicon Oxidation

Photoresist

SiO₂

Patterned Edges

p⁻ Silicon

Thermally Grown SiO₂ - actual growth

Bird's Beaking
Oxidation

Nonplanar Surface

p⁻ Silicon

Patterned Edges

Thermally Grown SiO₂ - actual growth
Oxidation

Silicon Nitride

Photoresist

Pad Oxide

$p^-$ Silicon

Shallow Trench Isolation (STI)
Shallow Trench Isolation (STI)

- **Oxidation**
- **p- Silicon**
- **Pad Oxide**
- **Etched Shallow Trench**
- **Silicon Nitride**
Oxidation

- Silicon Nitride
- CVD SiO₂
- Pad Oxide

Shallow Trench Isolation (STI)
Oxidation

Planarity Improved

Planarization Target

$p^-$ Silicon

Shallow Trench Isolation (STI)
Oxidation

After Planarization

CVD SiO$_2$

p-$\text{Silicon}$

Shallow Trench Isolation (STI)
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Epitaxy

• Single Crystaline Extension of Substrate Crystal
  – Commonly used in bipolar processes
  – CVD techniques
  – Impurities often added during growth
  – Grows slowly to allow alignment with substrate
Epitaxy

Epitaxial Layer

Original Silicon Surface

p-Silicon

epi can be uniformly doped or graded

Question: Why can’t a diffusion be used to create the same effect as an epi layer?
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Polysilicon

- Elemental contents identical to that of single crystaline silicon
  - Electrical properties much different
  - If doped heavily makes good conductor
  - If doped moderately makes good resistor
  - Widely used for gates of MOS devices
  - Widely used to form resistors
  - Grows fast over non-crystaline surface
  - Silicide often used in regions where resistance must be small
    - Refractory metal used to form silicide
    - Designer must indicate where silicide is applied (or blocked)
Polysilicon

Polysilicon

Single-Crystaline Silicon