Quiz 8

A 2m silicon crystal is cut into wafers using a wire saw. If the wire diameter is 220um and the wafer thickness is 350um, how many wafers will this 2m crystal provide? In solving this problem you may neglect any wire vibration or abrasive particles used during cutting that would increase the width of the kerf.
And the number is ....
And the number is ….
Quiz 8

A 2m silicon crystal is cut into wafers using a wire saw. If the wire diameter is 220um and the wafer thickness is 350um, how many wafers will this 2m crystal provide? In solving this problem you may neglect any wire vibration or abrasive particles used during cutting that would increase the width of the kerf.

Solution:

\[
\begin{align*}
   n_w &= \frac{\text{Pull height}}{t_{\text{CUT}} + t_{\text{wafer}}} = \frac{2m}{220\text{um} + 350\text{um}} \\
   n_w &= \frac{2m}{220\text{um} + 350\text{um}} = 3509
\end{align*}
\]
IC Fabrication Technology

- Crystal Preparation
- Masking
  - Photolithographic Process
  - Deposition
  - Implantation
  - Etching
  - Diffusion
  - Oxidation
  - Epitaxy
  - Polysilicon
  - Contacts, Interconnect and Metalization
- Planarization

Review from Last Time
Review from Last Time

Crystal Preparation

Source: WEB
Masking

• Use masks or reticles to define features on a wafer
  – Masks same size as wafer
  – Reticles used for projection
  – Reticle much smaller (but often termed mask)
  – Reticles often of quartz with chrome
  – Quality of reticle throughout life of use is critical
  – Single IC may require 20 or more reticles
  – Cost of “mask set” now exceeds $1million for state of the art processes
  – Average usage 500 to 1500 times
  – Mask costs exceeding 50% of total fabrication costs in sub 100nm processes
  – Serve same purpose as a negative (or positive) in a photographic process
IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
  - Deposition
  - Etching
  - Diffusion
  - Oxidation
  - Epitaxy
  - Polysilicon
  - Contacts, Interconnect and Metalization
- Planarization
Photolithographic Process

• Photoresist
  – Viscous Liquid
  – Uniform Application Critical (spinner)
  – Baked to harden
  – Approx 1u thick
  – Non-Selective
  – Types
    • Negative – unexposed material removed when developed
    • Positive-exposed material removed when developed
    • Thickness about 450nm in 90nm process (ITRS 2007 Litho)

• Exposure
  – Projection through reticle with stepper
  – Alignment is critical !!
  – E-Bean Exposures
    • Eliminate need fro reticle
    • Capacity very small
Mask Alignment

Correctly Aligned
Mask Alignment

Alignment Errors

ΔX

ΔY
IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
  - Deposition
  - Implantation
  - Etching
  - Diffusion
  - Oxidation
  - Epitaxy
  - Polysilicon
  - Contacts, Interconnect and Metalization
  - Planarization
Deposition

• Application of something to the surface of the silicon wafer or substrate
  – Layers 15A to 20u thick

• Methods
  – Physical Vapor Deposition (nonselective)
    • Evaporation/Condensation
    • Sputtering (better host integrity)
  – Chemical Vapor Deposition (nonselective)
    • Reaction of 2 or more gases with solid precipitate
    • Reduction by heating creates solid precipitate (pyrolytic)
  – Screening (selective)
    • For thick films
    • Low Tech, not widely used today
IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Implantation
- Etching
- Diffusion
- Oxidation
- Epitaxy
- Polysilicon
- Contacts, Interconnect and Metalization
- Planarization
Implantation

Application of impurities into the surface of the silicon wafer or substrate

- Individual atoms are first ionized (so they can be accelerated)
- Impinge on the surface and burry themselves into the upper layers
- Often very shallow but with high enough energy can go modestly deep
- Causes damage to target on impact
- Annealing heals most of the damage
- Very precise control of impurity numbers is possible
- Very high energy required
- High-end implanters considered key technology for national security
Ion Implantation Process

From http://www.casetechnology.com/implanter
Ion Implantation Process

From http://www.casetechnology.com/implanter
Ion Implanter

From http://www.casetechnology.com/implanter
IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Implantation
- Etching
- Diffusion
- Oxidation
- Epitaxy
- Polysilicon
- Contacts, Interconnect and Metalization
- Planarization
Etching

Selective Removal of Unwanted Materials

• Wet Etch
  – Inexpensive but under-cutting a problem

• Dry Etch
  – Often termed ion etch or plasma etch
Etching

Desired Physical Features

Note: Vertical Dimensions Generally Orders of Magnitude Smaller Than Lateral Dimensions so Different Vertical and Lateral Scales Will be Used In This Discussion
Dry Etch can provide very well-defined and nearly vertical edges (relative to photoresist patterning).
Etching (limited by photolithographic process)

SiO₂

Dry etch (anisotropic)

Photoresist

p-Silicon

Dry etch (anisotropic)

Consider neg photoresist

Over Exposed
- Correctly Developed
- Over Developed
- Under Developed

Under Exposed
- Correctly Developed
- Over Developed
- Under Developed

Under Exposed
- Correctly Developed
- Over Developed
- Under Developed
Lateral Relative to Vertical Dimensions

For Example, the wafer thickness is around 250\( \mu \text{m} \) and the gate oxide is around 50\( \text{A} \) (5E-3\( \mu \text{m} \)) and diffusion depths are around \( \lambda/5 \).
Etching

SiO₂

Photoresist

Undercutting (wet etch)

p⁻ Silicon

Isotropic Feature Degradation

Desired Edges of SiO₂ from Mask

Edge Movement Due to Over Etch, Over Exposure, or Over-Development
Etching

SiO₂

Undercutting (wet etch)

Desired Edges of SiO₂ from Mask

Edge Movement Due to Over Etch, Over Exposure, or Over-Development

SiO₂ after photoresist removal
IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Ion Implantation
- Etching
- Diffusion
- Oxidation
- Epitaxy
- Polysilicon
- Contacts, Interconnect and Metalization
- Planarization
Diffusion

• Controlled Migration of Impurities
  – Time and Temperature Dependent
  – Both vertical and lateral diffusion occurs
  – Crystal orientation affects diffusion rates in lateral and vertical dimensions
  – Materials Dependent
  – Subsequent Movement
  – Electrical Properties Highly Dependent upon Number and Distribution of Impurities
  – Diffusion at 800°C to 1200°C

• Source of Impurities
  – Deposition
  – Ion Implantation
    • Only a few Å deep
    • More accurate control of doping levels
    • Fractures silicon crystalline structure during implant
    • Annealing occurs during diffusion

• Types of Impurities
  – n-type  Arsenic, Antimony, Phosphorous
  – p-type  Gallium, Aluminum, Boron
Diffusion

Source of Impurities Deposited on Silicon Surface

Before Diffusion

After Diffusion
Diffusion

Source of Impurities Implanted in Silicon Surface

Before Diffusion

After Diffusion

p⁻ Silicon

p⁻ Silicon
Diffusion

Before Diffusion

Lateral Diffusion

After Diffusion

Implant

p-Silicon
p-Silicon
p-Silicon
p-Silicon
IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Ion Implantation
- Etching
- Diffusion
- Oxidation
- Epitaxy
- Polysilicon
- Contacts, Interconnect and Metalization
- Planarization
Oxidation

- SiO₂ is widely used as an insulator
  - Excellent insulator properties
- Used for gate dielectric
  - Gate oxide layers very thin
- Used to separate devices by raising threshold voltage
  - termed field oxide
  - field oxide layers very thick
- Methods of Oxidation
  - Thermal Growth (LOCOS)
    - Consumes host silicon
    - x units of SiO₂ consumes .47x units of Si
    - Undercutting of photoresist
    - Compromises planar surface for thick layers
    - Excellent quality
  - Chemical Vapor Deposition
    - Needed to put SiO₂ on materials other than Si
Oxidation

Photoresist

SiO$_2$

p$^-$ Silicon

Patterned Edges

Thermally Grown SiO$_2$ - desired growth
Oxidation

Thermally Grown SiO$_2$ - actual growth
Oxidation

Nonplanar Surface

p-Silicon

Patterned Edges

Thermally Grown SiO₂ - actual growth
Oxidation

Photoresist  Silicon Nitride  Pad Oxide

p-Silicon

Shallow Trench Isolation (STI)
Oxidation

Shallow Trench Isolation (STI)

 Silicon Nitride

Etched Shallow Trench

Pad Oxide

p-Silicon

Shallow Trench Isolation (STI)
Oxidation

Silicon Nitride

CVD SiO₂

Pad Oxide

p⁻ Silicon

Shallow Trench Isolation (STI)
Oxidation

Planarity Improved

Planarization Target

p⁻ Silicon

Shallow Trench Isolation (STI)
Oxidation

After Planarization

CVD SiO$_2$

$p^-$ Silicon

Shallow Trench Isolation (STI)
IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Ion Implantation
- Etching
- Diffusion
- Oxidation
- Epitaxy
- Polysilicon
- Contacts, Interconnect and Metalization
- Planarization
Epitaxy

• Single Crystaline Extension of Substrate Crystal
  – Commonly used in bipolar processes
  – CVD techniques
  – Impurities often added during growth
  – Grows slowly to allow alignment with substrate
Epitaxy

Epitaxial Layer

p⁻ Silicon

epi can be uniformly doped or graded

Original Silicon Surface

Question: Why can’t a diffusion be used to create the same effect as an epi layer?
IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Etching
- Diffusion
- Ion Implantation
- Oxidation
- Epitaxy
- Polysilicon
- Contacts, Interconnect and Metalization
- Planarization
Polysilicon

- Elemental contents identical to that of single crystalline silicon
  - Electrical properties much different
  - If doped heavily makes good conductor
  - If doped moderately makes good resistor
  - Widely used for gates of MOS devices
  - Widely used to form resistors
  - Grows fast over non-crystalline surface
  - Silicide often used in regions where resistance must be small
    - Refractory metal used to form silicide
    - Designer must indicate where silicide is applied (or blocked)
Polysilicon

Single-Crystalline Silicon