EE 330
Lecture 9

IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Implantation
- Etching
- Oxidation
- Epitaxy
- Polysilicon
- Planarization
- Resistance and Capacitance in Interconnect
Technology Files

• Design Rules

Process Flow (Fabrication Technology)

• Model Parameters (will discuss in substantially more detail after device operation and more advanced models are introduced)
IC Fabrication Technology

See Chapter 3 and a little of Chapter 1 of WH
or Chapter 2 GAS for details
Generic Process Flow

Front End

Wafer Fabrication
Epitaxy
Grow or Apply
Photoresist
Deposit or Implant
Etch
Strip
Planarization

Back End

Wafer Probe
Wafer Dicing
Die Attach
Wire Attach (bonding)
Package
Test
Ship
Recall

MOS Transistor

n-type
n+-type
p-type
p+-type
SiO$_2$ (insulator)
POLY (conductor)

Drain
Gate
Source

n-channel MOSFET
MOS Transistor

Review

p-channel MOSFET
MOS Transistor

n-channel MOS transistor in Bulk CMOS n-well process with bulk contact

p-substrate serves as the BULK for n-channel devices
p-channel MOS transistor in Bulk CMOS n-well process with bulk contact and well (tub)

Serves as the BULK for p-channel devices
MOS Transistor

- Single-crystalline silicon
  - Serves as physical support member
  - Lightly doped
  - Vertical dimensions are not linearly depicted
  - Often termed the Bulk
MOS Transistor

- Single-crystalline silicon
  - Serves as physical support member
  - Lightly doped
  - Vertical dimensions are not linearly depicted
  - Often termed the BULK
MOS Transistor

- Single-crystalline silicon
  - Serves as physical support member
  - Lightly doped (p-doping in the $10^{15}$/$cm^3$ range, silicon in the $2.2x10^{22}$/cm$^3$ range)
  - Vertical dimensions are not linearly depicted
  - Often termed the BULK

Conductor (usually polysilicon)

Thin insulator (10A to 50A range)

More heavily doped ($10^{17}$/cm$^3$ range)

n-channel MOSFET

- Dominant Doping Depicted – Generally Contain Prior Lower Density Dopants of Opposite Type
MOS Transistor

p-channel MOSFET

Bulk

Source

Lightly-doped n-type (5x10^{16}/cm^3 range)

More heavily-doped p-type (10^{18}/cm^3 range)

Lightly doped p-type (10^{15}/cm^3 range)

For Example: Drain Region Contains prior substrate p-dopants and n-type well dopants
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Crystal Preparation

• Large crystal is grown (pulled)
  – 12 inches (300mm) in diameter and 1 to 2 m long
  – Sliced to 250μm to 500μm thick
    • Prefer to be much thinner but thickness needed for mechanical integrity
  – 4 to 8 cm/hr pull rate
  – T=1430 °C

• Crystal is sliced to form wafers
• Cost for 12” wafer around $200
• 5 companies provide 90% of worlds wafers
• Somewhere around 400,000 12in wafers/month
## Crystal Preparation

<table>
<thead>
<tr>
<th>Wafer Size</th>
<th>Typical Thickness</th>
<th>Year Prodnt</th>
<th>Weight per Wafer</th>
<th>100 mm² Die per Wafer</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-inch (25 mm)</td>
<td></td>
<td>1960</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2-inch (51 mm)</td>
<td>275 µm</td>
<td>1969</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3-inch (76 mm)</td>
<td>375 µm</td>
<td>1972</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4-inch (100 mm)</td>
<td>525 µm</td>
<td>1976</td>
<td>10 grams</td>
<td>56</td>
</tr>
<tr>
<td>4.9 inch (125 mm)</td>
<td>625 µm</td>
<td>1981</td>
<td></td>
<td></td>
</tr>
<tr>
<td>150 mm (5.9 inch)</td>
<td>675 µm</td>
<td>1983</td>
<td></td>
<td></td>
</tr>
<tr>
<td>200 mm (7.9 inch)</td>
<td>725 µm</td>
<td>1992</td>
<td>53 grams</td>
<td>269</td>
</tr>
<tr>
<td>300 mm (11.8 inch)</td>
<td>775 µm</td>
<td>2002</td>
<td>125 grams</td>
<td>640</td>
</tr>
<tr>
<td>450 mm (17.7 inch)</td>
<td>925 µm</td>
<td>future</td>
<td>342 grams</td>
<td>1490</td>
</tr>
<tr>
<td>675-millimetre (26.6 in) (Theoretical)</td>
<td>Unknown.</td>
<td>future</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Crystal Preparation

300mm wafer

450 mm wafer
Crystal Preparation

Lightly-doped silicon
Excellent crystalline structure

Some predict newer FABs to be at 450mm (18in) by 2020 but appears to be uncertain whether it will ever happen.
Crystal Preparation

Return on Investment Essential to Make Transition

200mm (8”) and 300mm (12”) are dominant in production today
Crystal Preparation

From www.infras.com
Crystal Preparation
Crystal Preparation

Source: WEB
Crystal Preparation

Source: WEB
Crystal Preparation

A section of 300mm ingot is loaded into a wiresaw

Source: WEB
Crystal Preparation
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Masking

• Use masks or reticles to define features on a wafer
  – Masks same size as wafer
  – Reticles used for projection
  – Reticle much smaller (but often termed mask)
  – Reticles often of quartz with chrome
  – Quality of reticle throughout life of use is critical
  – Single IC may require 20 or more reticles
  – Cost of “mask set” now exceeds $1 million for state of the art processes
  – Average usage 500 to 1500 times
  – Mask costs exceeding 50% of total fabrication costs in sub 100nm processes
  – Serve same purpose as a negative (or positive) in a photographic process
  – Usually use 4X optical reduction - exposure area approx. 860mm$^2$

(now through 2022 ITRS 2007 litho, Table LITH3a)
Masking

Step and Repeat (stepper) used to image across wafer
Masking

Exposure through reticle
Masking

Mask Features
Masking Features Intentionally Distorted to Compensate for Wavelength Limitations in Small Features
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Photolithographic Process

• Photoresist
  – Viscous Liquid
  – Uniform Application Critical (spinner)
  – Baked to harden
  – Approx 1u thick
  – Non-Selective
  – Types
    • Negative – unexposed material removed when developed
    • Positive-exposed material removed when developed
    • Thickness about 450nm in 90nm process (ITRS 2007 Litho)

• Exposure
  – Projection through reticle with stepper (scanners becoming popular)
  – Alignment is critical !!
  – E-Bean Exposures
    • Eliminate need from reticle
    • Capacity very small

Stepper: Optics fixed, wafer steps in fixed increments
Scanner: Wafer steps in fixed increments and during exposure both optics and wafer are moved to increase effective reticle size
Steppers

Stepper costs in the $10M range with thru-put of around 100 wafers/hour
Steppers
Mask Alignment

Correctly Aligned
Mask Alignment

Alignment Errors

$\Delta X$

$\Delta Y$

$\Delta X$

$\Delta Y$
Mask Alignment

Other alignment marks (http://www.mems-exchange.org/users/masks/intro-equipment.html)
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Deposition

• Application of something to the surface of the silicon wafer or substrate
  – Layers 15A to 20u thick

• Methods
  – Physical Vapor Deposition (nonselective)
    • Evaporation/Condensation
    • Sputtering (better host integrity)
  – Chemical Vapor Deposition (nonselective)
    • Reaction of 2 or more gases with solid precipitate
    • Reduction by heating creates solid precipitate (pyrolytic)
  – Screening (selective)
    • For thick films
    • Low Tech, not widely used today
Deposition

Example: Chemical Vapor Deposition

Silane (SiH\(_4\)) is a gas (toxic and spontaneously combustible in air) at room temperature but breaks down into Si and H\(_2\) above 400\(^\circ\)C so can be used to deposit Si.

\[ \text{SiH}_4 \rightarrow \text{Si} + 2\text{H}_2 \]
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Implantation

Application of impurities into the surface of the silicon wafer or substrate

- Individual atoms are first ionized (so they can be accelerated)
- Impinge on the surface and burry themselves into the upper layers
- Often very shallow but with high enough energy can go modestly deep
- Causes damage to target on impact
- Annealing heals most of the damage
- Very precise control of impurity numbers is possible
- Very high energy required
- High-end implanters considered key technology for national security
Ion Implanter

From http://www.casetechnology.com/implanter
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Etching

Selective Removal of Unwanted Materials

- **Wet Etch**
  - Inexpensive but under-cutting a problem

- **Dry Etch**
  - Often termed ion etch or plasma etch
Etching

Desired Physical Features

Note: Vertical Dimensions in silicon generally orders of magnitude smaller than lateral dimensions so different vertical and lateral scales will be used in this discussion. Vertical dimensions of photoresist which is applied on top of wafer is about ½ order of magnitude larger than lateral dimensions.
Desired Physical Features

Dry Etch can provide very well-defined and nearly vertical edges (relative to photoresist patterning)
Stay Safe and Stay Healthy !
End of Lecture 9