EE 330
Lecture 9

Design Rules

IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Ion Implantation
- Etching
- Diffusion
- Oxidation
- Epitaxy
- Polysilicon
- Planarization
- Contacts, Interconnect and Metalization

Exam 1	Friday Sept 23	
Exam 2	Friday Oct 21	
Exam 3	Friday Nov 13	
Final	Tuesday Dec 13	12:00 – 2:00 p.m.

Review from Last Time

Design Rules

- Give minimum feature sizes, spacing, and other constraints that are acceptable in a process

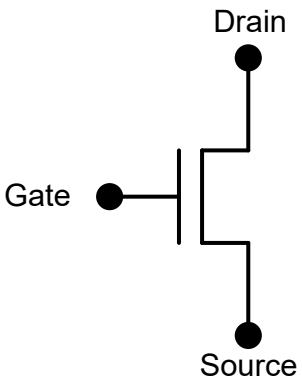
- Very large number of devices can be reliably made with the design rules of a process

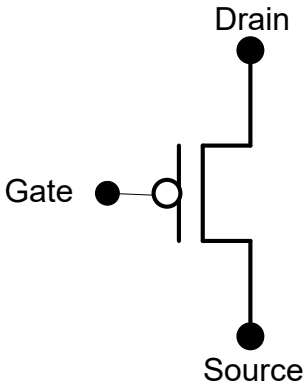
- Yield and performance unpredictable and often low if rules are violated

- Compatible with design rule checker in integrated toolsets

Review from Last Time

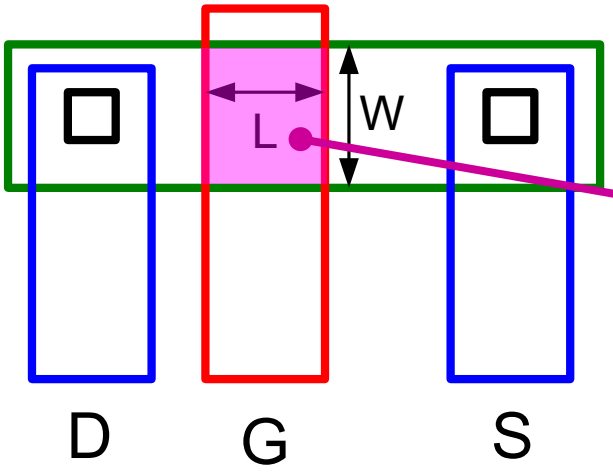
Design Rules and Layout – consider transistors



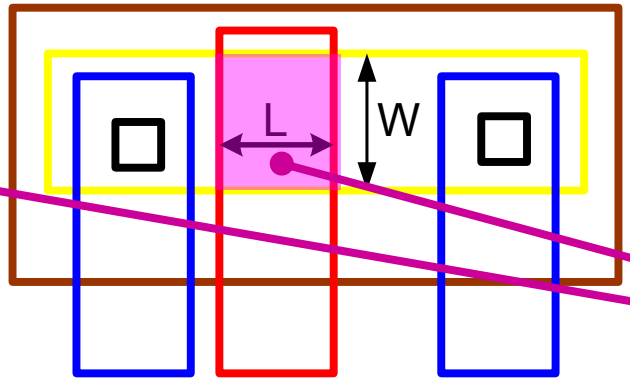


Layer Map

- p-active
- n-active
- Poly 1
- Metal 1
- n-well
- contact



Layout

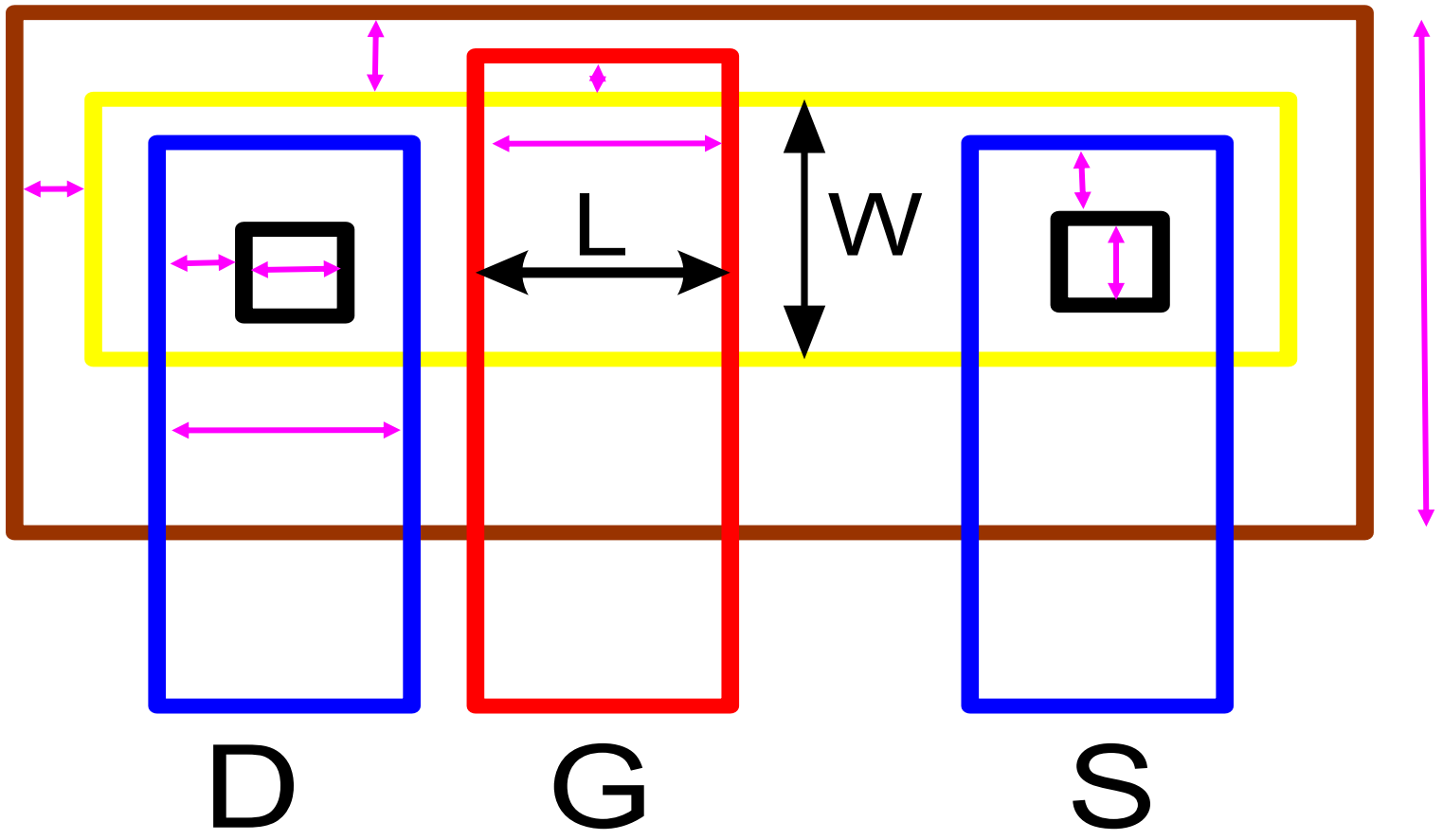


Layout

Everything useful in channel region. All other features just overhead that degrades performance

Review from Last Time

Design Rules

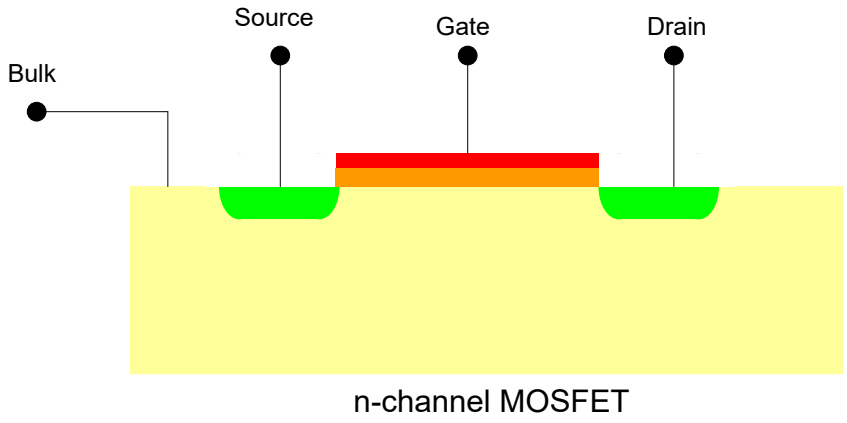


Design rules give minimum feature sizes and spacings

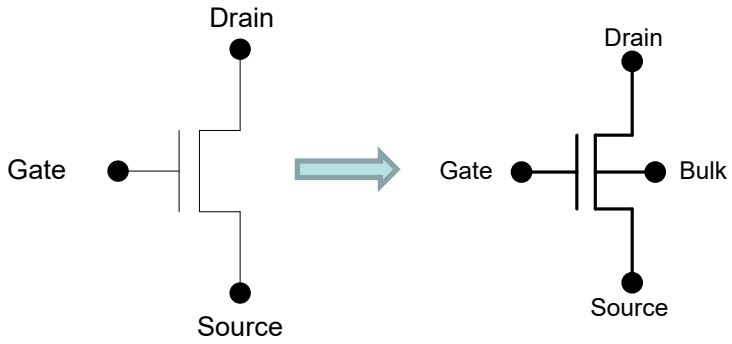
Designers generally do layouts to minimize size of circuit subject to design rule constraints (because yield, cost, and performance usually improve)

Review from Last Time

MOS Transistor Nomenclature



n-channel MOSFET

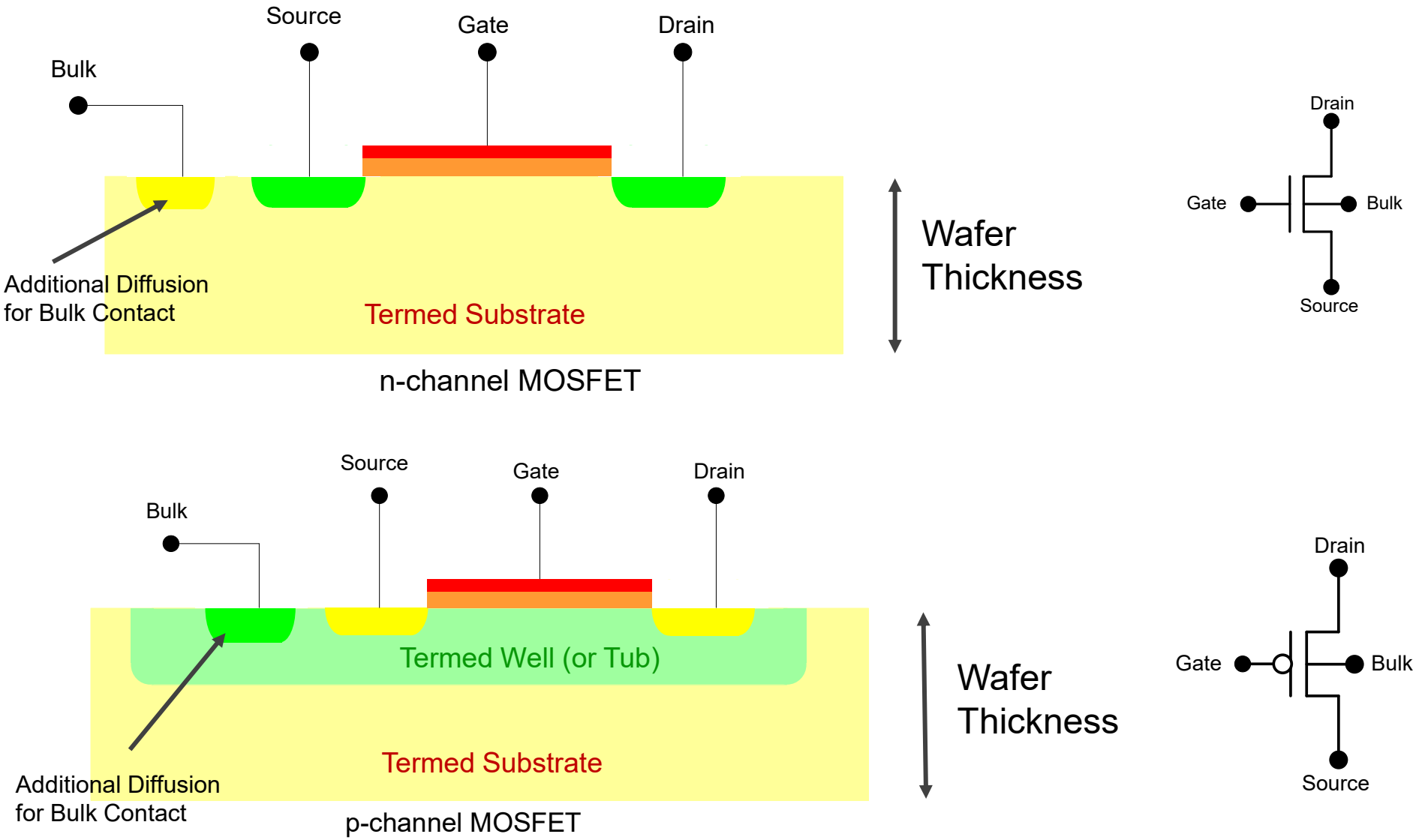


Metal Oxide Semiconductor ⇒ MOS

Early processes used metal for the gate, today metal is seldom used but the term MOS transistor is standard even though the gate is no longer metal

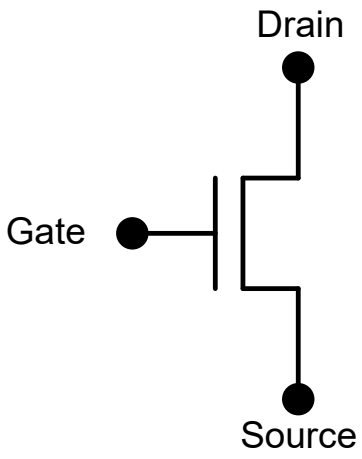
Review from Last Time

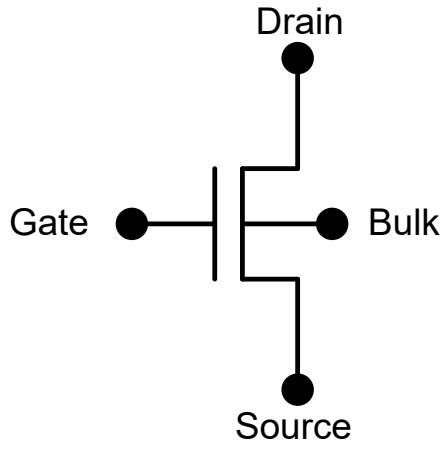
MOS Transistor in Bulk CMOS Process



Review from Last Time

Design Rules and Layout – consider transistors





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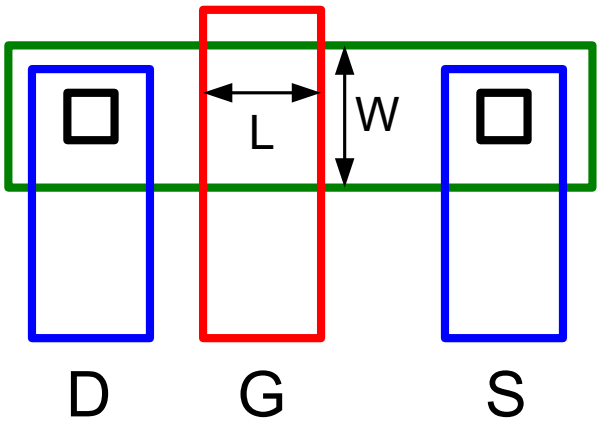
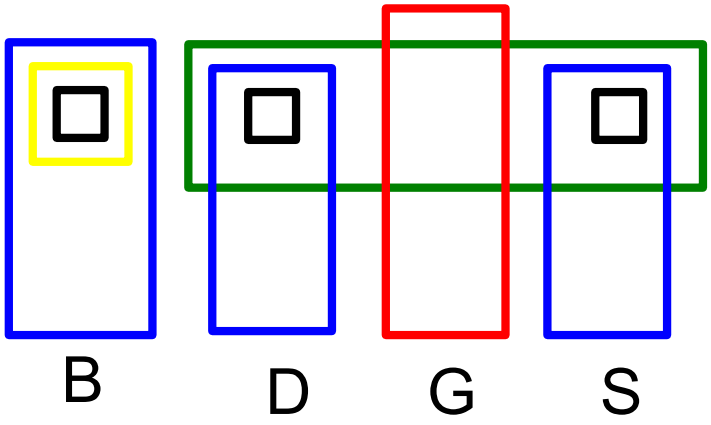
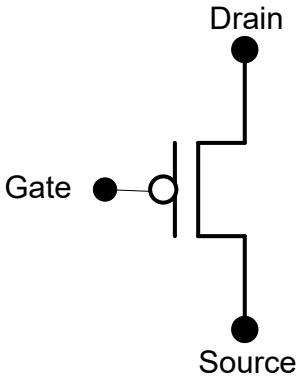


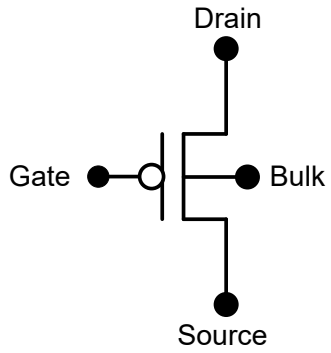


- Bulk connection needed
- Single bulk connection can often be used for several (many) transistors

Review from Last Time

Design Rules and Layout – consider transistors





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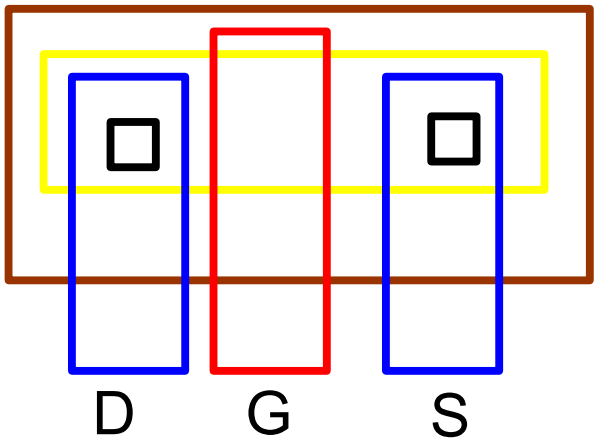
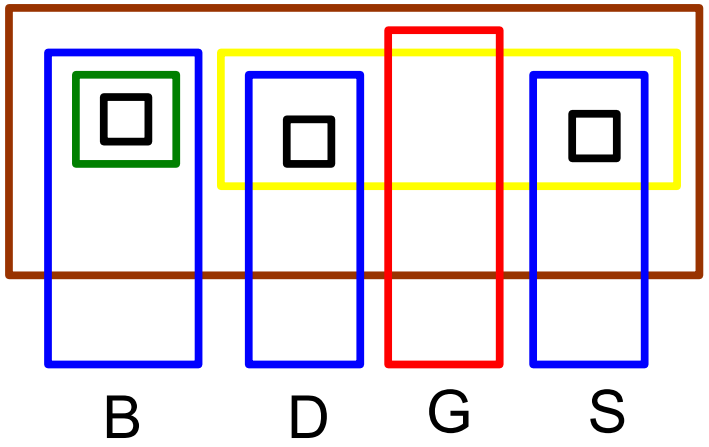
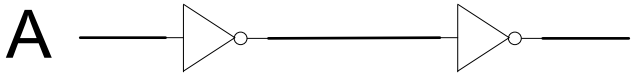




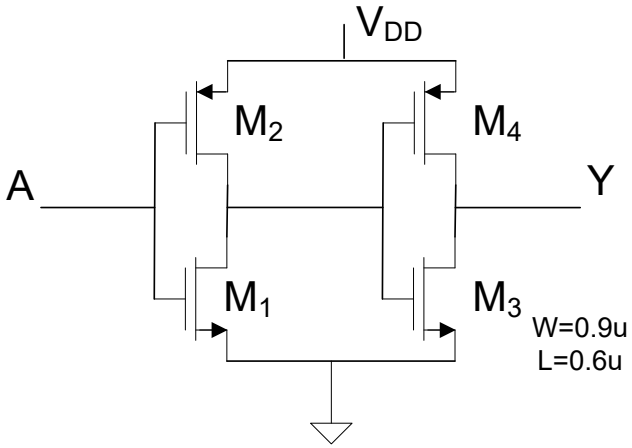
- Bulk connection needed
- Single bulk connection can often be used for several (many) transistors if they share the same well

Review from Last Time

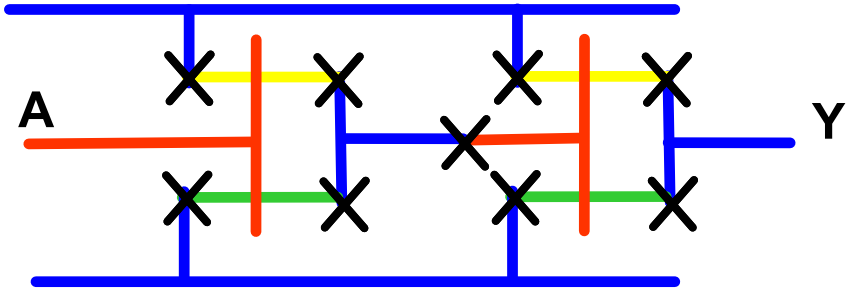
Design Rules and Layout (example)



Logic Circuit



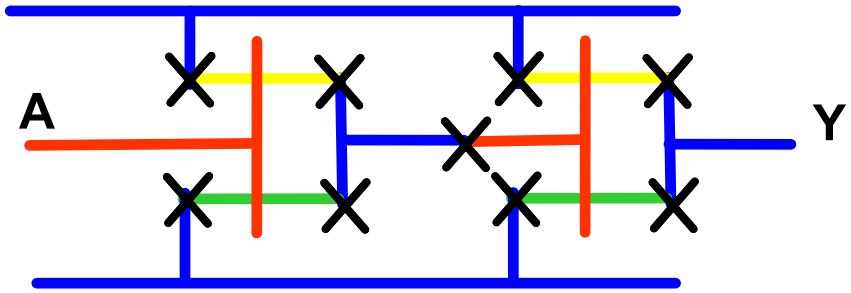
Circuit Schematic (Including Device Sizing)

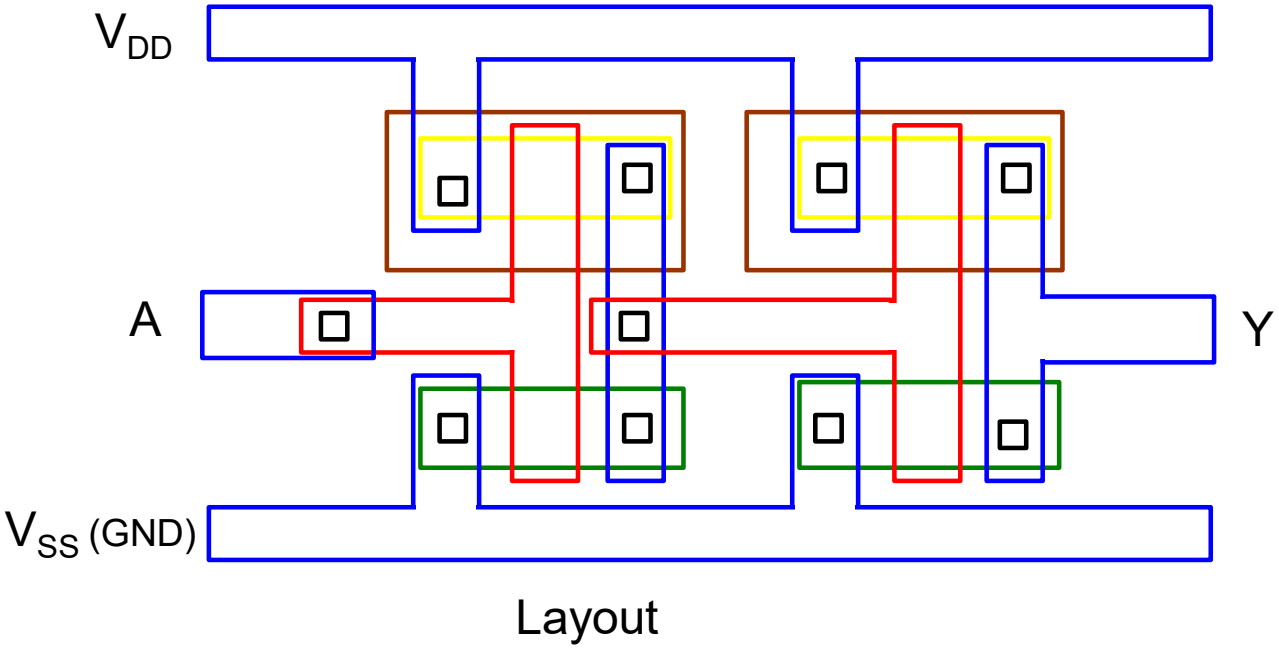


Stick Diagram

Review from Last Time

Design Rules (example)





Layout

Layer Map

- p-active
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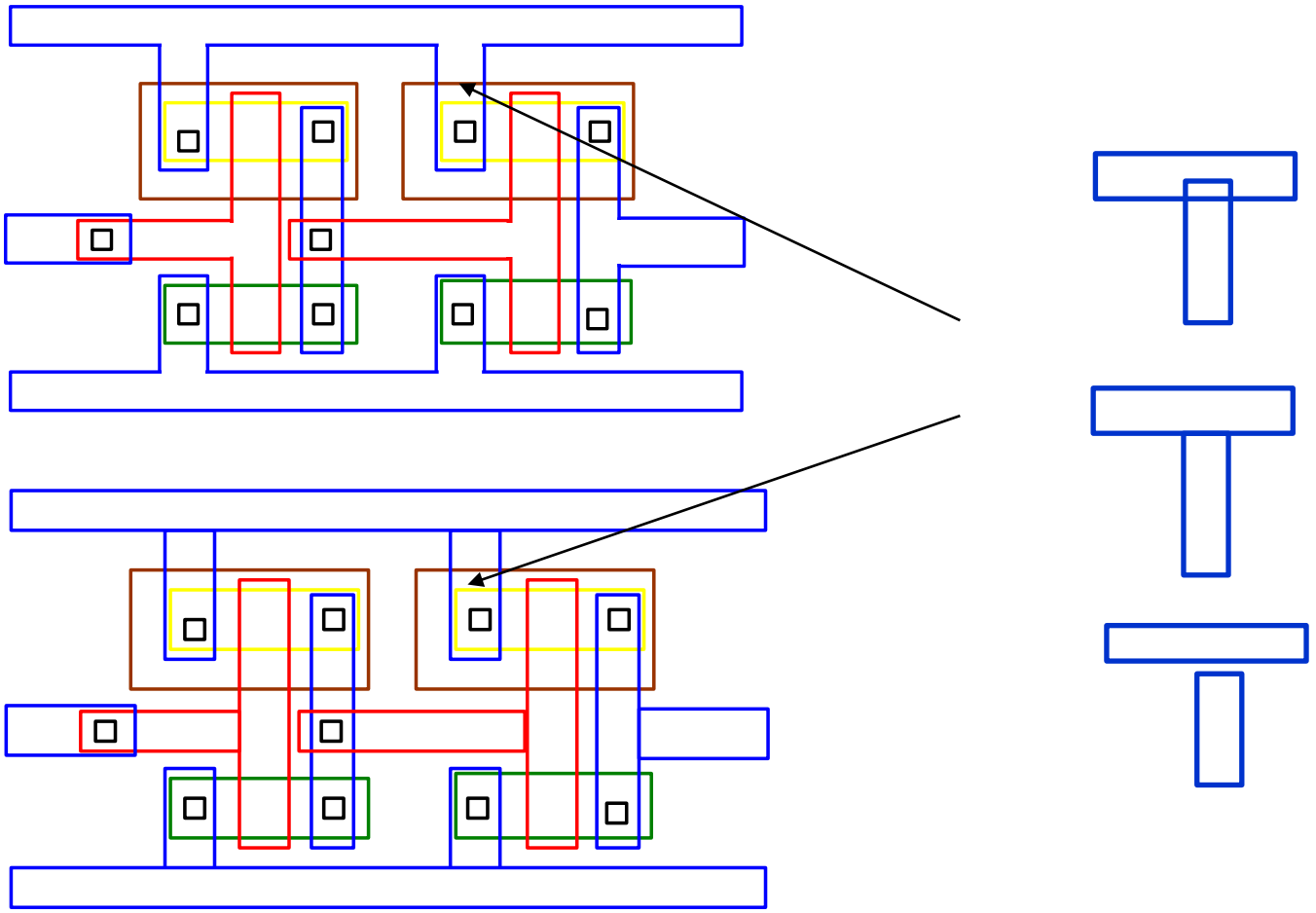
Review from Last Time

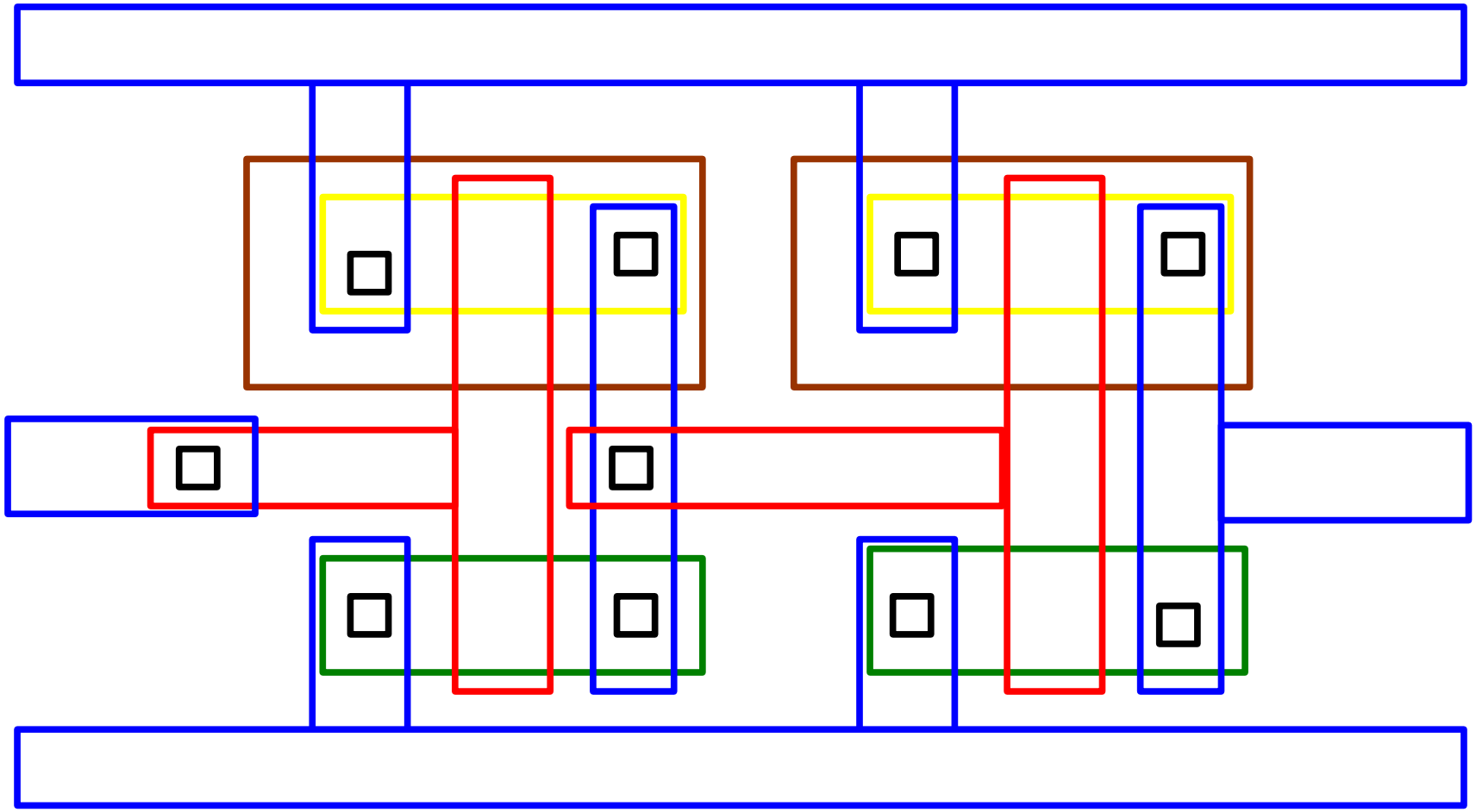
Design Rules (example)



- Polygons in Geometric Description File (GDF) merged (when driving the pattern generator that makes the masks)
- Separate rectangles generally more convenient to represent
- Good practice to overlap rectangles to avoid break (though such an error would likely be caught with DRC)

Review from Last Time

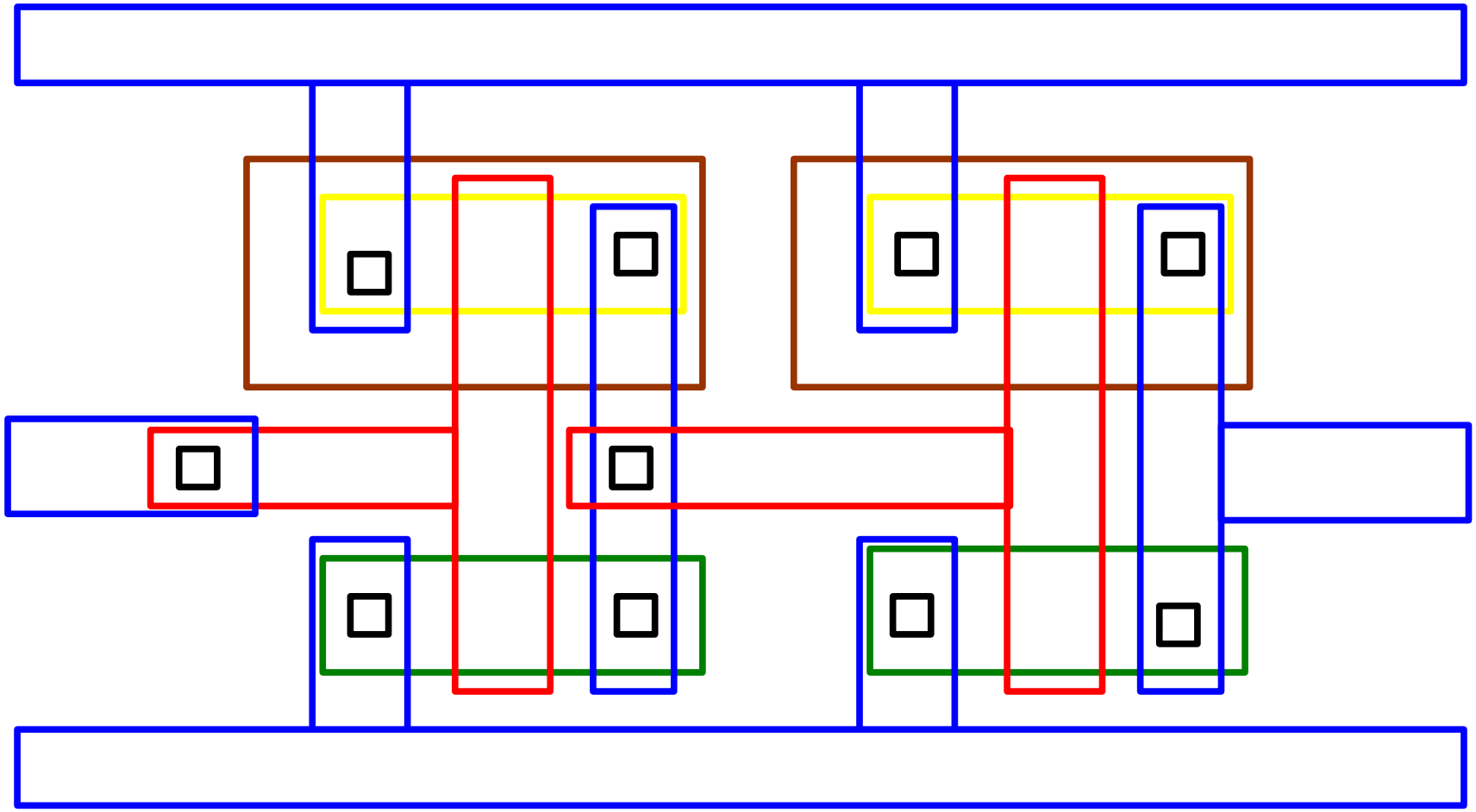
Design Rules (example)



- Design rules must be satisfied throughout the design
- DRC runs incrementally during layout in most existing tools to flag most problems
- DRC can catch layout design rule errors but not circuit connection errors

Review from Last Time

Design Rules (example)

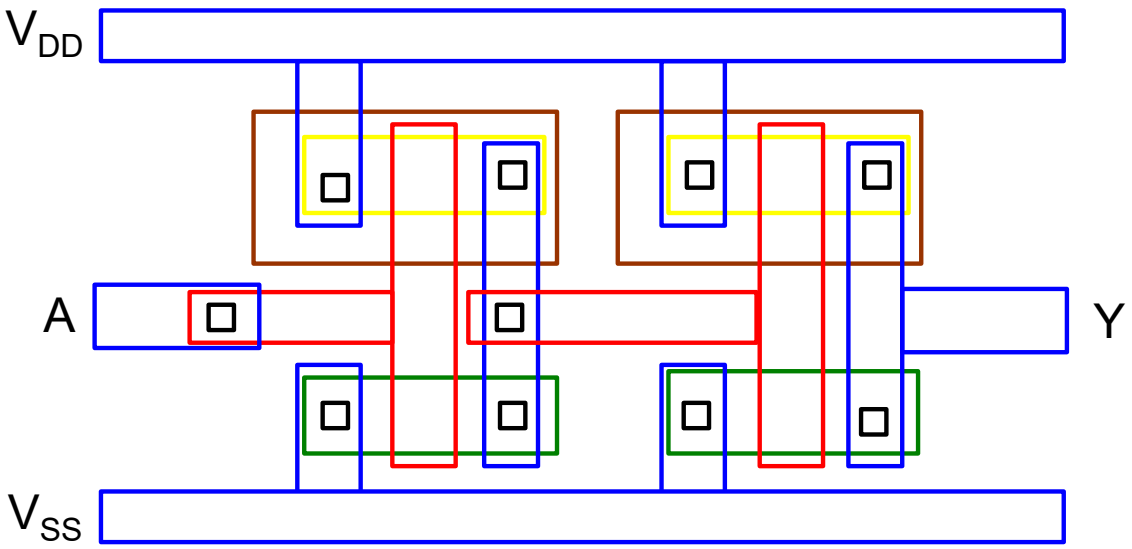


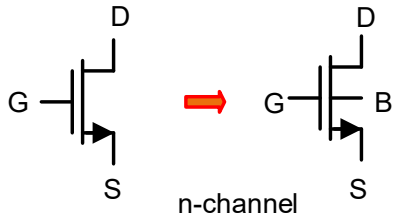
What is wrong with this layout ?

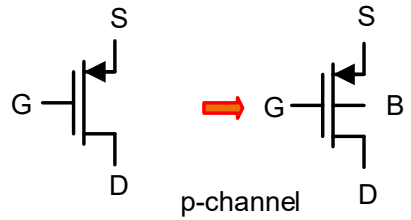
Bulk connections missing!

Review from Last Time

Design Rules (example)

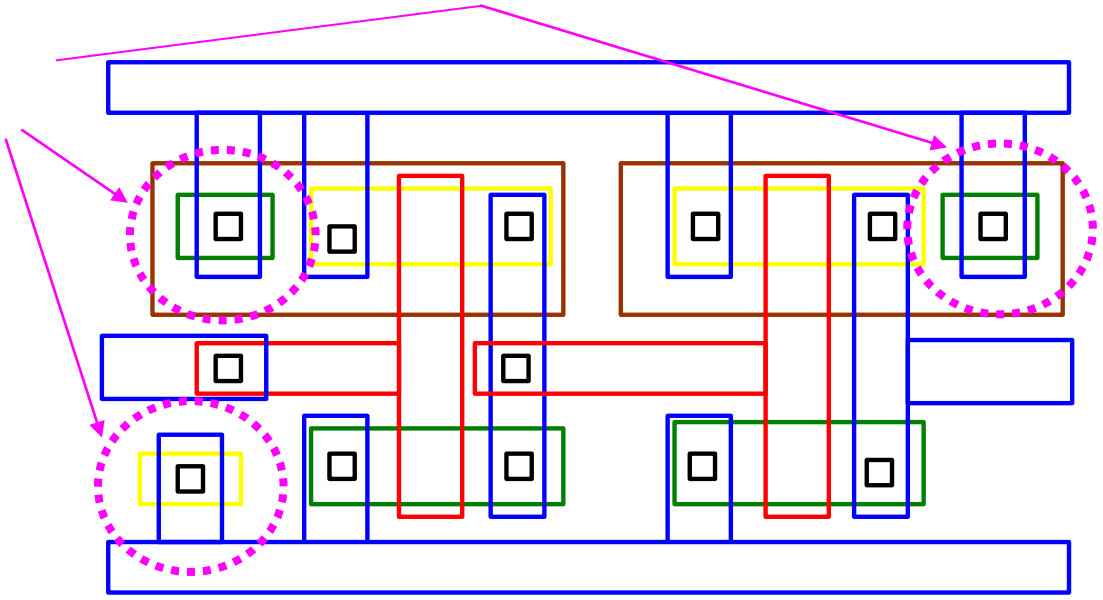






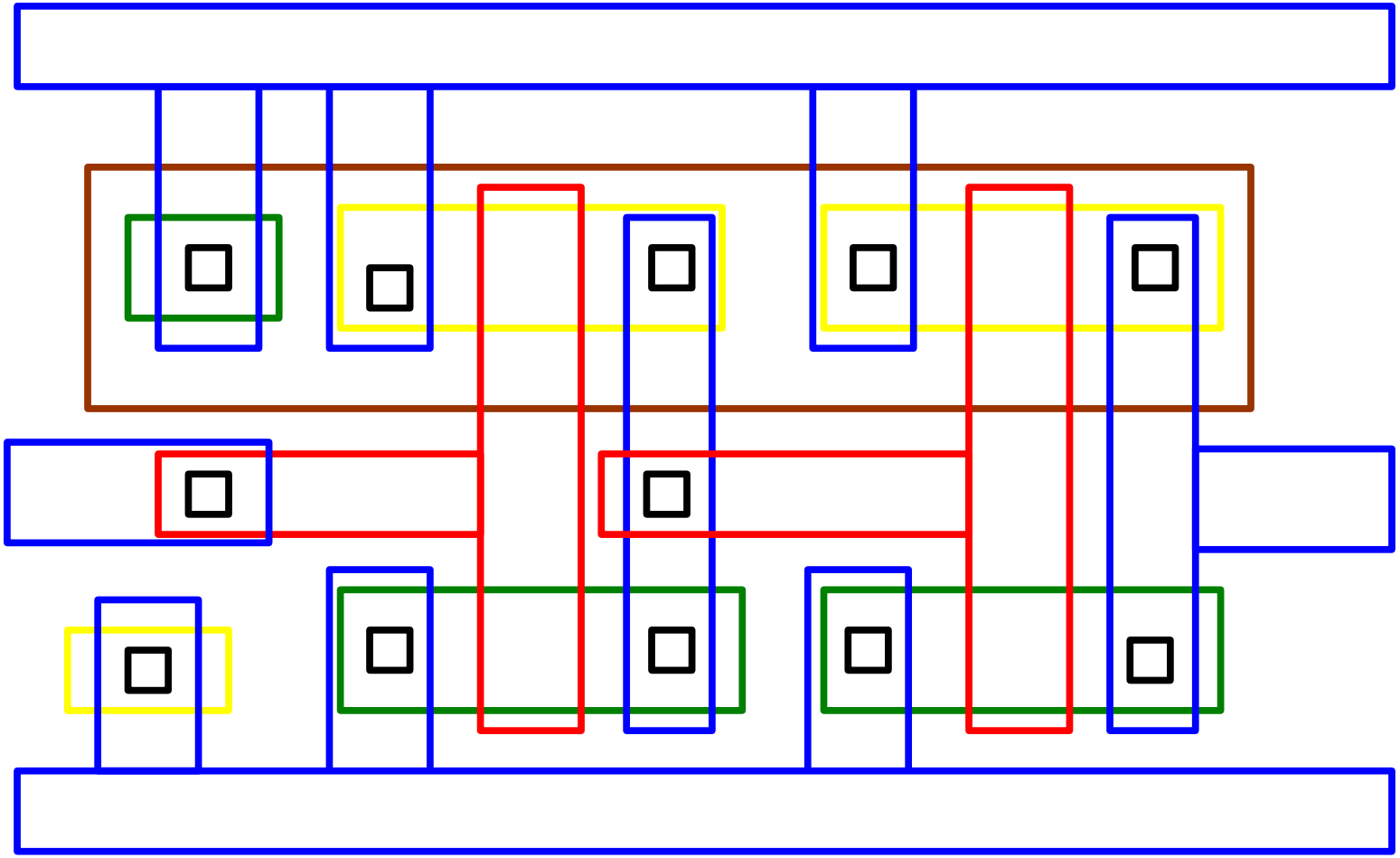
Actually 4-terminal device

- Note diffusions needed for bulk connections
- Note n-well connections increase area a significant amount
- Note n-wells are both connected to V_{DD} in this circuit



Review from Last Time

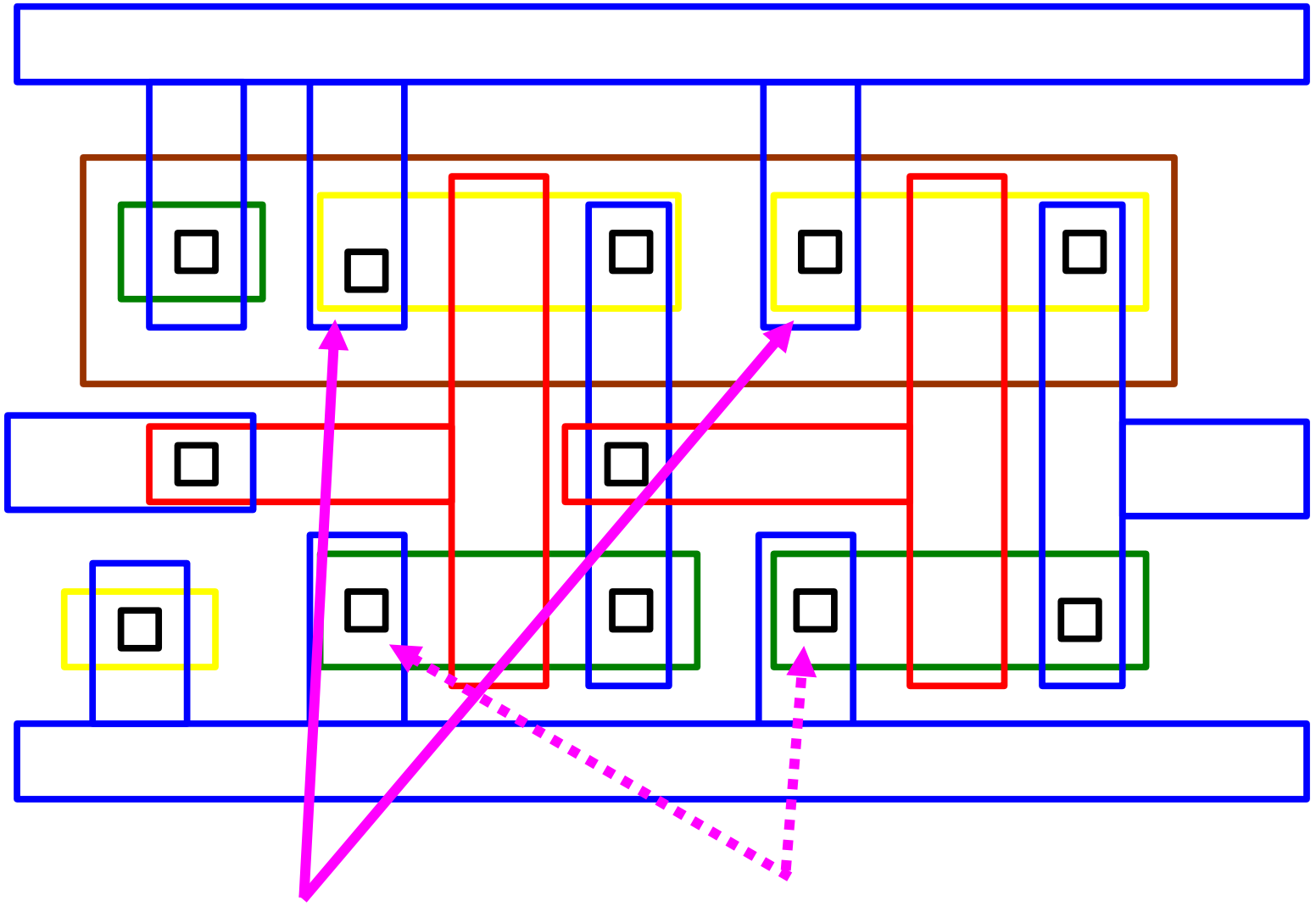
Design Rules (example)



Layout with shared p-well reduces area

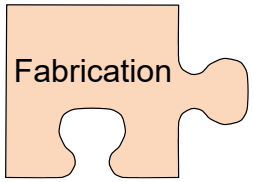
Review from Last Time

Design Rules (example)



Shared p-active can be combined to reduce area

Shared n-active can be combined to reduce area



Technology Files

- Design Rules

- Process Flow (Fabrication Technology)

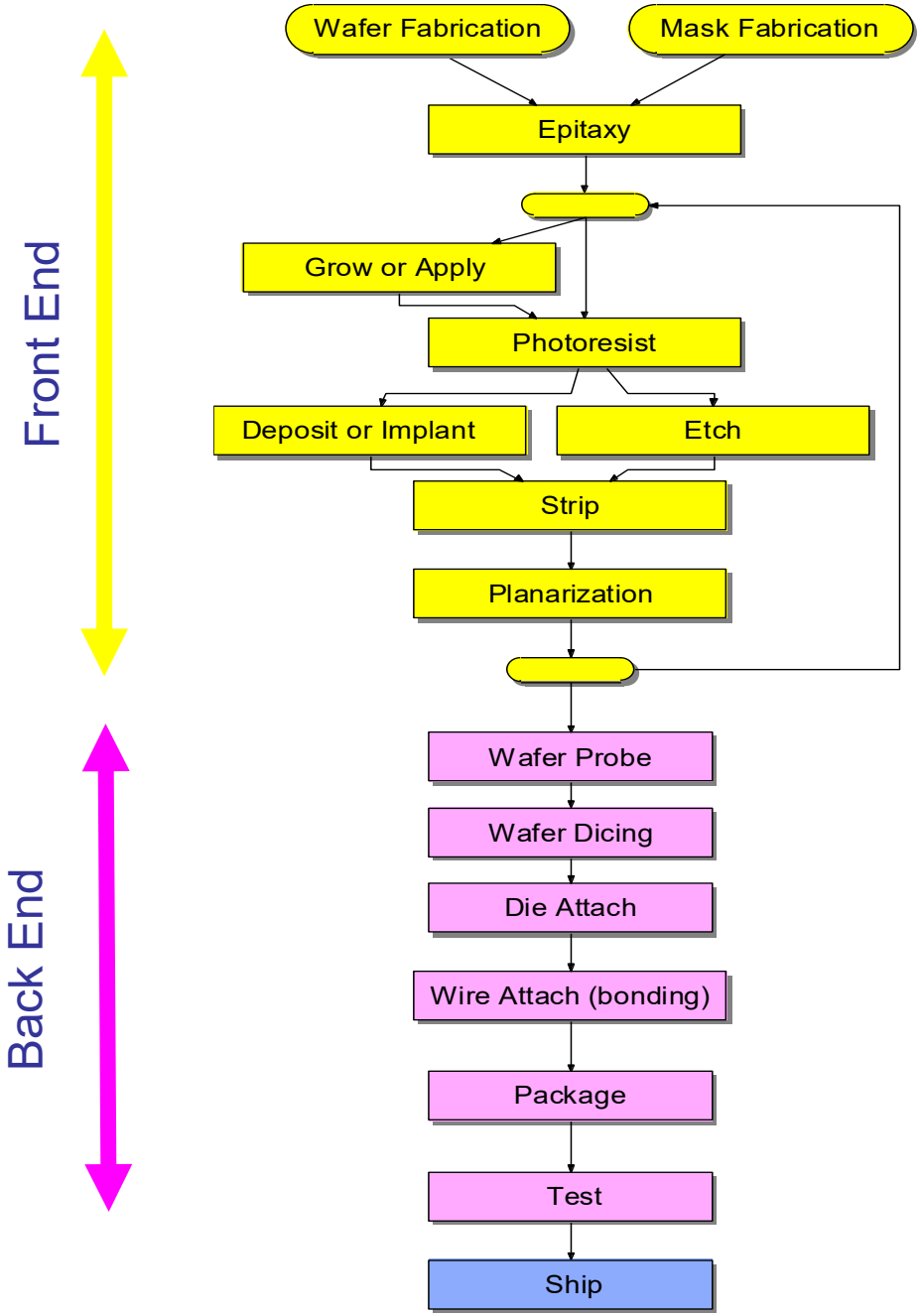
- Model Parameters (will discuss in substantially more detail after device operation and more advanced models are introduced)

IC Fabrication Technology

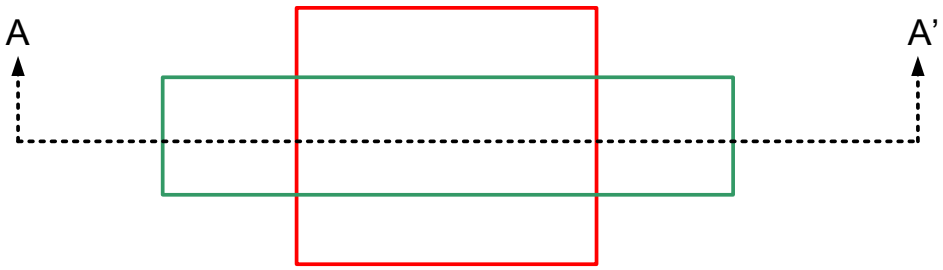
See Chapter 3 and a little of Chapter 1 of WH

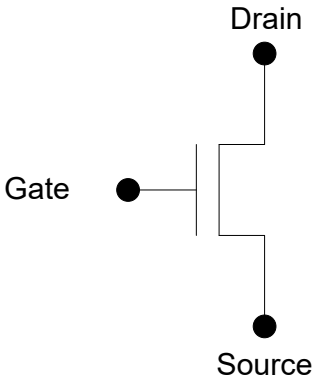
or Chapter 2 GAS for details

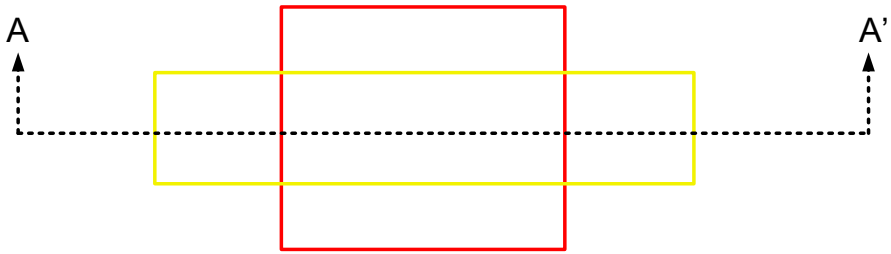
Generic Process Flow

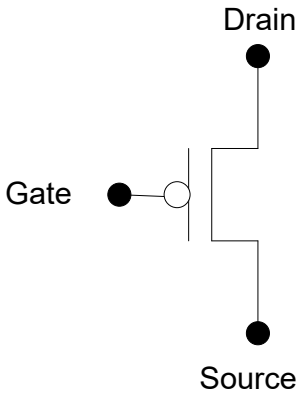


First a bit of background on transistor structure



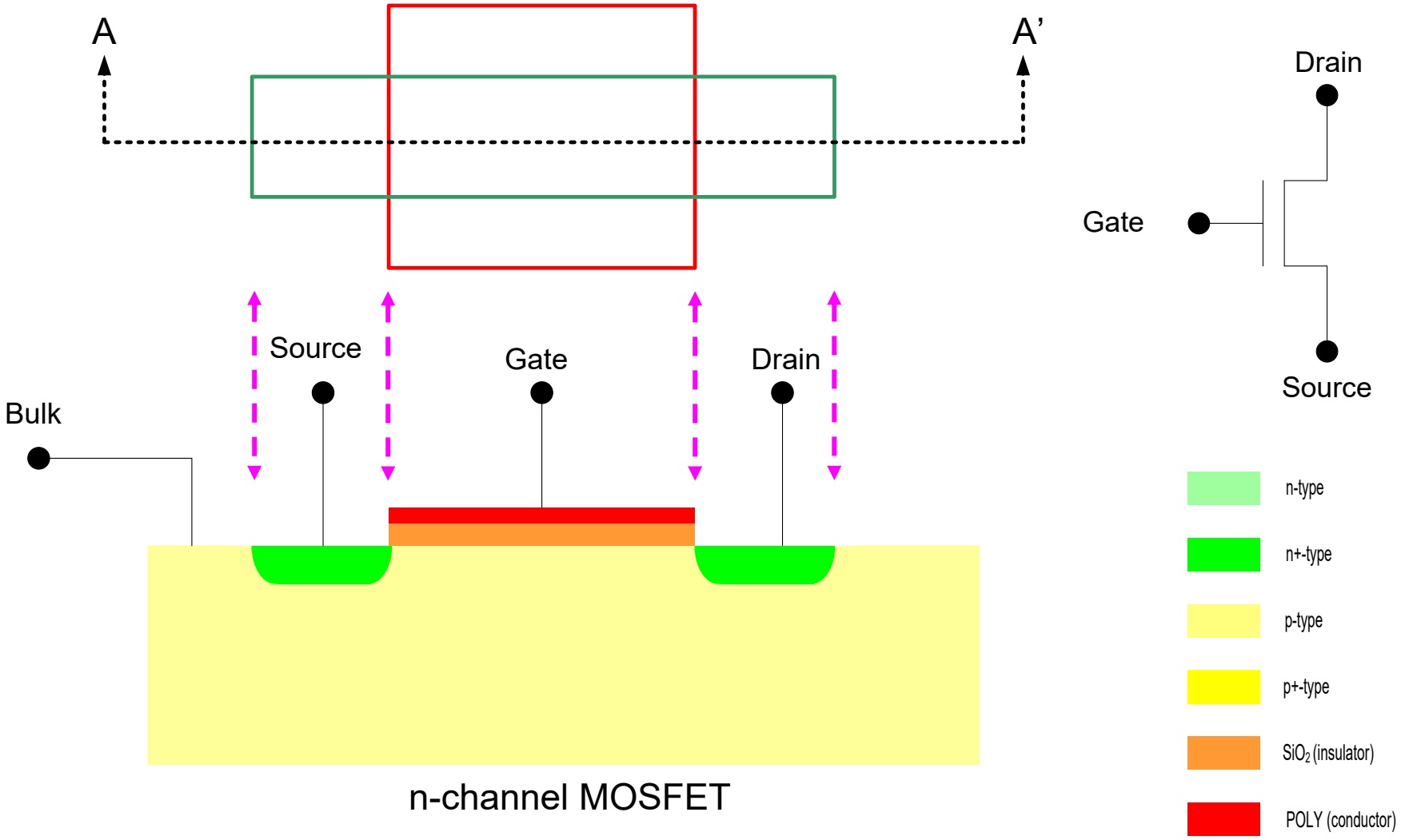






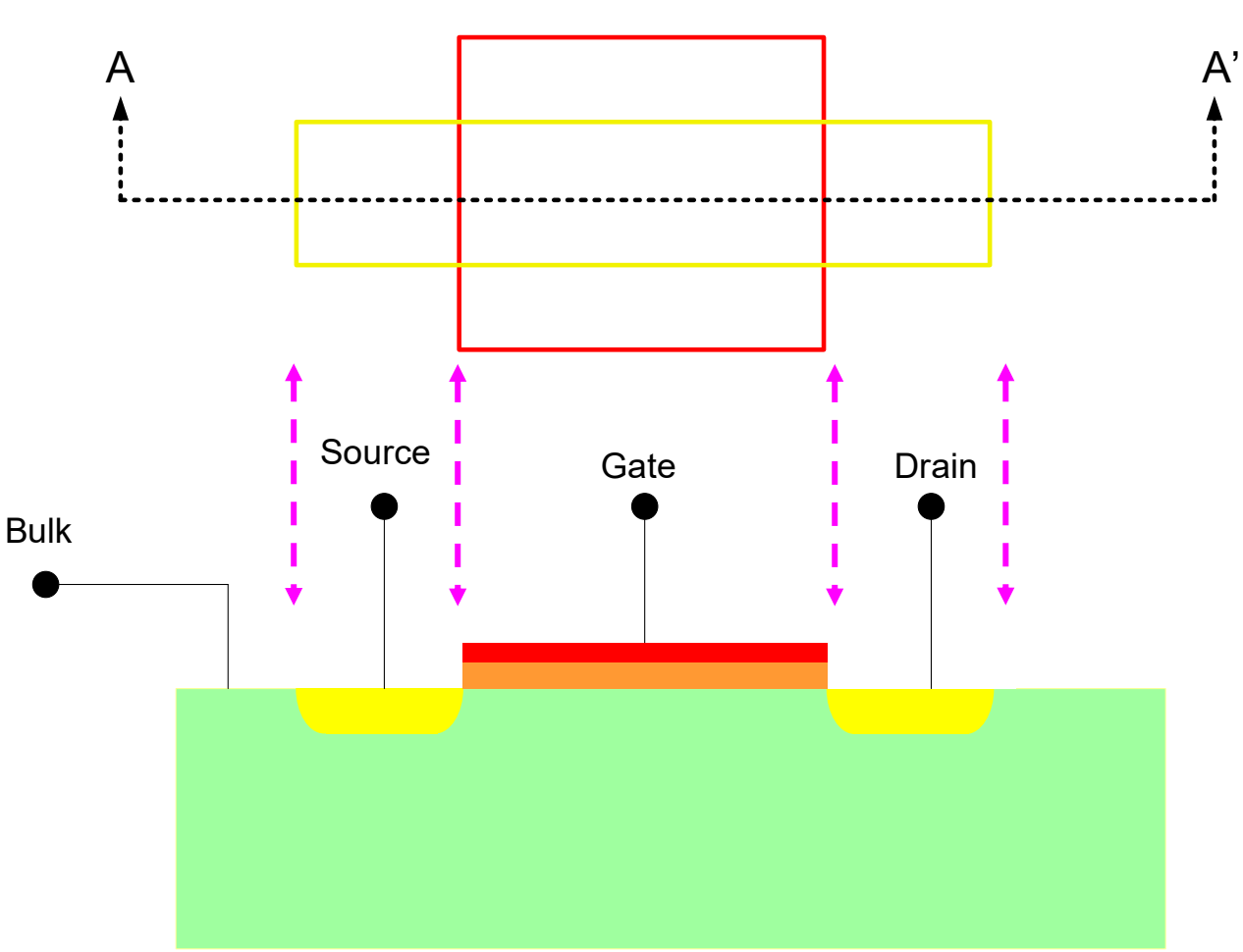
Recall

MOS Transistor

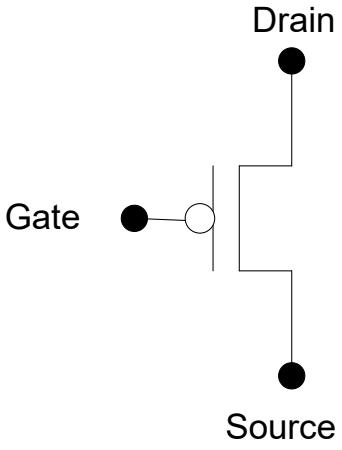


Review

MOS Transistor

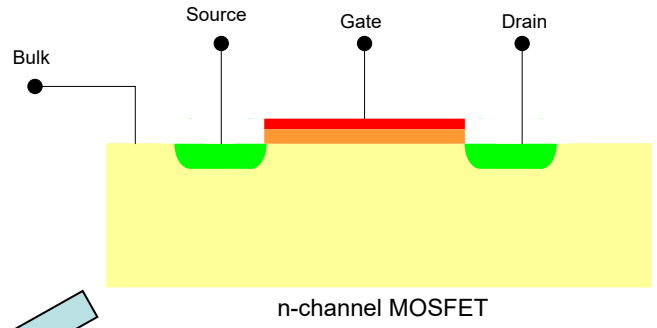


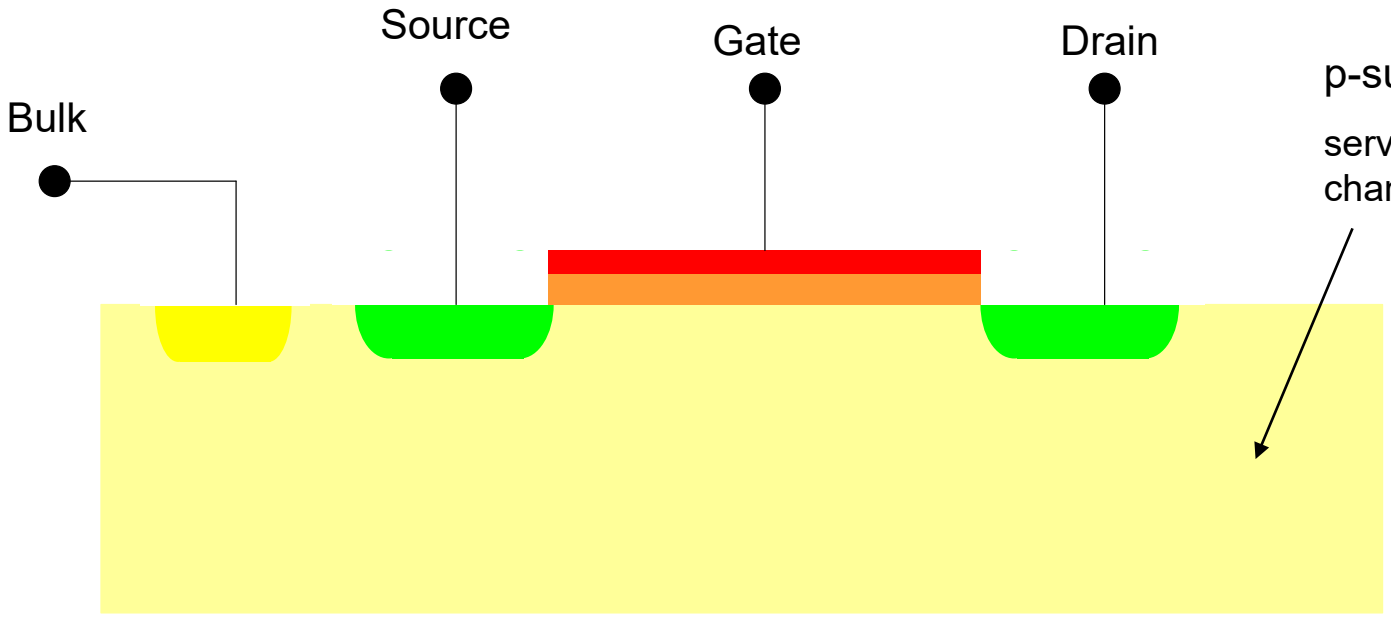
p-channel MOSFET



MOS Transistor

n-channel MOS transistor in Bulk CMOS n-well process with bulk contact

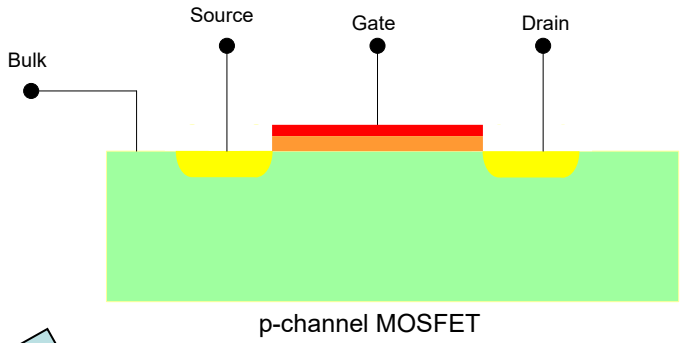


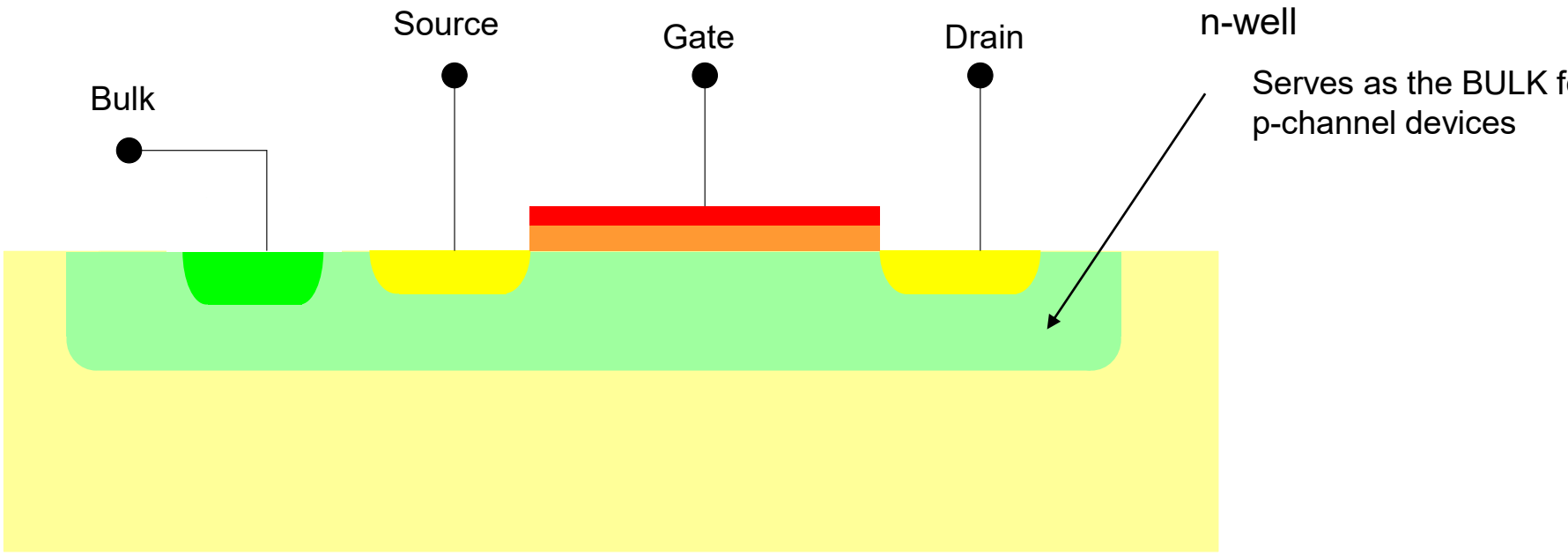


n-channel MOSFET

MOS Transistor

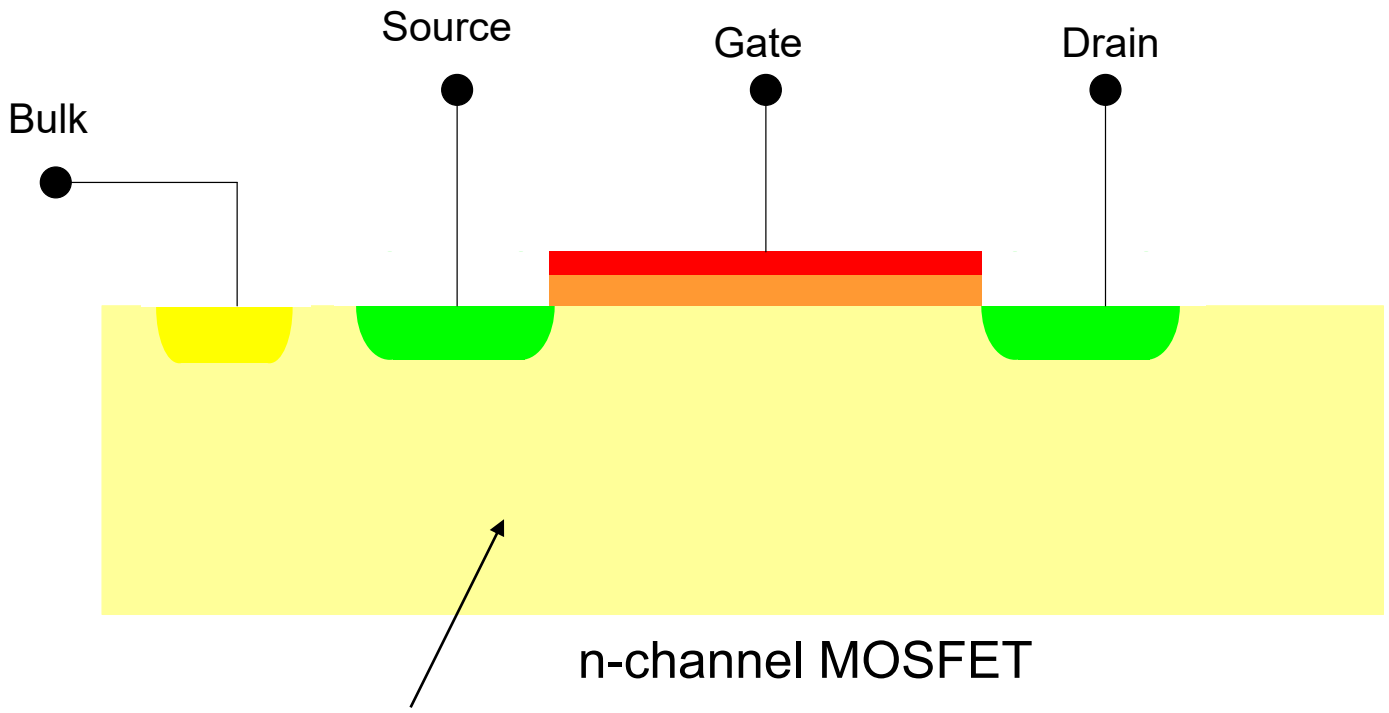
p-channel MOS transistor in
Bulk CMOS n-well process
with bulk contact and well (tub)





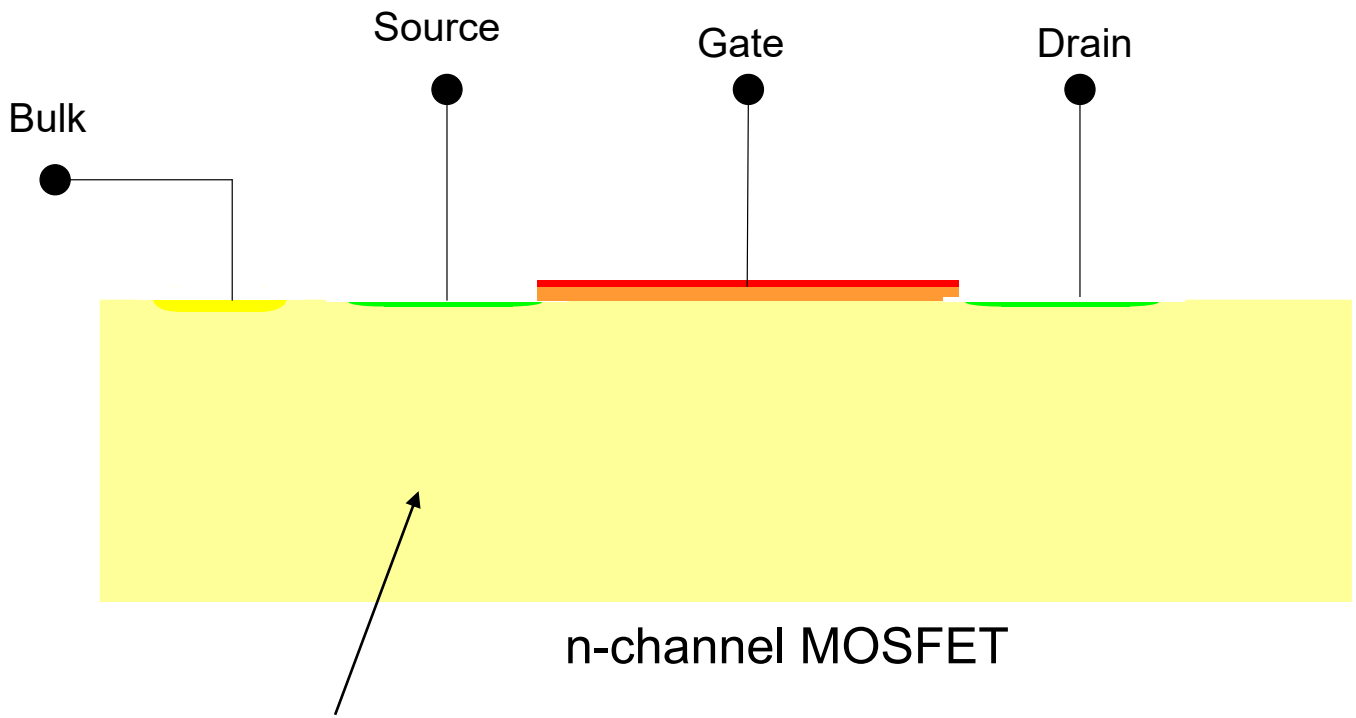
p-channel MOSFET

MOS Transistor



- Single-crystalline silicon
  - Serves as physical support member
  - Lightly doped
  - Vertical dimensions are not linearly depicted
  - Often termed the Bulk

MOS Transistor



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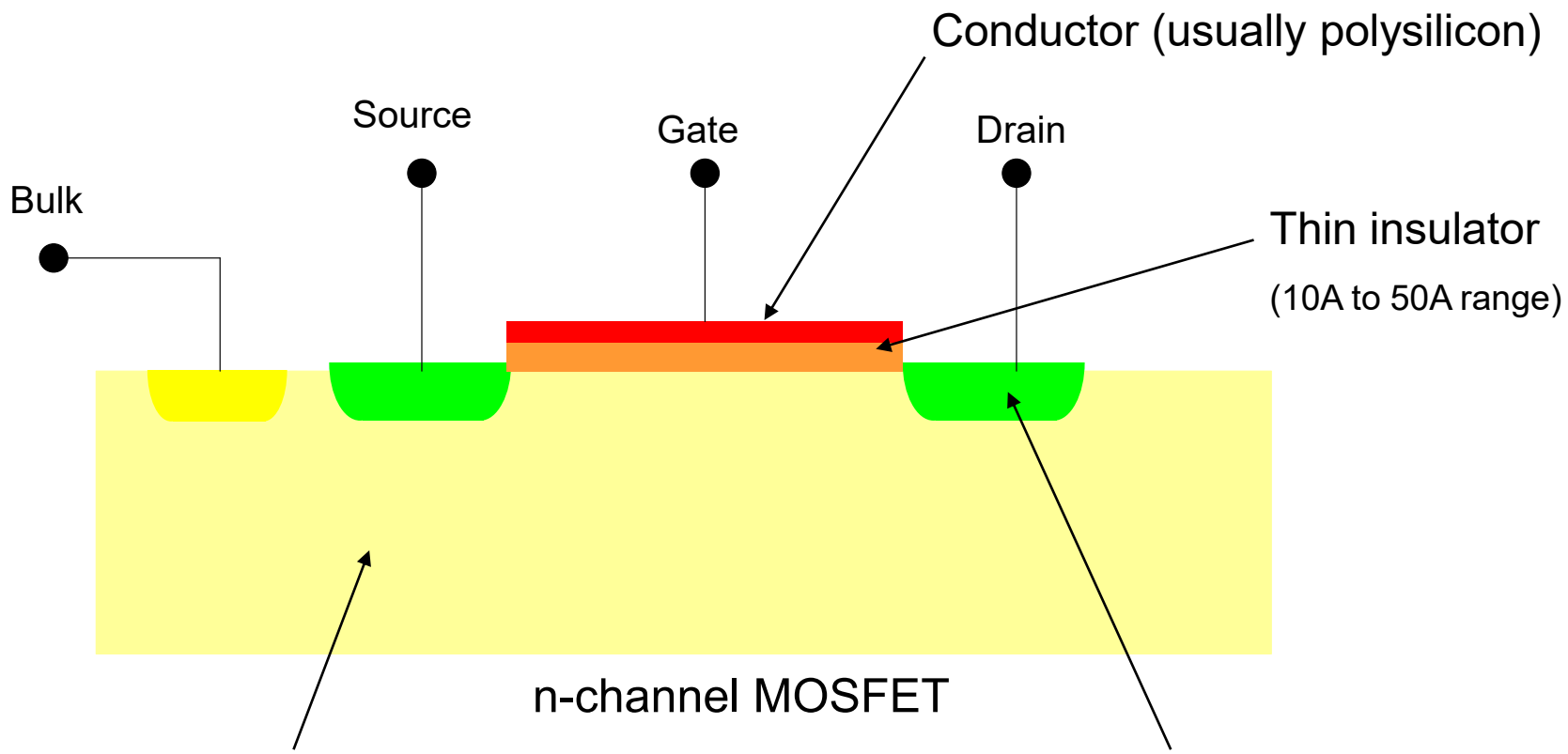
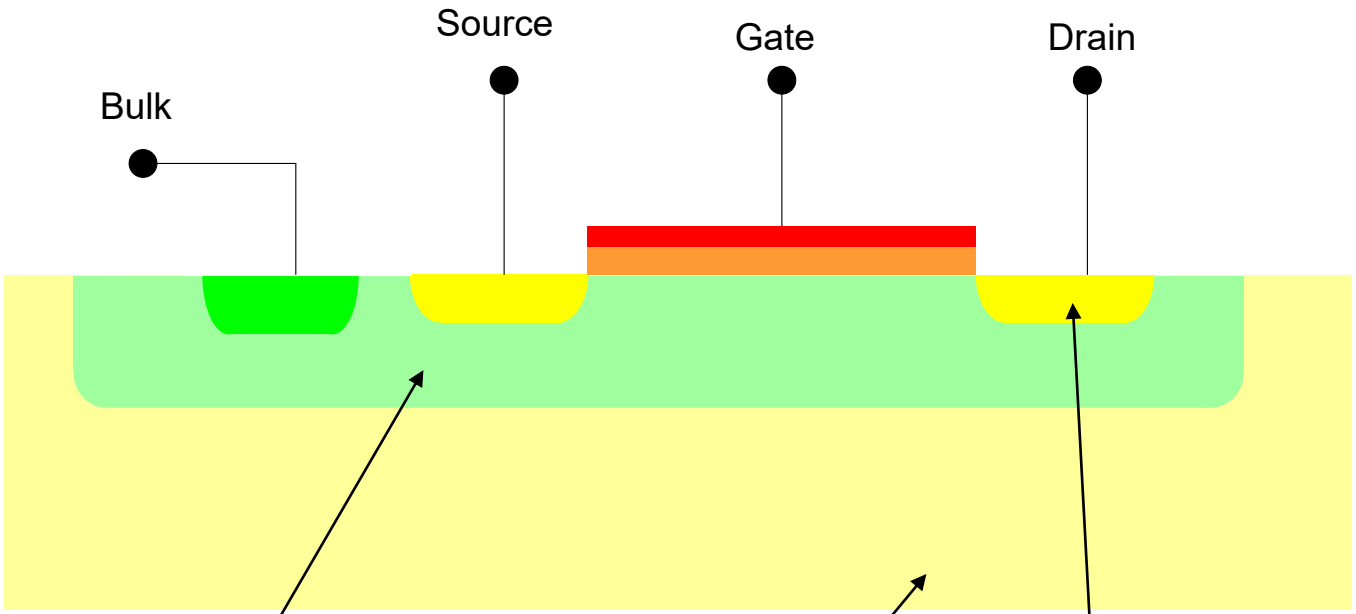
MOS Transistor



- Single-crystalline silicon
  - Serves as physical support member
  - Lightly doped (p-doping in the 10^{15}/cm^3 range, silicon in the 2.2×10^{22}/cm^3 range)
  - Vertical dimensions are not linearly depicted
  - Often termed the BULK

Dominant Doping Depicted – Generally Contain Prior Lower Density Dopants of Opposite Type

MOS Transistor



Lightly-doped n-type
($5x10^{16}/cm^3$ range)

More heavily-doped p-type
($10^{18}/cm^3$ range)

Lightly doped p-type
($10^{15}/cm^3$ range)

For Example: Drain Region Contains prior substrate p-dopants and n-type well dopants

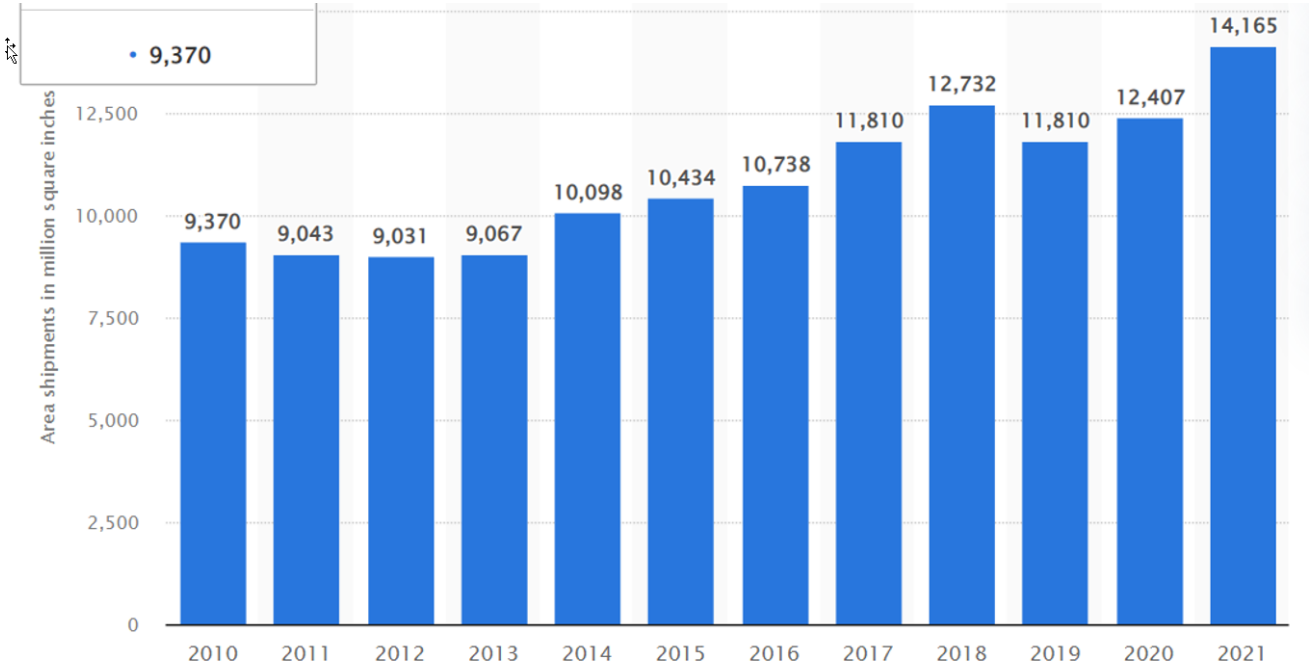
IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Ion Imlantation
- Etching
- Diffusion
- Oxidation
- Epitaxy
- Polysilicon
- Planarization
- Contacts, Interconnect and Metalization

Crystal Preparation

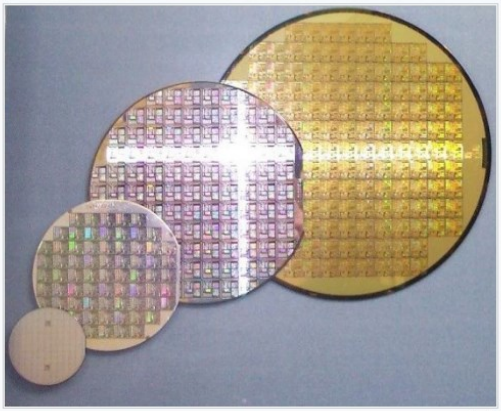
- Large crystal is grown (pulled)
  - 12 inches (300mm) in diameter and 1 to 2 m long
  - Sliced to 250μm to 500μm thick
    - Prefer to be much thinner but thickness needed for mechanical integrity
  - 4 to 8 cm/hr pull rate
  - T=1430 ^{o}C
- Crystal is sliced to form wafers
- Cost for 12” wafer around $200
- 5 companies provide 90% of worlds wafers
- Somewhere around 400,000 12in wafers/month

Silicon wafer area is a better metric



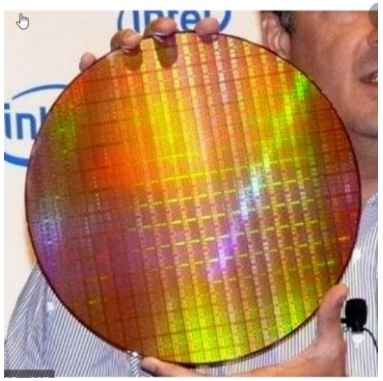
Crystal Preparation

Wafer size	Typical Thickness	Year Prodn [15]	Weight per wafer	100 mm2 [hide] (10 mm) Die per wafer
1-inch (25 mm)		1960		
2-inch (51 mm)	275 µm	1969		
3-inch (76 mm)	375 µm	1972		
4-inch (100 mm)	525 µm	1976	10 grams [19]	56
4.9 inch (125 mm)	625 µm	1981		
150 mm (5.9 inch, usually referred to as "6 inch")	675 µm	1983		
200 mm (7.9 inch, usually referred to as "8 inch")	725 µm.	1992	53 grams [19]	269
300 mm (11.8 inch, usually referred to as "12 inch")	775 µm	2002	125 grams[19]	640
450 mm (17.7 inch) (proposed).[20]	925 µm	future	342 grams [19]	1490
675-millimetre (26.6 in) (Theoretical).[21]	Unknown.	future		

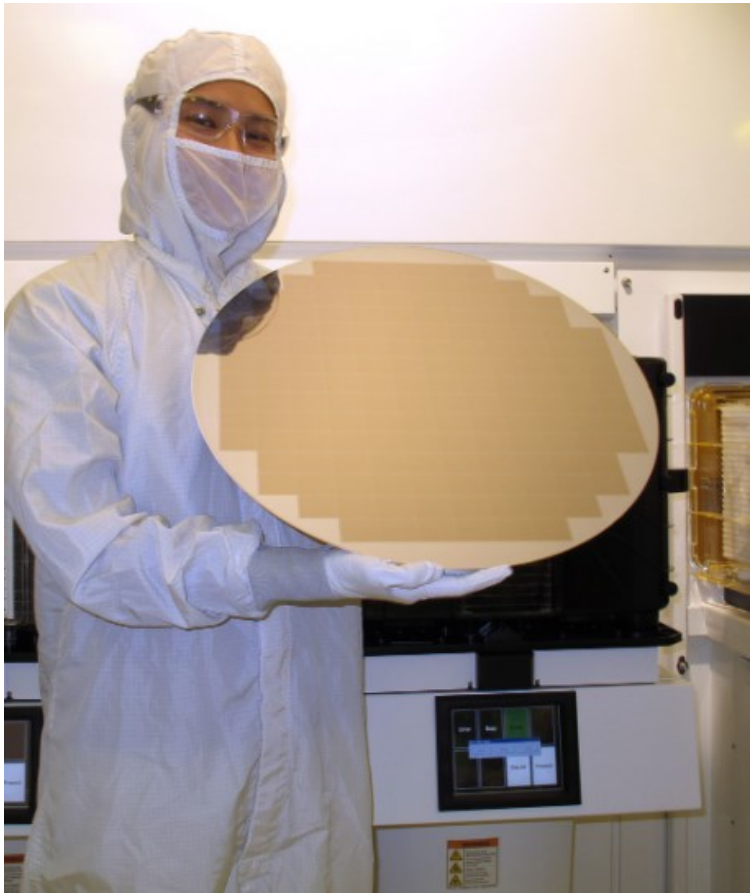


2-inch (51 mm), 4-inch (100 mm), 6-inch (150 mm), and 8-inch (200 mm) wafers

Crystal Preparation

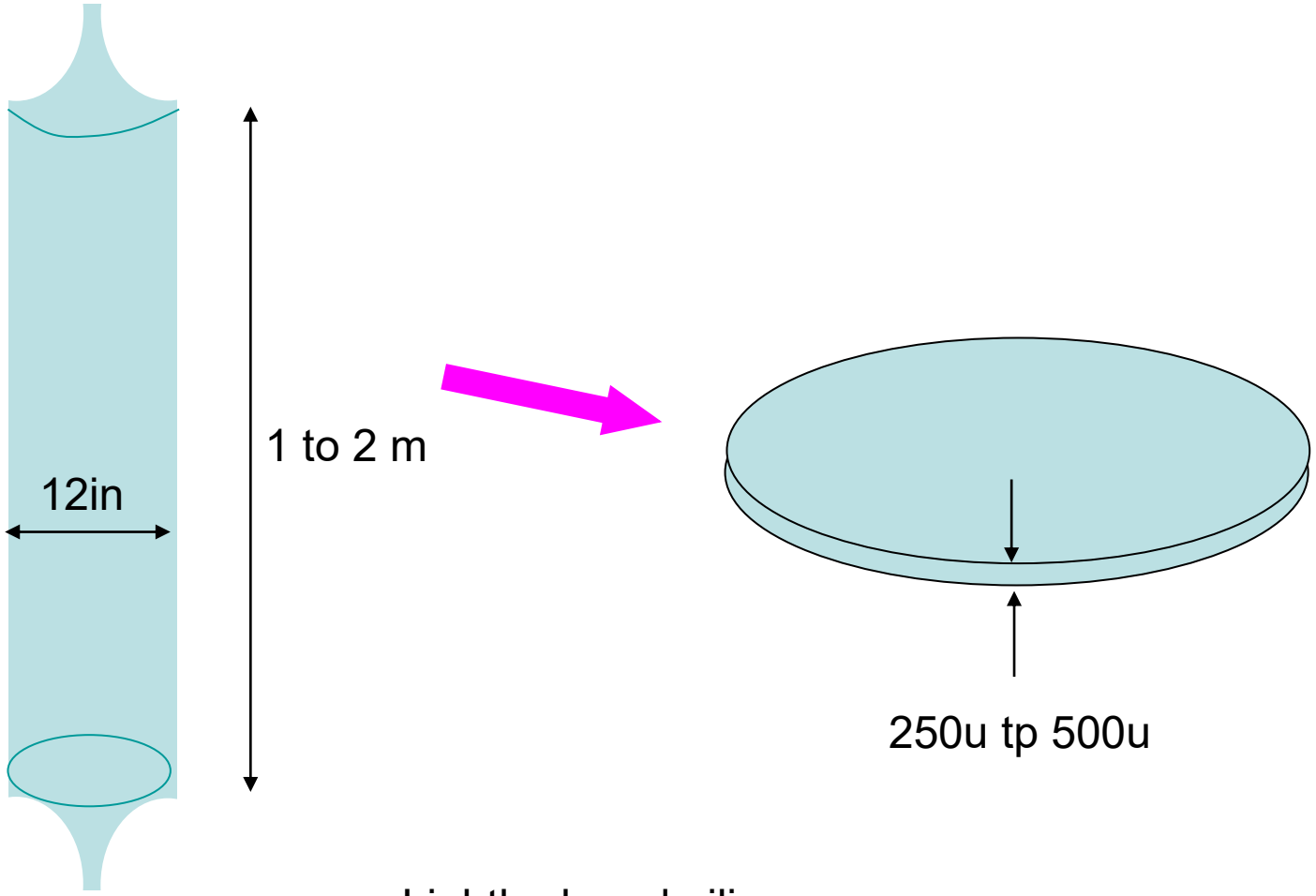


300mm wafer



450 mm wafer

Crystal Preparation



Some predict newer FABs to be at 450mm (18in) by 2020 but appears to be uncertain whether it will ever happen

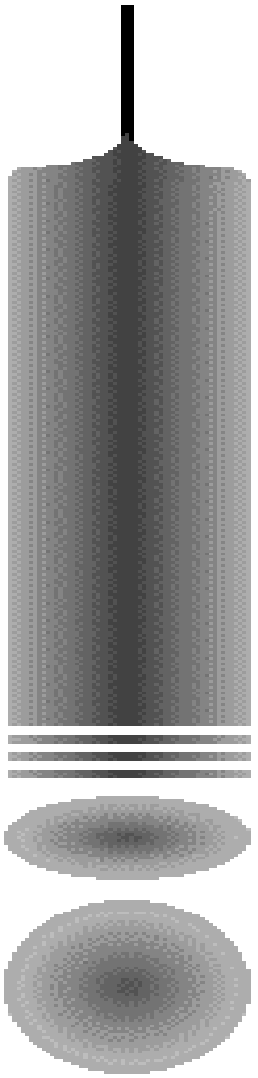
Lightly-doped silicon
Excellent crystalline structure

Crystal Preparation

Return on Investment Essential to Make Transition

200mm (8”) and 300mm (12”) are dominant in production today

Crystal Preparation

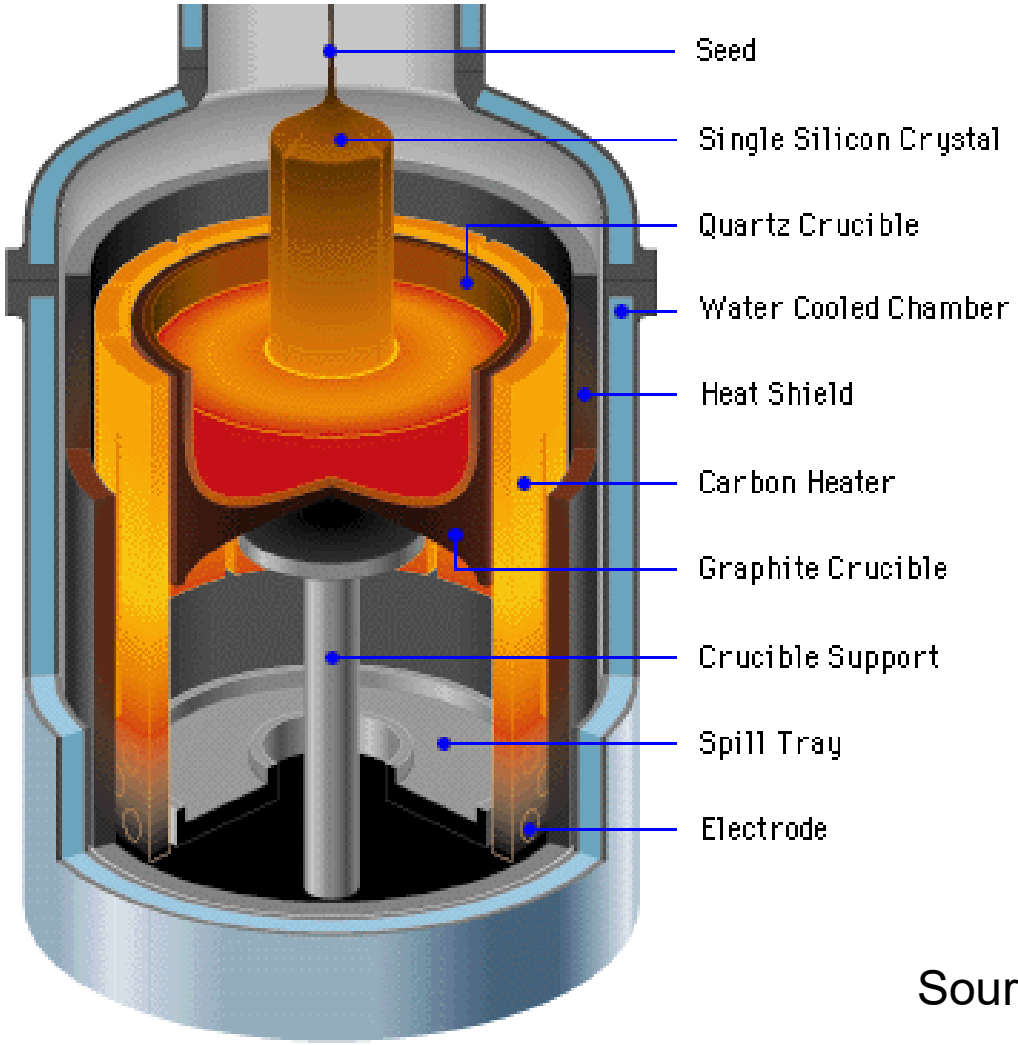


From www.infras.com

Crystal Preparation

Source: WEB

Crystal Preparation



Source: WEB

Crystal Preparation

Source: WEB

Crystal Preparation

A section of 300mm ingot is loaded into a wiresaw

Source: WEB

Crystal Preparation

Source: WEB

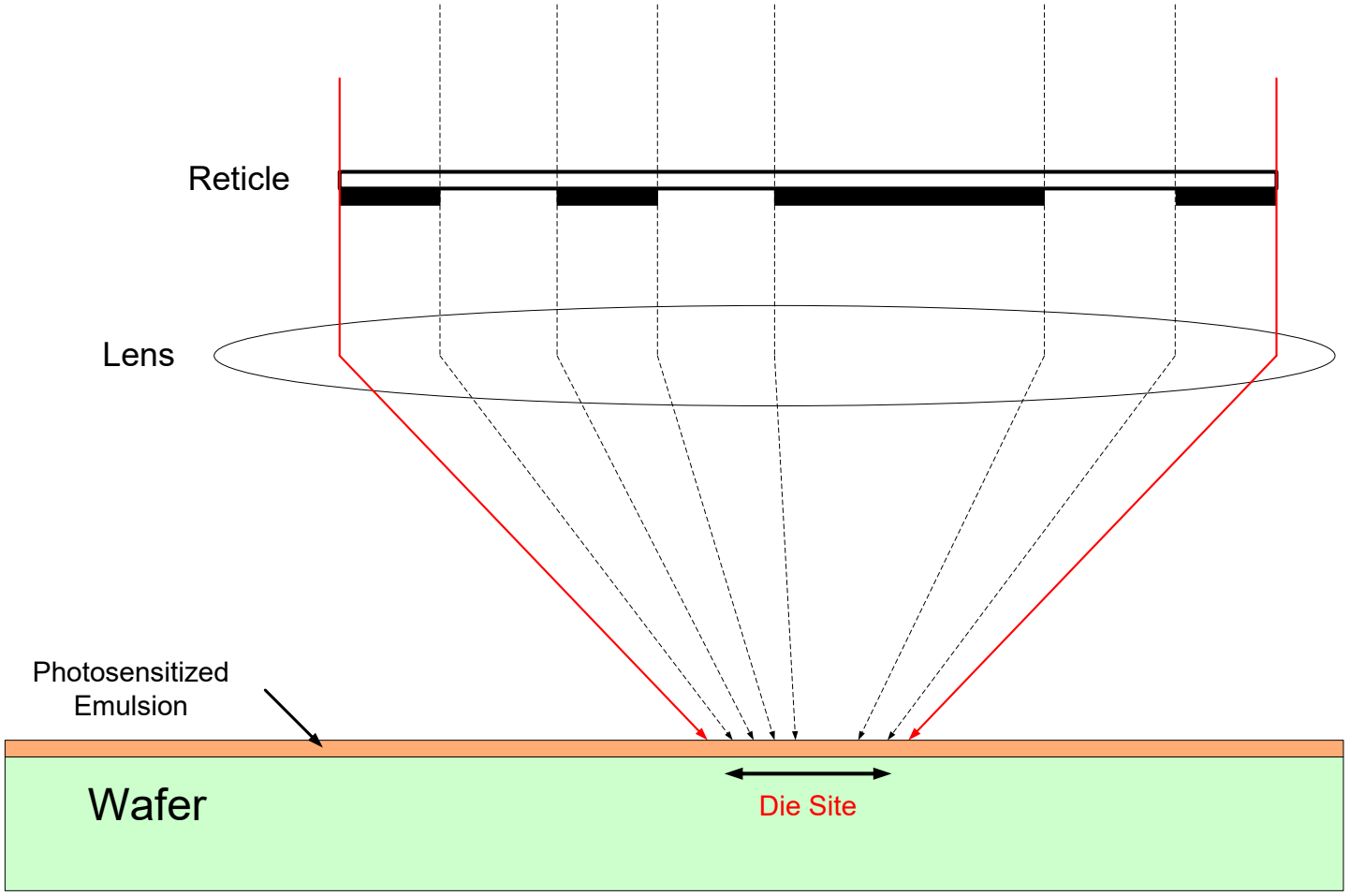
IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Ion Implantation
- Etching
- Diffusion
- Oxidation
- Epitaxy
- Polysilicon
- Planarization
- Contacts, Interconnect and Metalization

Masking

- Use masks or reticles to define features on a wafer
  - Masks same size as wafer
  - Reticles used for projection
  - Reticle much smaller (but often termed mask)
  - Reticles often of quartz with chrome
  - Quality of reticle throughout life of use is critical
  - Single IC may require 20 or more reticles
  - Cost of “mask set” now exceeds $1million for state of the art processes
  - Average usage 500 to 1500 times
  - Mask costs exceeding 50% of total fabrication costs in sub 100nm processes
  - Serve same purpose as a negative (or positive) in a photographic process
  - Usually use 4X optical reduction - exposure area approx. 860mm^2
    (now through 2022 ITRS 2007 litho, Table LITH3a)

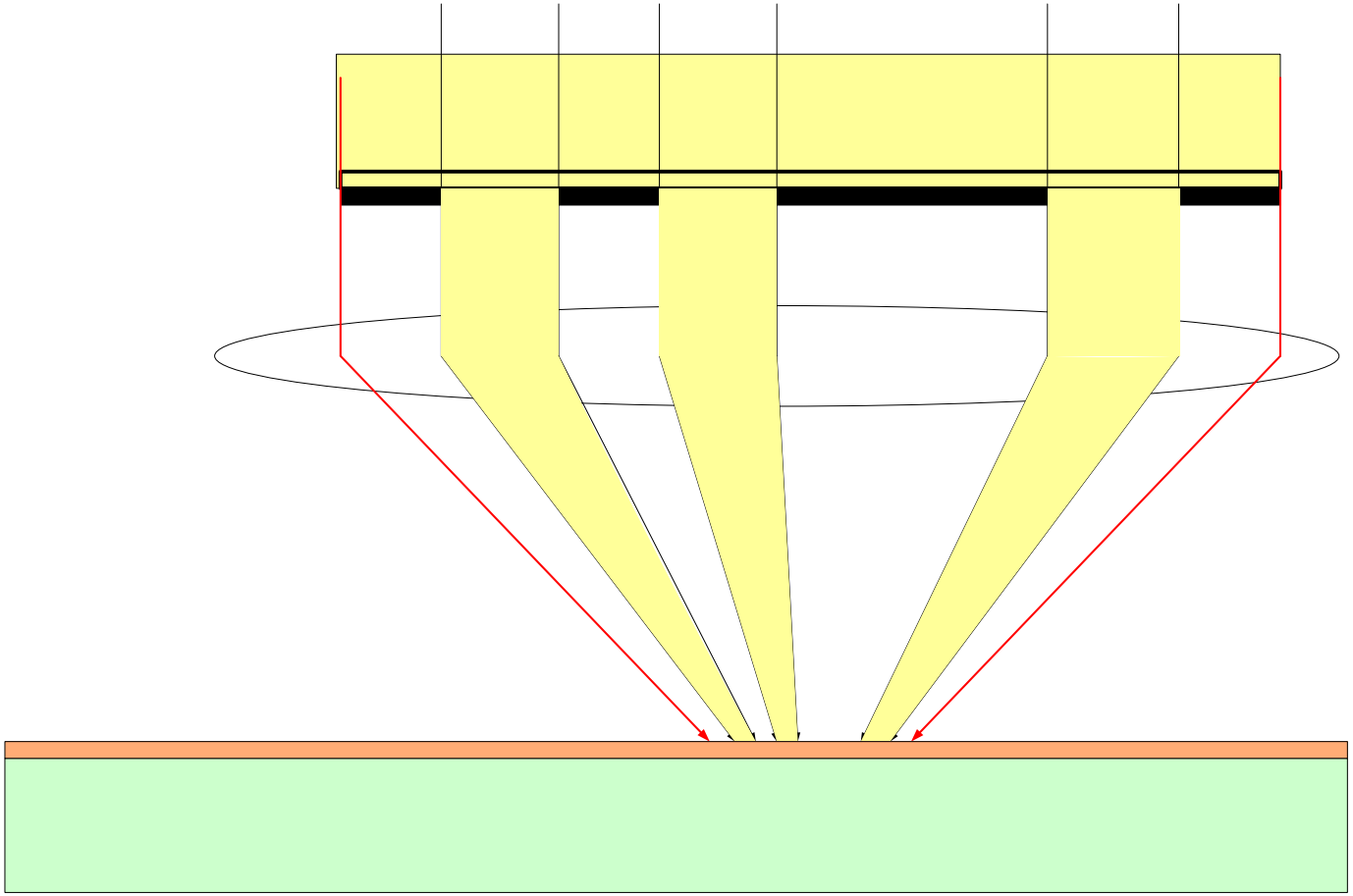
Masking



Step and Repeat (stepper) used to image across wafer

Masking

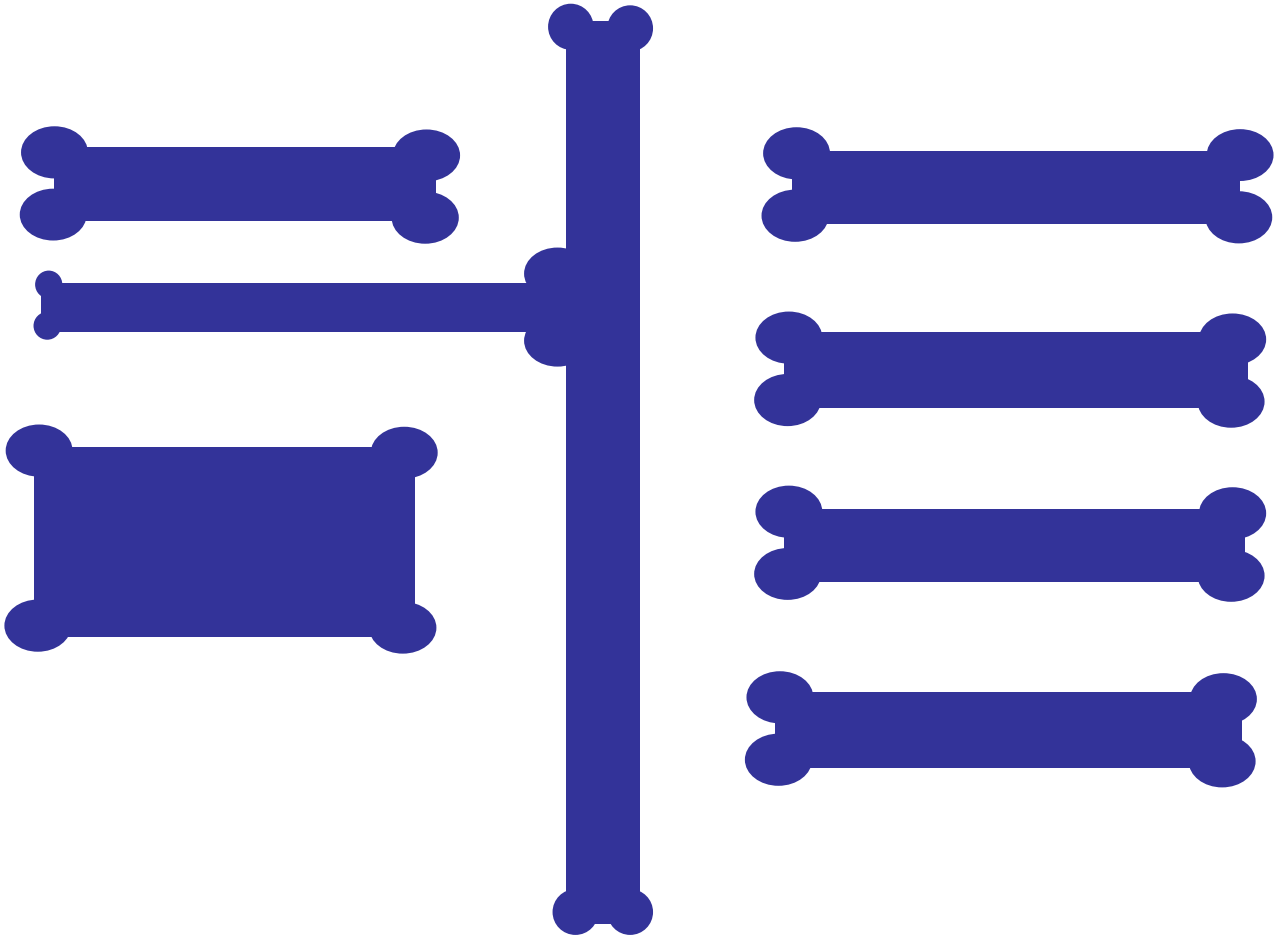
Exposure through reticle



Masking

Mask Features

Masking



Mask Features Intentionally Distorted to Compensated For Wavelength Limitations in Small Features

IC Fabrication Technology

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Photolithographic Process

- Photoresist
  - Viscous Liquid
  - Uniform Application Critical (spinner)
  - Baked to harden
  - Approx 1u thick
  - Non-Selective
  - Types
    - Negative – unexposed material removed when developed
    - Positive-exposed material removed when developed
    - Thickness about 450nm in 90nm process (ITRS 2007 Litho)
- Exposure
  - Projection through reticle with stepper (scanners becoming popular)
  - Alignment is critical !!
  - E-Bean Exposures
    - Eliminate need fro reticle
    - Capacity very small

Stepper: Optics fixed, wafer steps in fixed increments
Scanner: Wafer steps in fixed increments and during exposure both optics and wafer are moved to increase effective reticle size

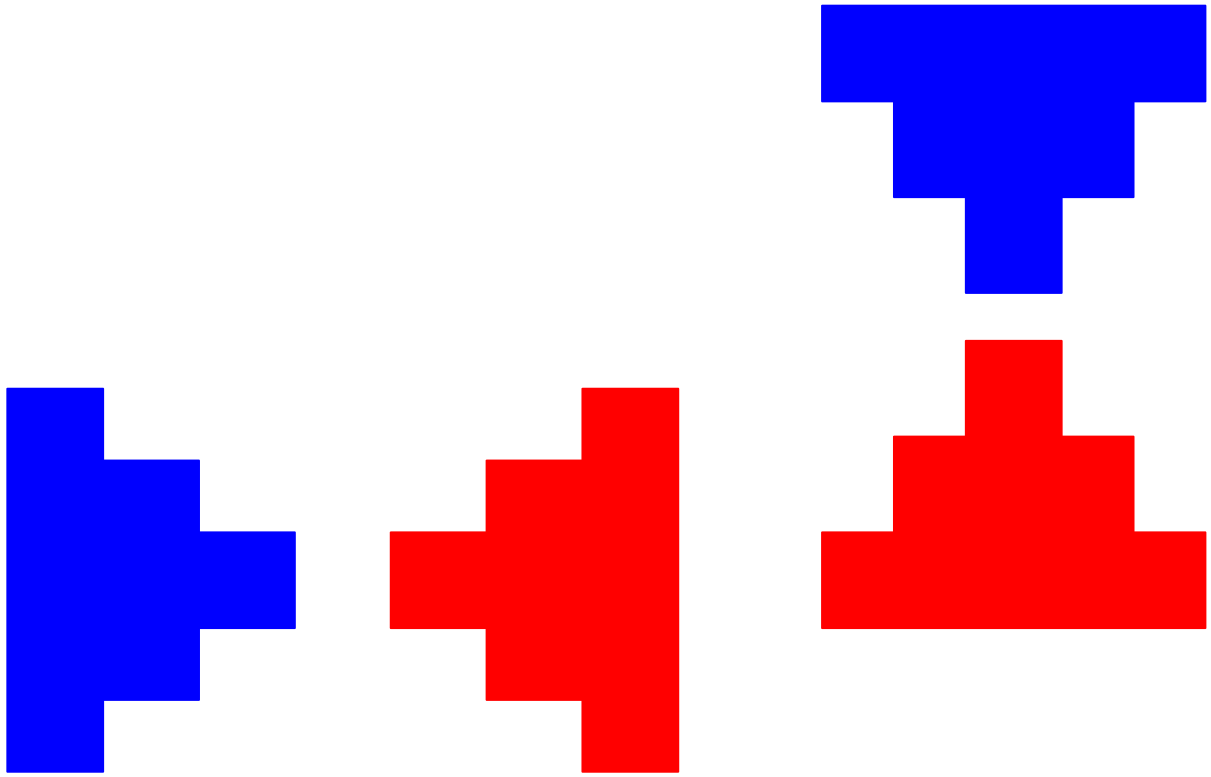
Steppers

Stepper costs in the $10M range with thru-put of around 100 wafers/hour

Steppers

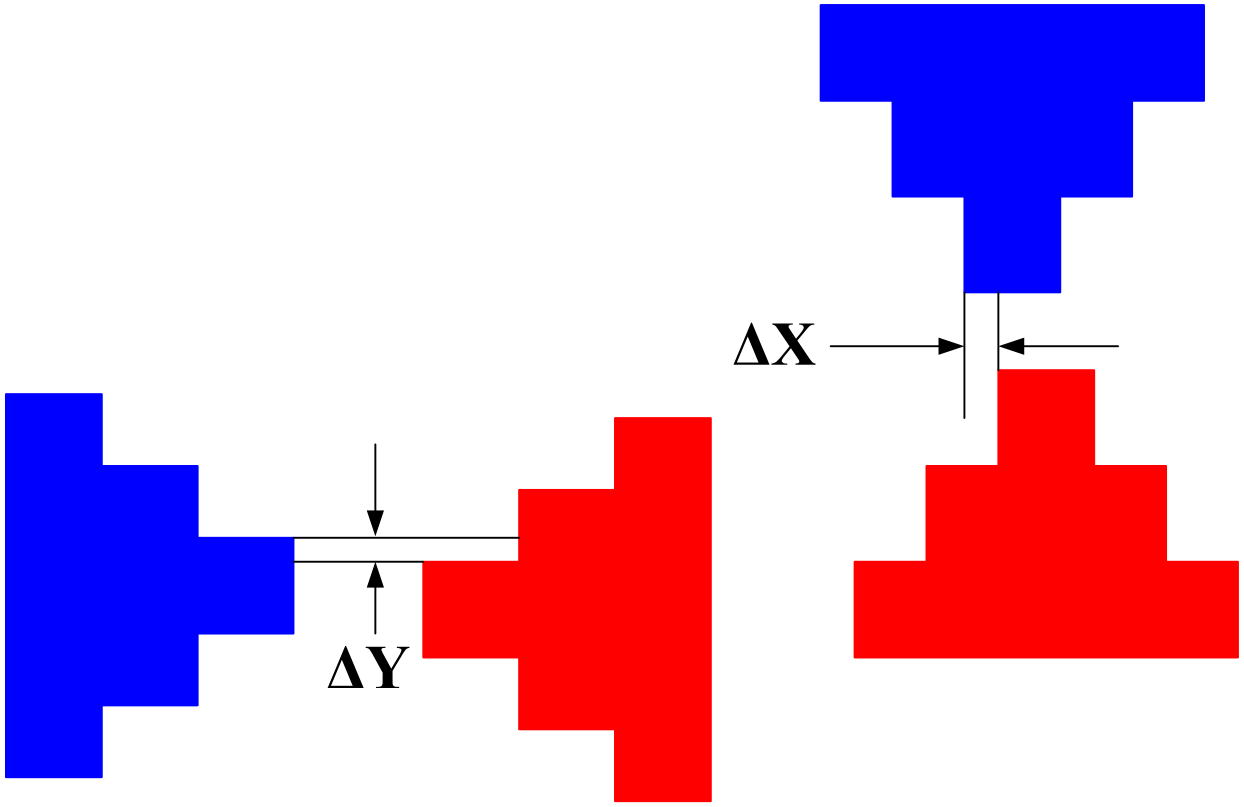
Mask Alignment

Correctly Aligned



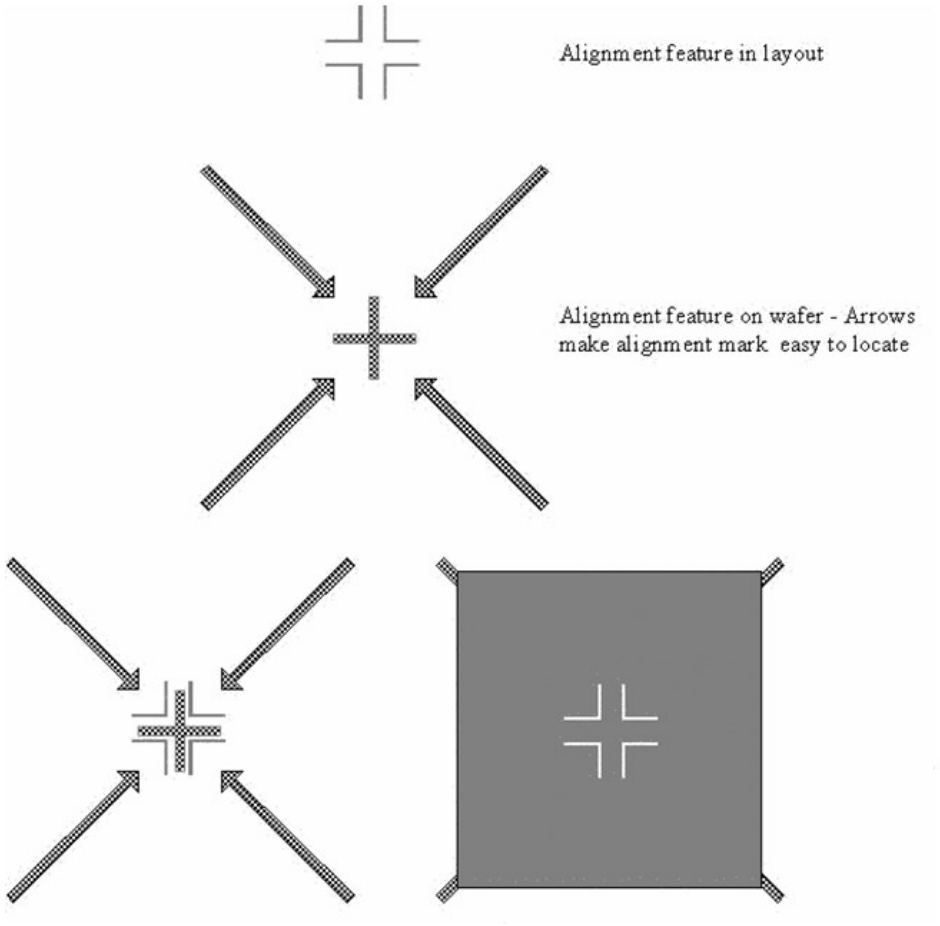
Mask Alignment

Alignment Errors



Mask Alignment

Other alignment marks (http://www.mems-exchange.org/users/masks/intro-equipment.html)



Stay Safe and Stay Healthy !

End of Lecture 9

IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Ion Implantation
- Etching
- Diffusion
- Oxidation
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Deposition

- Application of something to the surface of the silicon wafer or substrate
  - Layers 15A to 20u thick
- Methods
  - Physical Vapor Deposition (nonselective)
    - Evaporation/Condensation
    - Sputtering (better host integrity)
  - Chemical Vapor Deposition (nonselective)
    - Reaction of 2 or more gases with solid precipitate
    - Reduction by heating creates solid precipitate (pyrolytic)
  - Screening (selective)
    - For thick films
    - Low Tech, not widely used today

Deposition

Example: Chemical Vapor Deposition

Silane (SiH_4) is a gas (toxic and spontaneously combustible in air) at room temperature but breaks down into Si and H_2 above 400^{o}C so can be used to deposit Si.

$$S_iH_4 \rightarrow S_i + 2H_2$$

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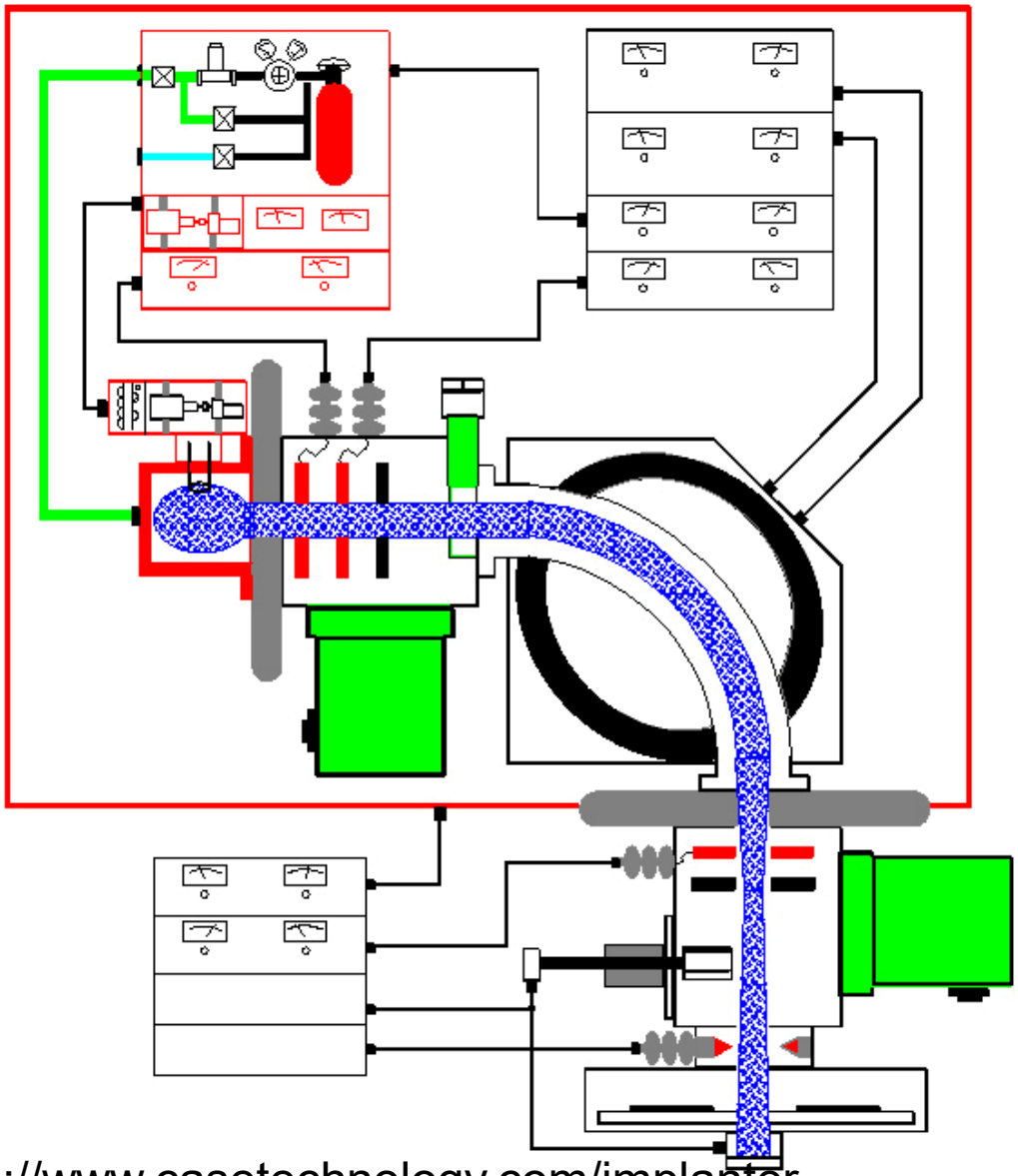
Ion Implantation

Application of impurities into the surface of the silicon wafer or substrate

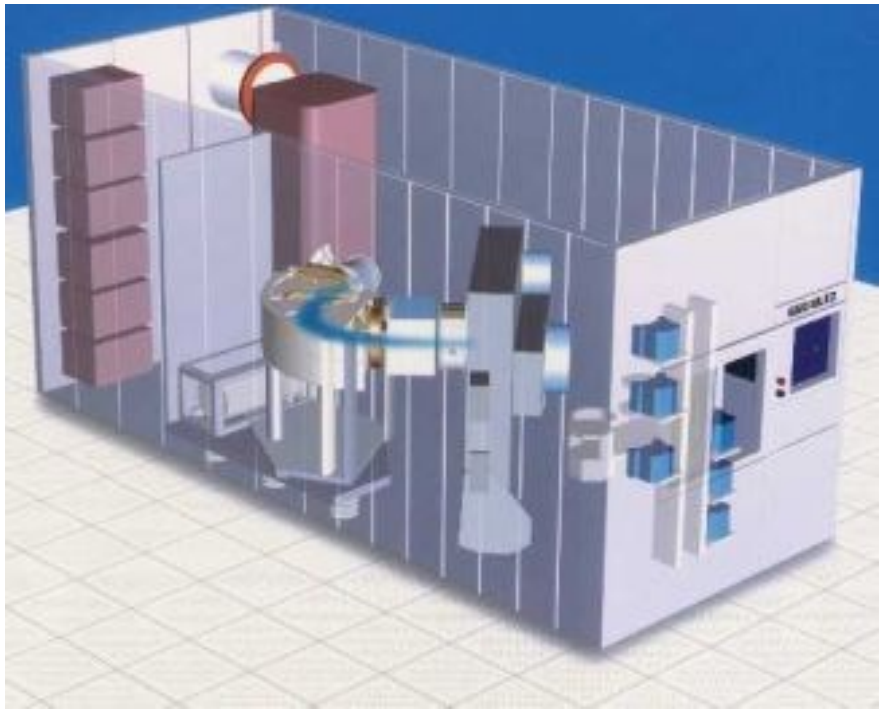
- Individual atoms are first ionized (so they can be accelerated)
- Impinge on the surface and burry themselves into the upper layers
- Often very shallow but with high enough energy can go modestly deep
- Causes damage to target on impact
- Annealing heals most of the damage
- Very precise control of impurity numbers is possible
- Very high energy required
- High-end implanters considered key technology for national security

Ion Implantation Process



From http://www.casetechnology.com/implanter

Ion Implanter



From http://www.casetechnology.com/implanter

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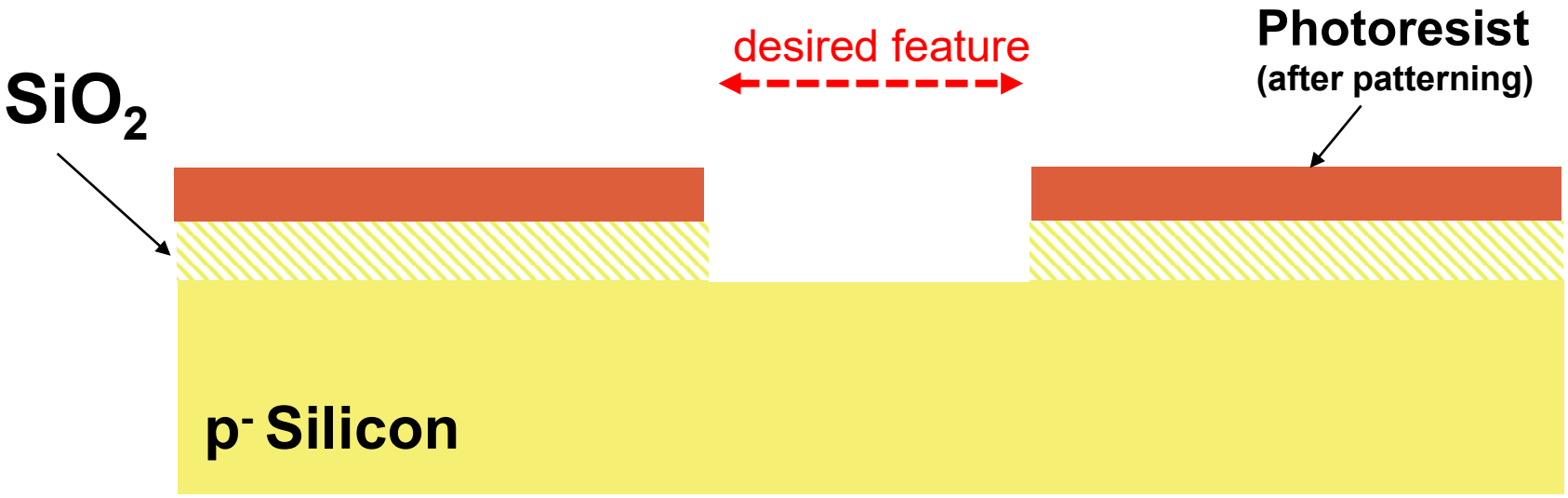
Etching

Selective Removal of Unwanted Materials

- Wet Etch
  - Inexpensive but under-cutting a problem
- Dry Etch
  - Often termed ion etch or plasma etch

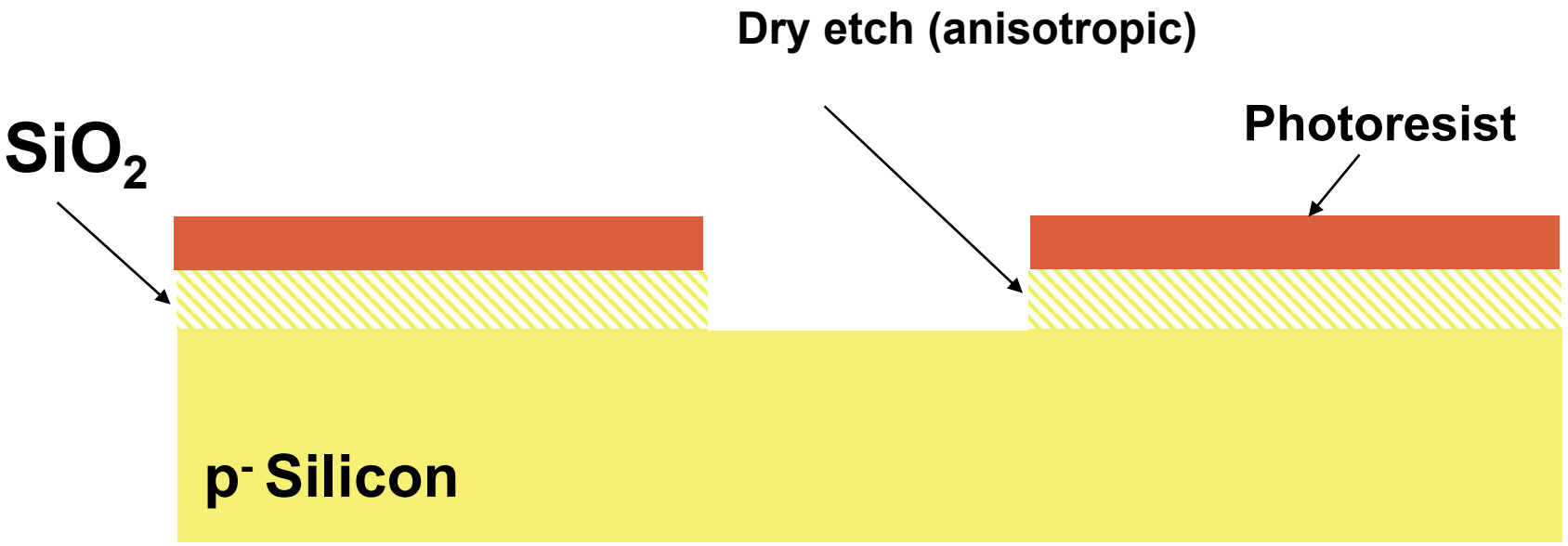
Etching



Desired Physical Features

Note: Vertical Dimensions in silicon generally orders of magnitude smaller than lateral dimensions so different vertical and lateral scales will be used in this discussion. Vertical dimensions of photoresist which is applied on top of wafer is about ½ order of magnitude larger than lateral dimensions

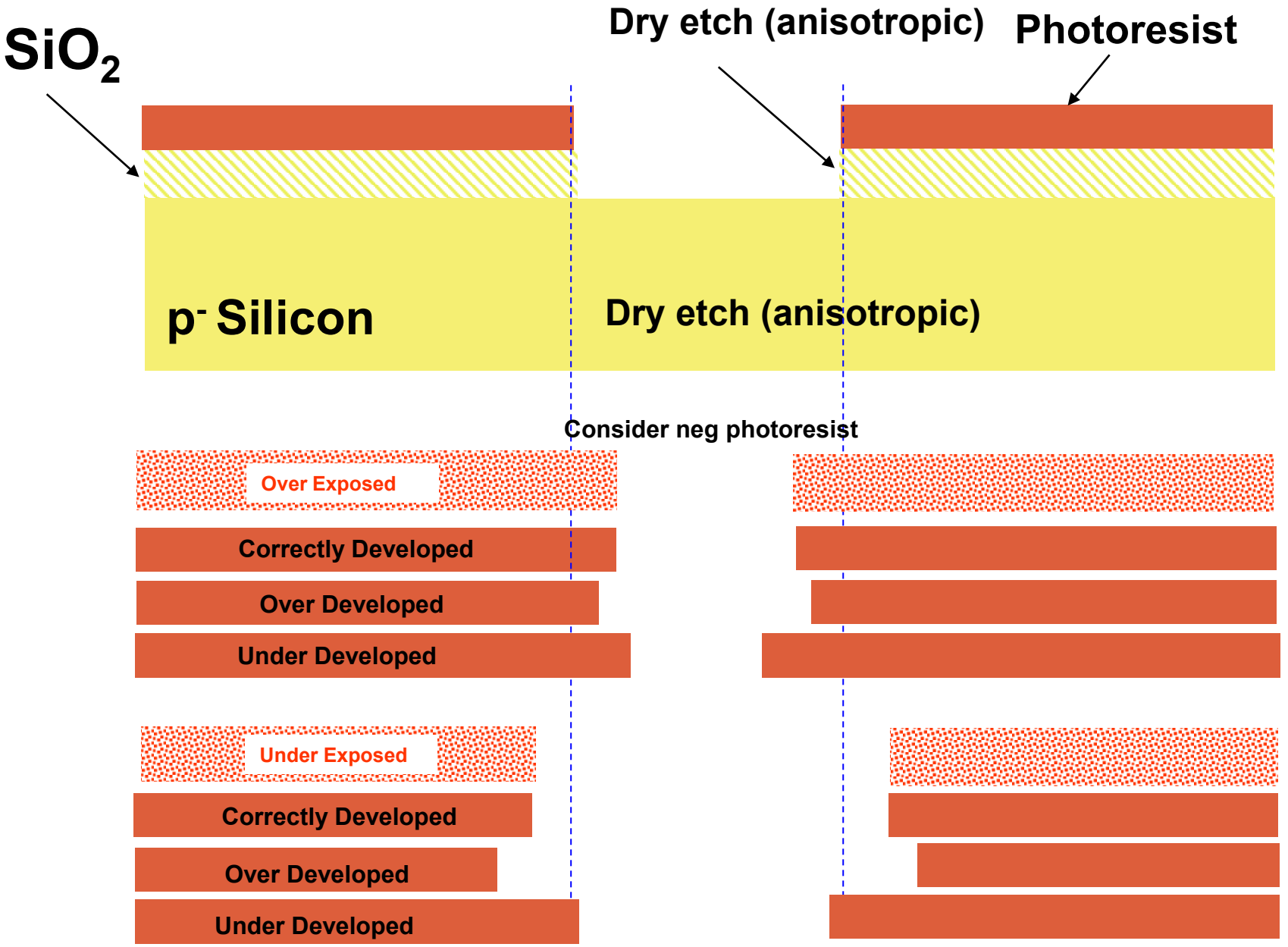
Etching



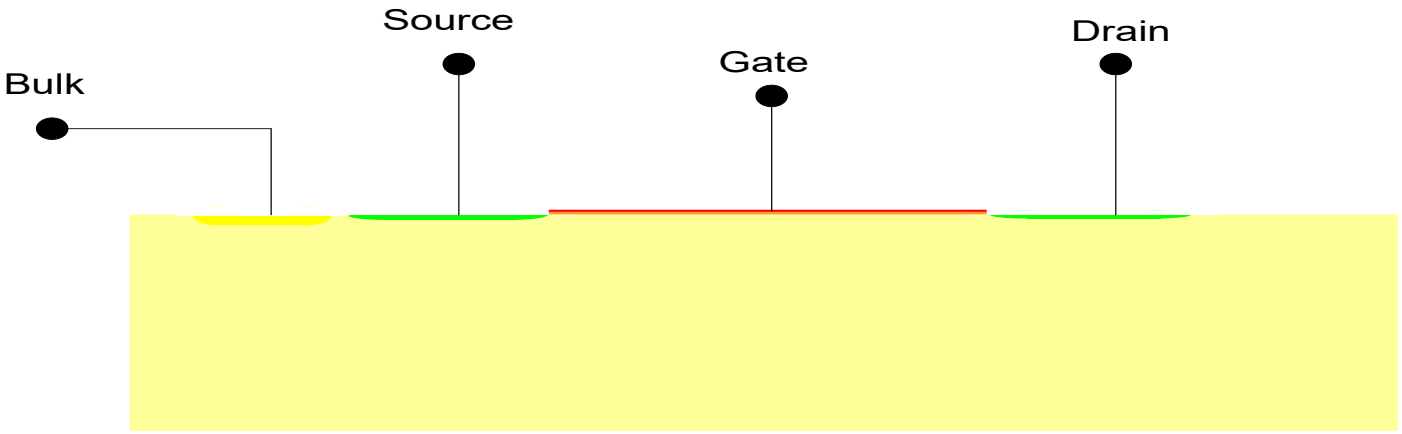
Desired Physical Features

Dry Etch can provide very well-defined and nearly vertical edges (relative to photoresist paterning)

Etching (limited by photolitghographic process)



Lateral Relative to Vertical Dimensions

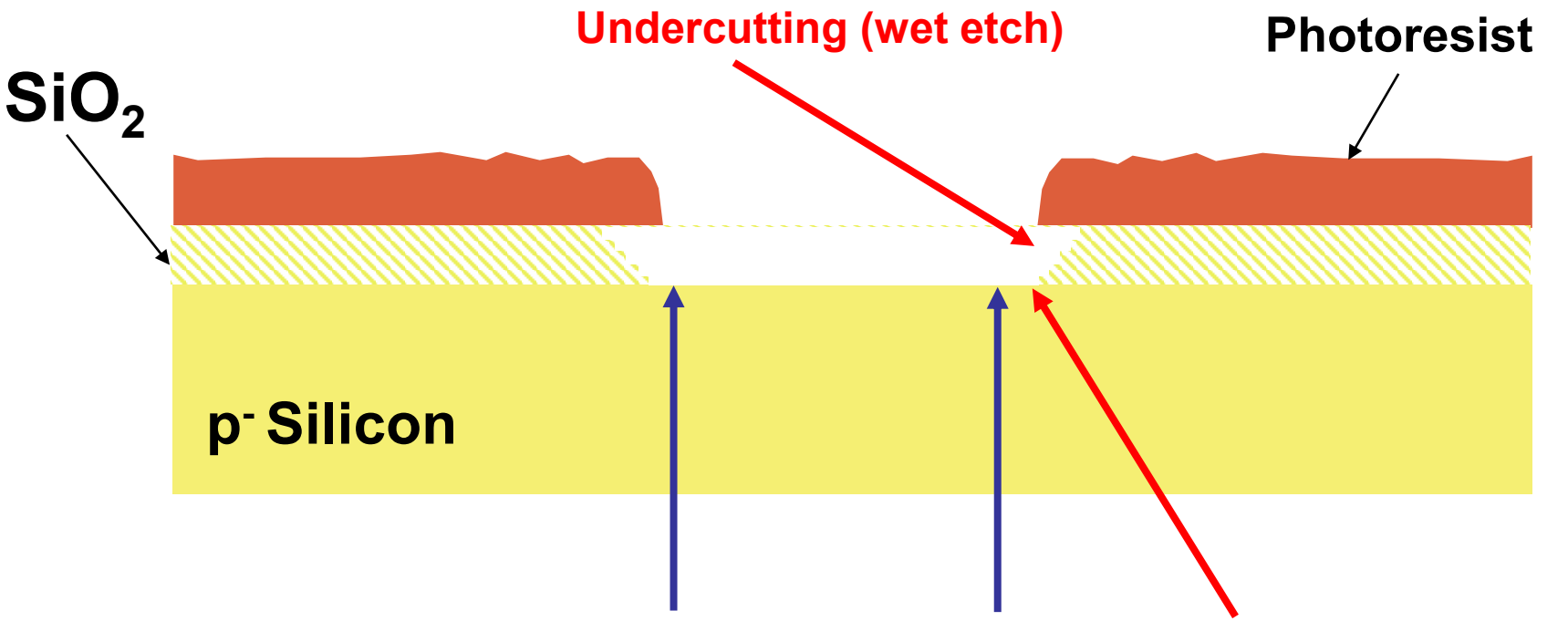


n-channel MOSFET

Still Not to Scale

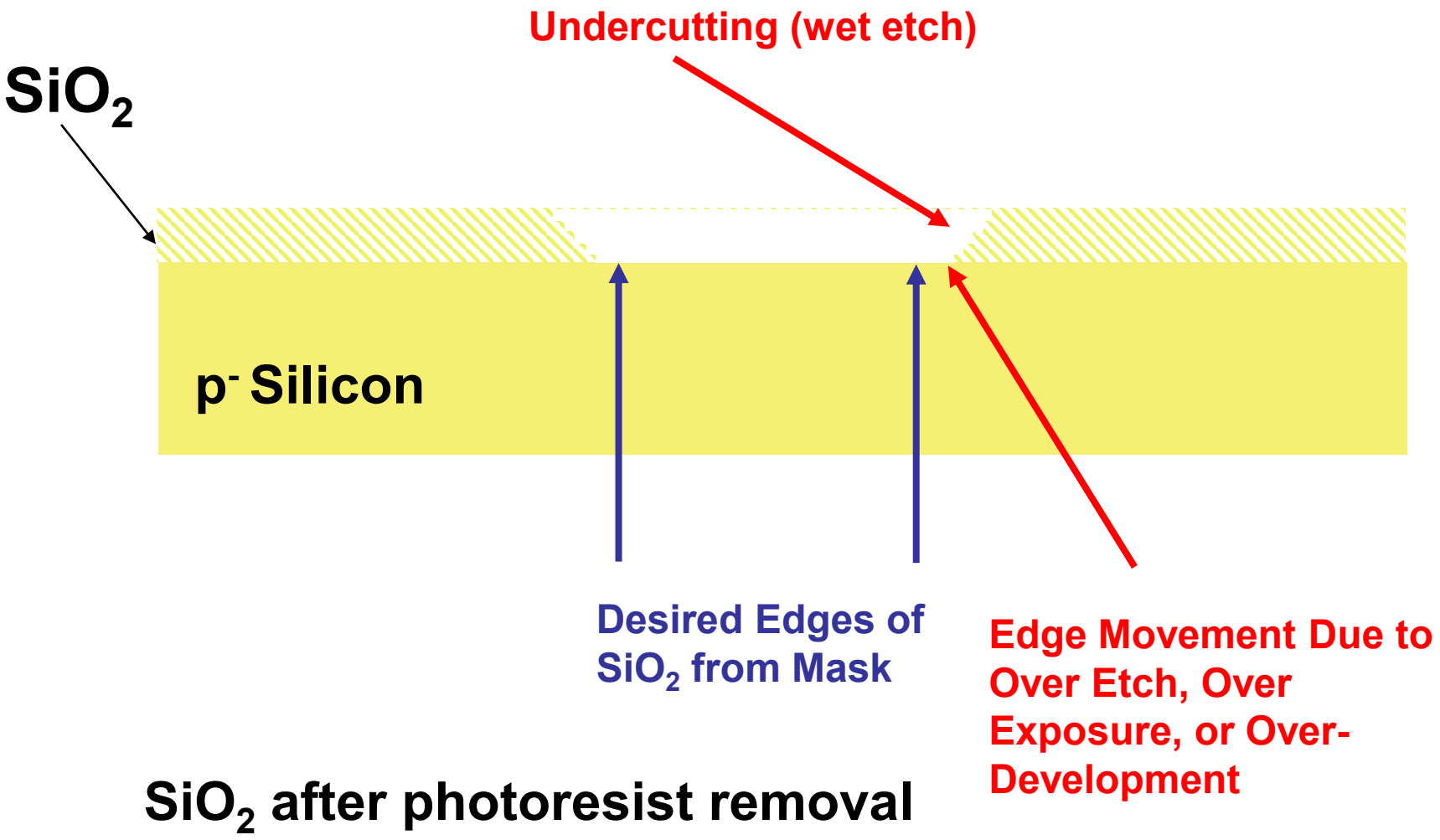
For Example, the wafer thickness is around 250u and the gate oxide is around 50A (5E-3u) and diffusion depths are around λ/5

Etching



Anisotropic etch, Feature Degradation

Etching


Undercutting (wet etch)
SiO_2
p^- Silicon
Desired Edges of SiO_2 from Mask
Edge Movement Due to Over Etch, Over Exposure, or Over-Development
SiO_2 after photoresist removal