EE 330
Lecture 9

IC Fabrication Technology
Part II
- Oxidation
- Epitaxy
- Polysilicon
- Interconnects
Review from Last Time

IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Implantation
- Etching
- Diffusion
- Oxidation
- Epitaxy
- Polysilicon
- Contacts, Interconnect and Metalization
- Planarization
Etching

Selective Removal of Unwanted Materials

- Wet Etch
  - Inexpensive but under-cutting a problem

- Dry Etch
  - Often termed ion etch or plasma etch
Review from Last Time

Diffusion

- Controlled Migration of Impurities
  - Time and Temperature Dependent
  - Both vertical and lateral diffusion occurs
  - Crystal orientation affects diffusion rates in lateral and vertical dimensions
  - Materials Dependent
  - Subsequent Movement
  - Electrical Properties Highly Dependent upon Number and Distribution of Impurities
  - Diffusion at 800°C to 1200°C

- Source of Impurities
  - Deposition
  - Ion Implantation
    - Only a few Å deep
    - More accurate control of doping levels
    - Fractures silicon crystalline structure during implant
    - Annealing occurs during diffusion
Oxidation

• SiO$_2$ is widely used as an insulator
  – Excellent insulator properties
• Used for gate dielectric
  – Gate oxide layers very thin
• Used to separate devices by raising threshold voltage
  – termed field oxide
  – field oxide layers very thick
• Methods of Oxidation
  – Thermal Growth (LOCOS)
    • Consumes host silicon
    • $x$ units of SiO$_2$ consumes $.47x$ units of Si
    • Undercutting of photoresist
    • Compromises planar surface for thick layers
    • Excellent quality
  – Chemical Vapor Deposition
    • Needed to put SiO$_2$ on materials other than Si
Review from Last Time

Oxidation

Photoresist

SiO$_2$

p$^-$ Silicon

Patterned Edges

Thermally Grown SiO$_2$ - desired growth
Review from Last Time

Oxidation

Photoresist

SiO$_2$

Bird’s Beaking

p-$\text{Silicon}$

Patterned Edges

Thermally Grown SiO$_2$ - actual growth
Review from Last Time

Oxidation

Nonplanar Surface

p$^-$ Silicon

Patterned Edges

Thermally Grown SiO$_2$ - actual growth
Oxidation

Silicon Nitride

Photoresist

Pad Oxide

p-Silicon

Shallow Trench Isolation (STI)
Oxidation

Silicon Nitride

Etched Shallow Trench

Pad Oxide

p^- Silicon

Shallow Trench Isolation (STI)
Oxidation

Silicon Nitride

CVD SiO$_2$

Pad Oxide

p$^-$ Silicon

Shallow Trench Isolation (STI)
Oxidation

Planarity Improved

Shallow Trench Isolation (STI)

Planarization Target

p^- Silicon
Oxidation

After Planarization

CVD SiO$_2$

p$^-$ Silicon

Shallow Trench Isolation (STI)
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Epitaxy

• Single Crystaline Extension of Substrate Crystal
  – Commonly used in bipolar processes
  – CVD techniques
  – Impurities often added during growth
  – Grows slowly to allow alignmnt with substrate
Epitaxy

Epitaxial Layer

Original Silicon Surface

$p^-$ Silicon

epi can be uniformly doped or graded

Question: Why can’t a diffusion be used to create the same effect as an epi layer?
IC Fabrication Technology

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Polysilicon

- Elemental contents identical to that of single crystaline silicon
  - Electrical properties much different
  - If doped heavily makes good conductor
  - If doped moderately makes good resistor
  - Widely used for gates of MOS devices
  - Widely used to form resistors
  - Grows fast over non-crystaline surface
  - Patterned with Photoresist/Etch process
  - Silicide often used in regions where resistance must be small
    - Refractory metal used to form silicide
    - Designer must indicate where silicide is applied (or blocked)
IC Fabrication Technology

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- Planarization
Contacts, Interconnect and Metalization

• Contacts usually of a fixed size
  – All etches reach bottom at about the same time
  – Multiple contacts widely used
  – Contacts not allowed to Poly on thin oxide in most processes
  – Dog-bone often needed for minimum-length devices
Contacts

Unacceptable Contact

Vulnerable to pin holes
(usually all contacts are same size)

Acceptable Contact
Contacts

Acceptable Contact
Contacts

Design Rule Violation

“Dog Bone” Contact
Contacts

Common Circuit Connection

Standard Interconnection

Buried Contact

Can save area but not allowed in many processes
Metalization

• Aluminum widely used for interconnect
• Copper finding some applications
• Must not exceed maximum current density
  – around 1ma/u
• Ohmic Drop must be managed
• Parasitic Capacitances must be managed
• Interconnects from high to low level metals require connections to each level of metal
• Stacked vias permissible in some processes
Metalization

Aluminum

- Aluminum is usually deposited uniformly over entire surface and etched to remove unwanted aluminum
- Mask is used to define area in photoresist where aluminum is to be removed

Copper

- Plasma etches not effective at removing copper because of absence of volatile copper compounds
- Barrier metal layers needed to isolate silicon from migration of copper atoms
- Damascene or Dual-Damascene processes used to pattern copper
Patterning of Aluminum

Contact Opening from Mask

Photoresist
Patterning of Aluminum

Contact Opening after SiO$_2$ etch

Photoresist
Patterning of Aluminum

Contact Opening after SiO$_2$ etch

Photoresist
Patterning of Aluminum

Metal Applied to Entire Surface
Patterning of Aluminum

Photoresist Patterned with Metal Mask
Patterning of Aluminum

Aluminum After Metal Etch (photoresist still showing)
Patterning of Copper

Damascene Process

Contact Opening after SiO$_2$ etch

Photoresist
Patterning of Copper

Damascone Process

Tungsten (W)

CMP Target
Chemical-Mechanical Planarization (CMP)

- Polishing Pad and Wafer Rotate in non-concentric pattern to thin, polish, and planarize surface
- Abrasive/Chemical polishing
- Depth and planarity are critical

Acknowledgement:
http://en.wikipedia.org/wiki/Chemical-mechanical_planarization
Patterning of Copper

Damasocene Process

After first CMP Step

W-plug

CMP Target
Patterning of Copper

Damascene Process
After first CMP Step

Oxidation
Patterning of Copper

Damasocene Process

Photoresist Patterned with Metal Mask Defines Trench
Patterning of Copper

Damasocene Process

Shallow Trench after Etch

W-plug
Patterning of Copper

Damascene Process

W-plug

Copper Deposition

CMP Target
Patterning of Copper

Damascone Process

After Second CMP Step

W-plug

Copper

CMP Target
Patterning of Copper

Dual-Damascene Process

Shallow Trench Defined in PR with Metal Mask

Photoresist
Patterning of Copper

Dual-Damascene Process

Shallow Trench After Etch

Photoresist
Patterning of Copper

Dual-Damascene Process

Via Defined in PR with Via Mask

Photoresist
Patterning of Copper

Dual-Damascene Process

Via Etch Defines Contact Region

Photoresist
Patterning of Copper

Dual-Damascene Process

Copper Deposited on Surface
Patterning of Copper

Dual-Damascene Process

Copper Deposited on Surface

CMP Target
Patterning of Copper

Dual-Damascene Process

Copper Via

Copper Interconnect

CMP Target
Patterning of Copper

Both Damascene Processes Realize Same Structure

**Damascene Process**
- Two Dielectric Deposition Steps
- Two CMP Steps
- Two Metal Deposition Steps
- Two Dielectric Etches
- W-Plug

**Dual-Damascene Process**
- One Dielectric Deposition Steps
- One CMP Steps
- One Metal Deposition Steps
- Two Dielectric Etches
- Via formed with metal step
Multiple Level Interconnects

3-rd level metal connection to n-active without stacked vias
Multiple Level Interconnects

3-rd level metal connection to n-active with stacked vias
Interconnects

• Metal is preferred interconnect
  – Because conductivity is high
• Parasitic capacitances and resistances of concern in all interconnects
• Polysilicon used for short interconnects
  – Silicided to reduce resistance
  – Unsilicided when used as resistors
• Diffusion used for short interconnects
  – Parasitic capacitances are high
Interconnects

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Parasitic capacitances and resistances of concern in all interconnects

• Polysilicon used for short interconnects
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• Diffusion used for short interconnects
  – Parasitic capacitances are high
Resistance in Interconnects

The diagram illustrates a rectangular interconnect with dimensions W and L. The resistance R is represented by the circuit symbol R between points A and B.
Resistance in Interconnects

\[ R = \frac{L}{A} \rho \]

\[ A = HW \]

\( \rho \) independent of geometry and characteristic of the process
Resistance in Interconnects

\[ R = \frac{L}{A} \rho = \frac{L}{W} \left[ \frac{\rho}{H} \right] \]

H << W and H << L in most processes
Interconnect behaves as a “thin” film
Sheet resistance often used instead of conductivity to characterize film

\[ R_\square = \frac{\rho}{H} \quad R = R_\square \left[ \frac{L}{W} \right] \]
Resistance in Interconnects

\[ R = R_{\square} \left[ \frac{L}{W} \right] \]

The “Number of Squares” approach to resistance determination in thin films

\[ N_S = 21 \]

\[ \frac{L}{W} = 21 \]

\[ R = R_{\square} N_S \]
Resistance in Interconnects

The “squares” approach is not exact but is good enough for calculating resistance in almost all applications.

In this example:

\[ N_S = 12 + 0.55 + 0.7 = 13.25 \]

\[ R = R \square 13.25 \]
End of Lecture 9