EE 330
Lecture 9
IC Fabrication Technology
Part III
- Epitaxy
- Polysilicon
- Resistance and Capacitance in Interconnects
- Back-end Processes
Devices in Semiconductor Processes
IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Ion Implantation
- Etching
- Diffusion
- Oxidation
- Epitaxy
- Polysilicon
- Contacts, Interconnect and Metalization
- Planarization
Epitaxy

• Single Crystaline Extension of Substrate Crystal
  – Commonly used in bipolar processes
  – CVD techniques
  – Impurities often added during growth
  – Grows slowly to allow alignment with substrate
epi can be uniformly doped or graded

Question: Why can’t a diffusion be used to create the same effect as an epi layer?
IC Fabrication Technology

- Crystal Preparation
- Masking
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Polysilicon

- Elemental contents identical to that of single crystaline silicon
  - Electrical properties much different
  - If doped heavily makes good conductor
  - If doped moderately makes good resistor
  - Widely used for gates of MOS devices
  - Widely used to form resistors
  - Grows fast over non-crystaline surface
  - Patterned with Photoresist/Etch process
  - Silicide often used in regions where resistance must be small
    - Refractory metal used to form silicide
    - Designer must indicate where silicide is applied (or blocked)
Polysilicon

Single-Crystaline Silicon
IC Fabrication Technology

- Crystal Preparation
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- Contacts, Interconnect and Metalization
- Planarization
Contacts, Interconnect and Metalization

• Contacts usually of a fixed size
  – All etches reach bottom at about the same time
  – Multiple contacts widely used
  – Contacts not allowed to Poly on thin oxide in most processes
  – Dog-bone often needed for minimum-length devices
Contacts

Unacceptable Contact

Vulnerable to pin holes (usually all contacts are same size)

Acceptable Contact
Contacts

Acceptable Contact
Contacts

Design Rule Violation

"Dog Bone" Contact
Contacts

Common Circuit Connection

Standard Interconnection

Buried Contact

Can save area but not allowed in many processes
Metalization

• Aluminum widely used for interconnect
• Copper finding some applications
• Must not exceed maximum current density
  – around 1ma/u
• Ohmic Drop must be managed
• Parasitic Capacitances must be managed
• Interconnects from high to low level metals require connections to each level of metal
• Stacked vias permissible in some processes
Metalization

Aluminum

- Aluminum is usually deposited uniformly over entire surface and etched to remove unwanted aluminum
- Mask is used to define area in photoresist where aluminum is to be removed

Copper

- Plasma etches not effective at removing copper because of absence of volatile copper compounds
- Barrier metal layers needed to isolate silicon from migration of copper atoms
- Damascene or Dual-Damascene processes used to pattern copper
Patterning of Aluminum

Contact Opening from Mask

Photoresist
Patterning of Aluminum

Contact Opening after SiO$_2$ etch

Photoresist
Patterning of Aluminum

Contact Opening after SiO$_2$ etch

Photoresist
Patterning of Aluminum

Metal Applied to Entire Surface
Patterning of Aluminum

Aluminum After Metal Etch (photoresist still showing)
Copper Interconnects

Limitations of Aluminum Interconnects

- Electromigration
- Conductivity not real high

Relevant Key Properties of Copper

- Reduced electromigration problems at given current level
- Better conductivity

Challenges of Copper Interconnects

- Absence of volatile copper compounds (does not etch)
- Copper diffuses into surrounding materials (barrier metal required)
Copper Interconnects

Practical methods of realizing copper interconnects took many years to develop.

Copper interconnects widely used in some processes today.
Patterning of Copper

Damascene Process

Contact Opening after SiO$_2$ etch

Photoresist
Patterning of Copper

Damascene Process

Tungsten (W)

CMP Target

W has excellent conformality when formed from WF6
Chemical-Mechanical Planarization (CMP)

- Polishing Pad and Wafer Rotate in non-concentric pattern to thin, polish, and planarize surface
- Abrasive/Chemical polishing
- Depth and planarity are critical

Acknowledgement:
http://en.wikipedia.org/wiki/Chemical-mechanical_planarization
Patterning of Copper

Damascene Process
After first CMP Step

W-plug

CMP Target
Patterning of Copper

Damasocene Process
After first CMP Step

Oxidation
Patterning of Copper

Damascene Process

Photoresist Patterned with Metal Mask Defines Trench
Patterning of Copper

Damasacene Process

Shallow Trench after Etch

W-plug
Patterning of Copper

Damascene Process

(Barrier metal added before copper to contain the copper atoms)
Patterning of Copper

Damascone Process

W-plug

Copper Deposition
Patterning of Copper

Damascene Process

W-plug

Copper Deposition

CMP Target

Copper is deposited or electroplated (Barrier Metal Used for Electroplating Seed)
Patterning of Copper

Damasocene Process

After Second CMP Step

W-plug

Copper

CMP Target
Patterning of Copper

Dual-Damascene Process

Shallow Trench Defined in PR with Metal Mask

Photoresist
Patterning of Copper

Dual-Damascene Process

Shallow Trench After Etch

Photoresist
Patterning of Copper

Dual-Damascene Process

Via Defined in PR with Via Mask

Photoresist
Patterning of Copper

Dual-Damascene Process

Via Etch Defines Contact Region

Photoresist

(Barrier Metal added before copper but not shown)
Patterning of Copper

Dual-Damascene Process

Copper is deposited or electroplated (Barrier Metal Used for Electroplating Seed)
Patterning of Copper

Dual-Damascene Process

Copper Deposited on Surface

CMP Target
Patterning of Copper

Dual-Damascene Process

Copper Interconnect

Copper Via

CMP Target
Patterning of Copper

Both Damascene Processes Realize Same Structure

**Damascene Process**
- Two Dielectric Deposition Steps
- Two CMP Steps
- Two Metal Deposition Steps
- Two Dielectric Etches
- W-Plug

**Dual-Damascene Process**
- One Dielectric Deposition Steps
- One CMP Steps
- One Metal Deposition Steps
- Two Dielectric Etches
- Via formed with metal step
Multiple Level Interconnects

3-rd level metal connection to n-active without stacked vias
Multiple Level Interconnects

3-rd level metal connection to n-active with stacked vias
Interconnect Layers May Vary in Thickness or Be Mostly Uniform

![Interconnect Layer Diagram](image)

**FIG 4.30** Interconnect geometry

<table>
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<th>( t ) (nm)</th>
<th>( w ) (nm)</th>
<th>( s ) (nm)</th>
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**FIG 4.31** Layer stack for 6-metal Intel 180 nm process
End of Lecture 9