EE 330
Lecture 9

IC Fabrication Technology
Part II

- Oxidation
- Epitaxy
- Polysilicon
- Planarization
- Resistance and Capacitance in Interconnects
IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Ion implantation
- Etching
- Diffusion
- Oxidation
- Epitaxy
- Polysilicon
- Contacts, Interconnect and Metalization
- Planarization

Review from Last Time

Use with nearly all other steps
Review from Last Time

Masking

Exposure through reticle
Photolithographic Process

- Photoresist
  - Viscous Liquid
  - Uniform Application Critical (spinner)
  - Baked to harden
  - Approx 1μ thick
  - Non-Selective
- Types
  - Negative – unexposed material removed when developed
  - Positive-exposed material removed when developed
  - Thickness about 450nm in 90nm process (ITRS 2007 Litho)

- Exposure
  - Projection through reticle with stepper (scanners becoming popular)
  - Alignment is critical !!
  - E-Bean Exposures
    - Eliminate need fro reticle
    - Capacity very small

Stepper: Optics fixed, wafer steps in fixed increments
Scanner: Wafer steps in fixed increments and during exposure both optics and wafer are moved to increase effective reticle size
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Etching

Selective Removal of Unwanted Materials

• Wet Etch
  – Inexpensive but under-cutting a problem

• Dry Etch
  – Often termed ion etch or plasma etch
Etching

Note: Vertical Dimensions in silicon generally orders of magnitude smaller than lateral dimensions so different vertical and lateral scales will be used in this discussion. Vertical dimensions of photoresist which is applied on top of wafer is about ½ order of magnitude larger than lateral dimensions.
Etching

Dry etch (anisotropic)

SiO$_2$

Photoresist

Desired Physical Features

$p^-$ Silicon

Dry Etch can provide very well-defined and nearly vertical edges (relative to photoresist patterning)
Etching (limited by photolithographic process)

SiO$_2$

Dry etch (anisotropic)

Photoresist

Consider neg photoresist

Over Exposed
Correctly Developed
Over Developed
Under Developed

Under Exposed
Correctly Developed
Over Developed
Under Developed
For Example, the wafer thickness is around 250u and the gate oxide is around 50A (5E-3u) and diffusion depths are around $\lambda/5$. 
Etching

SiO$_2$

Undercutting (wet etch)

Photoresist

p-$\text{Si}$

Desired Edges of SiO$_2$ from Mask

Edge Movement Due to Over Etch, Over Exposure, or Over-Development

Isotropic Feature Degradation
Etching

Undercutting (wet etch)

SiO₂ after photoresist removal

Desired Edges of SiO₂ from Mask

Edge Movement Due to Over Etch, Over Exposure, or Over-Development

p⁻ Silicon
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Diffusion

- Controlled Migration of Impurities
  - Time and Temperature Dependent
  - Both vertical and lateral diffusion occurs
  - Crystal orientation affects diffusion rates in lateral and vertical dimensions
  - Materials Dependent
  - Subsequent Movement
  - Electrical Properties Highly Dependent upon Number and Distribution of Impurities
  - Diffusion at 800°C to 1200°C

- Source of Impurities
  - Deposition
  - Ion Implantation
    - Depth depending on ion speed/energy
    - More accurate control of doping levels
    - Fractures silicon crystalline structure during implant
    - Annealing occurs during diffusion

- Types of Impurities
  - n-type  Arsenic, Antimony, Phosphorous
  - p-type  Gallium, Aluminum, Boron
Diffusion

Source of Impurities Deposited on Silicon Surface

Before Diffusion

After Diffusion

$p^-$ Silicon

$p^-$ Silicon
Diffusion

Source of Impurities Implanted in Silicon Surface

Before Diffusion

After Diffusion

$p^{-}$ Silicon

$p^{-}$ Silicon
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Oxidation

- SiO$_2$ is widely used as an insulator
  - Excellent insulator properties
- Used for gate dielectric
  - Gate oxide layers very thin
- Used to separate devices by raising threshold voltage
  - termed field oxide
  - field oxide layers very thick
- Methods of Oxidation
  - Thermal Growth (LOCOS)
    - Consumes host silicon
    - $x$ units of SiO$_2$ consumes $.47x$ units of Si
    - Undercutting of photoresist
    - Compromises planar surface for thick layers
    - Excellent quality
  - Chemical Vapor Deposition
    - Needed to put SiO$_2$ on materials other than Si
Oxidation

Thermally Grown SiO$_2$ - desired growth
Oxidation

Thermally Grown SiO$_2$ - actual growth
Oxidation

Nonplanar Surface

p- Silicon

Patterned Edges

Thermally Grown SiO$_2$ - actual growth
Oxidation

Silicon Nitride

Photoresist

Pad Oxide

p^- Silicon

Shallow Trench Isolation (STI)
Oxidation

Silicon Nitride

Etched Shallow Trench

Pad Oxide

p-Silicon

Shallow Trench Isolation (STI)
Oxidation

Silicon Nitride

CVD SiO$_2$

Pad Oxide

$p^-$ Silicon

Shallow Trench Isolation (STI)
Oxidation

Planarity Improved

Planarization Target

$\text{p^{-} Silicon}$

Shallow Trench Isolation (STI)
Oxidation

After Planarization

CVD SiO$_2$

p$^-$ Silicon

Shallow Trench Isolation (STI)
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Epitaxy

• Single Crystaline Extension of Substrate Crystal
  – Commonly used in bipolar processes
  – CVD techniques
  – Impurities often added during growth
  – Grows slowly to allow alignment with substrate
Epitaxy

Epitaxial Layer

Epitaxial Layer

Original Silicon Surface

p-Silicon

epi can be uniformly doped or graded

Question: Why can’t a diffusion be used to create the same effect as an epi layer?
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Polysilicon

- Elemental contents identical to that of single crystaline silicon
  - Electrical properties much different
  - If doped heavily makes good conductor
  - If doped moderately makes good resistor
  - Widely used for gates of MOS devices
  - Widely used to form resistors
  - Grows fast over non-crystaline surface
  - Patterned with Photoresist/Etch process
  - Silicide often used in regions where resistance must be small
    - Refractory metal used to form silicide
    - Designer must indicate where silicide is applied (or blocked)
Polysilicon

Polysilicon

Single-Crystaline Silicon
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Planarization

- Planarization used to keep surface planar during subsequent processing steps
  - Important for creating good quality layers in subsequent processing steps
  - Mechanically planarized
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Contacts, Interconnect and Metalization

• Contacts usually of a fixed size
  – All etches reach bottom at about the same time
  – Multiple contacts widely used
  – Contacts not allowed to Poly on thin oxide in most processes
  – Dog-bone often needed for minimum-length devices
Contacts

Unacceptable Contact

Vulnerable to pin holes
(usually all contacts are same size)

Acceptable Contact
Contacts

Acceptable Contact
End of Lecture 9